4-Bit Bi-directional Level Shifter with Automatic Direction Controller

Features

- 1.2V to 3.6V on A Port and 1.65V to 5.5V on B Port ($V_{CCA} \leq V_{CCB}$)
- V_{CC} Isolation Feature – If Either V_{CC} Input Is at GND, All Outputs Are in the High-Impedance State
- OE Input Circuit Referenced to V_{CCA}
- Low Power Consumption, 5-µA Max I_{CC}
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22

A Port

- ◆2500-V Human-Body Model (A114-F)
- ◆200-V Machine Model (A115-A)
- ◆1500-V Charged-Device Model (C101D)

B Port

- ◆15-kV Human-Body Model (A114-F)
- ◆200-V Machine Model (A115-A)
- ◆1500-V Charged-Device Model (C101D)

Description

This 4-bit non-inverting translator uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.2V to 3.6V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.65V to 5.5V. This allows for universal low-voltage bidirectional translation between any of the 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, and 5V voltage nodes. V_{CCA} should not exceed V_{CCB}.

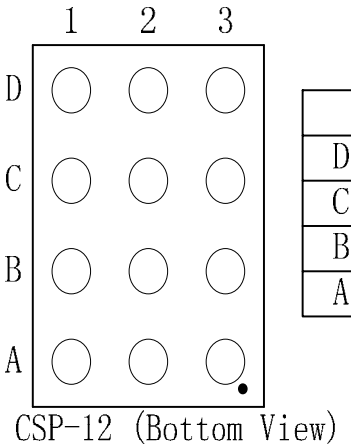
When the output-enable (OE) input is low, all outputs are placed in the high-impedance state.

The PI4ULS5V104 is designed so that the OE input circuit is supplied by V_{CCA}.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

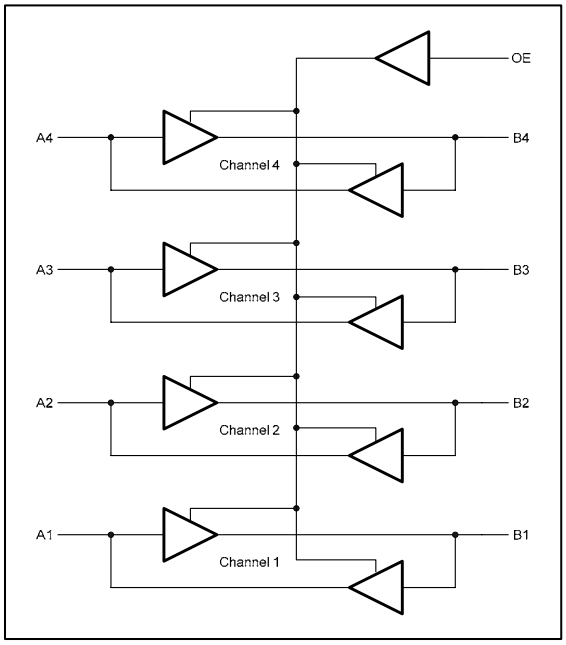
Pin Configuration



CSP-12 (Bottom View)

	1	2	3
D	B4	GND	A4
C	B3	OE	A3
B	B2	V_{CCA}	A2
A	B1	V_{CCB}	A1

Block Diagram



Maximum Ratings*1

			Min	Max	Unit
V_{CCA}	Supply voltage range		-0.5	4.6	V
V_{CCB}			-0.5	6.5	
V_I	Input voltage range	A port	-0.5	4.6	V
		B port	-0.5	6.5	
V_O	Voltage range applied to any output in the high-impedance or power-off state	A port	-0.5	4.6	V
		B port	-0.5	6.5	
V_O	Voltage range applied to any output in the high or low state*2	A port	-0.5	V_{CCA} + 0.5	V
		B port	-0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current, $V_I < 0$		-	-50	mA
I_{OK}	Output clamp current, $V_O < 0$		-	-50	mA
I_O	Continuous output current		-	±50	mA
I_O	Continuous current through V_{CCA}, V_{CCB}, or GND		-	±100	mA
T_{stg}	Storage temperature range		-65	150	℃

*1 Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
*2 The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

Pin Description

Pin Name	Description
V_{CCA}	A-port supply voltage 1.2 V ≤ V_{CCA} ≤ 3.6 V and V_{CCA} ≤ V_{CCB}.
A1	Input/output 1. Referenced to V_{CCA}.
A2	Input/output 2. Referenced to V_{CCA}.
A3	Input/output 3. Referenced to V_{CCA}.
A4	Input/output 4. Referenced to V_{CCA}.
GND	Ground
OE	3-State output. Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
B4	Input/output 4. Referenced to V_{CCB}.
B3	Input/output 3. Referenced to V_{CCB}.
B2	Input/output 2. Referenced to V_{CCB}.
B1	Input/output 1. Referenced to V_{CCB}.
V_{CCB}	B-port supply voltage 1.65 V ≤ V_{CCB} ≤ 5.5 V.

Recommend Operation Conditions(1)(2)

Parameter	Description		V_{CCA}	V_{CCB}	Min	Max	Unit
V_{CCA}	Supply voltage		-	-	1.2	3.6	V
V_{CCB}			-	-	1.65	5.5	
V_{IH}	High-level input voltage	Data inputs	1.2V to 3.6V	1.65V to 5.5V	V_{CCI} * 0.65(3)	V_{CCI}	V
		OE input	1.2V to 3.6V	1.65V to 5.5V	V_{CCA} * 0.65	5.5	
V_{IL}	Low-level input voltage	Data inputs	1.2V to 3.6V	1.65V to 5.5V	0	V_{CCI} * 0.35(3)	V
		OE input	1.2V to 3.6V	1.65V to 5.5V	0	V_{CCA}* 0.35	
V_O	Voltage range applied to any output in the high-impedance or power-off state	A port	1.2V to 3.6V	1.65V to 5.5V	0	3.6	V
		B port			0	5.5	
△t/△v	Input transition rise or fall rate	A port inputs	1.2V to 3.6V	1.65V to 5.5V	-	40	ns/V
		B port inputs		1.65V to 3.6V	-	40	
				4.5V to 5.5V	-	30	
T_A	Operating free-air temperature		-	-	-40	85	℃

(1) The A and B sides of an unused data I/O pair must be held in the same state, i.e., both at V_{CCI} or both at GND.
(2) V_{CCA} must be less than or equal to V_{CCB} and must not exceed 3.6 V.
(3) V_{CCI} is the supply voltage associated with the input port.

DC Electrical Characteristics(1)(2)

Parameter		Test Conditions	V_{CCA}	V_{CCB}	T_A = 25℃			-40 to 85℃		Unit
					Min	Typ	Max	Min	Max	
V_{OHA}		I_{OH} = -20μA	1.2V	-	1.0	1.1	1.2	-	-	V
			1.4V to 3.6V		-	-	-	V_{CCA} - 0.4	-	
V_{OLA}		I_{OL} = 20μA	1.2V	-	0.0	0.09	0.4	-	-	V
			1.4V to 3.6V		-	-	-	-	0.4	
V_{OHB}		I_{OH} = -20μA	-	1.65V to 5.5V	-	-	-	V_{CCB} - 0.4		V
V_{OLB}		I_{OL} = 20μA	-	1.65V to 5.5V	-	-	-	-	0.4	V
I_I	OE	V_I = V_{CCI} or GND	1.2 to 3.6V	1.65V to 5.5V	-	-	±1	-	±2	μA
I_{off}	A port	V_I or V_O = 0 to 3.6V	0V	0V to 5.5V	-	-	±1	-	±2	μA
	B port	V_I or V_O = 0 to 5.5V	0 to 3.6V	0V	-	-	±1	-	±2	
I_{OZ}	A or B port	OE = GND	1.2 to 3.6V	1.65V to 5.5V	-	-	±1	-	±2	μA
I_{CCA}		V_I = V_{CCI} or GND, Io = 0	1.2V	1.65V to 5.5V	0.0	0.06	5.0	-	-	μA
			1.4V to 3.6V	1.65V to 5.5V	-	-	-	-	5	
			3.6V	0V	-	-	-	-	2	
			0V	5.5V	-	-	-	-	-2	
I_{CCB}		V_I = V_{CCI} or GND, Io = 0	1.2V	1.65V to 5.5V	0	2.3	5	-	-	μA
			1.4V to 3.6V	1.65V to 5.5V	-	-	-	-	5	
			3.6V	0V	-	-	-	-	-2	
			0V	5.5V	-	-	-	-	2	
I_{CCA} + I_{CCB}		V_I = V_{CCI} or GND, Io = 0	1.2V	1.65V to 5.5V	0.0	2.4	10	-	-	μA
			1.4V to 3.6V	1.65V to 5.5V	-	-	-	-	8	
I_{CCZA}		V_I = V_{CCI} or GND, Io = 0, OE = GND	1.2V	1.65V to 5.5V	0.0	0.05	0.4	-	-	μA
			1.4V to 3.6V	1.65V to 5.5V	-	-	-	-	5	
I_{CCZB}		V_I = V_{CCI} or GND, Io = 0, OE = GND	1.2V	1.65V to 5.5V	0.0	2.3	5.0	-	-	μA
			1.4V to 3.6V	1.65V to 5.5V	-	-	-	-	5	
Ci	OE	-	1.2 to 3.6V	1.65V to 5.5V	-	3	-	-	4	pF
Cio	A port	-	1.2 to 3.6V	1.65V to 5.5V	-	5	-	-	6	pF
	B port				-	11	-	-	14	

(1) V_{CCI} is the supply voltage associated with the input port.
(2) V_{CCO} is the supply voltage associated with the output port.

AC Electrical Characteristics

Timing requirements

a. T_A = 25°C, V_{CCA} = 1.2V

			V_{CCB} = 1.8V	V_{CCB} = 2.5V	V_{CCB} = 3.3V	V_{CCB} = 5V	Unit
			TYP	TYP	TYP	TYP	
Data rate			20	20	20	20	Mbps
t_W	Pulse duration	Data inputs	50	50	50	50	ns

b. T_A = 25°C, V_{CCA} = 1.5±0.1V

			V_{CCB}=1.8±0.15V		V_{CCB}=2.5±0.2V		V_{CCB}=3.3±0.3V		V_{CCB}=5±0.5V		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Data rate			-	40	-	40	-	40	-	40	Mbps
t_W	Pulse duration	Data inputs	25	-	25	-	25	-	25	-	ns

c. T_A = 25°C, V_{CCA} = 1.8±0.15V

			V_{CCB}=1.8±0.15V		V_{CCB}=2.5±0.2V		V_{CCB}=3.3±0.3V		V_{CCB}=5±0.5V		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Data rate			-	60	-	60	-	60	-	60	Mbps
t_W	Pulse duration	Data inputs	17	-	17	-	17	-	17	-	ns

d. T_A = 25°C, V_{CCA} = 2.5±0.2V

			V_{CCB}=2.5±0.2V		V_{CCB}=3.3±0.3V		V_{CCB}=5±0.5V		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
Data rate			-	100	-	100	-	100	Mbps
t_W	Pulse duration	Data inputs	10	-	10	-	10	-	ns

e. T_A = 25°C, V_{CCA} = 3.3±0.3V

			V_{CCB}=3.3±0.3V		V_{CCB}=5±0.5V		Unit
			MIN	MAX	MIN	MAX	
Data rate			-	100	-	100	Mbps
t_W	10	-	10	-	10	-	ns

Switching characteristics

a. T_A = 25°C, V_{CCA} = 1.2V

Parameter	From (INPUT)	To (OUTPUT)	V_{CCB}=1.8V	V_{CCB}=2.5V	V_{CCB}=3.3V	V_{CCB}=5V	Unit
			TYP	TYP	TYP	TYP	
t_{pd}	A	B	6.9	5.7	5.3	5.5	ns
	B	A	7.4	6.4	6	5.8	
t_{en}	OE	A	0.2	0.2	0.2	0.2	µs
		B	0.2	0.2	0.2	0.2	
t_{dis}	OE	A	0.4	0.4	0.4	0.4	µs
		B	0.2	0.2	0.2	0.2	
t_{rA}, t_{fA}	A-port rise and fall times		4.2	4.2	4.2	4.2	ns
t_{rB}, t_{fB}	B-port rise and fall times		2.1	1.5	1.2	1.1	ns
$t_{SK(O)}$	Channel-to-channel skew		0.5	0.5	0.5	1.4	ns
Max data rate	-		20	20	20	20	Mbps

b. T_A = 25°C, V_{CCA} = 1.5±0.1V

Parameter	From (INPUT)	To (OUTPUT)	V_{CCB}=1.8±0.15V		V_{CCB} = 2.5±0.2V		V_{CCB}=3.3±0.3V		V_{CCB} = 5±0.5V		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.4	12.9	1.2	10.1	1.1	10	0.8	9.9	ns
	B	A	0.9	14.2	0.7	12	0.4	11.7	0.3	13.7	
t_{en}	OE	A	-	0.5	-	0.5	-	0.5	-	0.5	µs
		B	-	0.5	-	0.5	-	0.5	-	0.5	
t_{dis}	OE	A	-	0.5	-	0.5	-	0.5	-	0.5	µs
		B	-	0.5	-	0.5	-	0.5	-	0.5	
t_{rA}, t_{fA}	A-port rise and fall times		1.4	5.1	1.4	5.1	1.4	5.1	1.4	5.1	ns
t_{rB}, t_{fB}	B-port rise and fall times		0.9	4.5	0.6	3.2	0.5	2.8	0.4	2.7	ns
$t_{SK(O)}$	Channel-to-channel skew		-	0.5	-	0.5	-	0.5	-	0.5	ns
Max data rate			40	-	40	-	40	-	40	-	Mbps

c. T_A = 25°C, V_{CCA} = 1.8±0.15V

Parameter	From (INPUT)	To (OUTPUT)	V_{CCB}=1.8±0.15V		V_{CCB}=2.5±0.2V		V_{CCB}=3.3±0.3V		V_{CCB}=5±0.5V		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.6	11	1.4	7.7	1.3	6.8	1.2	6.5	ns
	B	A	1.5	12	1.3	8.4	1	7.6	0.9	7.1	
t_{en}	OE	A	-	0.3	-	0.25		0.25	-	0.25	µs
		B	-	0.3	-	0.25		0.25	-	0.25	
t_{dis}	OE	A	-	0.5	-	0.5		0.5	-	0.5	µs
		B	-	0.5	-	0.5		0.5	-	0.5	
t_{rA}, t_{fA}	A-port rise and fall times		1	4.2	1	4.1	1	4.1	1	4.1	ns
t_{rB}, t_{fB}	B-port rise and fall times		0.9	4.5	0.6	3.2	0.5	2.8	0.4	2.7	ns
$t_{SK(O)}$	Channel-to-channel skew		-	0.5	-	0.5	-	0.5	-	0.5	ns
Max data rate			60	-	60	-	60	-	60	-	Mbps

d. T_A = 25°C, V_{CCA} = 2.5±0.2V

Parameter	From (INPUT)	To (OUTPUT)	V_{CCB}=2.5±0.2V		V_{CCB}=3.3±0.3V		V_{CCB}=5±0.5V		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.1	6.3	1.0	5.2	0.9	4.7	ns
	B	A	1.2	6.6	1.1	5.1	0.9	4.4	
t_{en}	OE	A	-	0.25	-	0.2	-	0.2	µs
		B	-	0.25	-	0.2	-	0.2	
t_{dis}	OE	A	-	0.5	-	0.4	-	035	µs
		B	-	0.5	-	0.4	-	0.35	
t_{rA}, t_{fA}	A-port rise and fall times		0.8	3.0	0.8	3.0	0.8	3.0	ns
t_{rB}, t_{fB}	B-port rise and fall times		0.7	3.0	0.5	2.8	0.4	2.7	ns
$t_{SK(O)}$	Channel-to-channel skew		-	0.5	-	0.5	-	0.5	ns
Max data rate			100	-	100	-	100	-	Mbps

e. T_A = 25°C, V_{CCA} = 3.3±0.3V

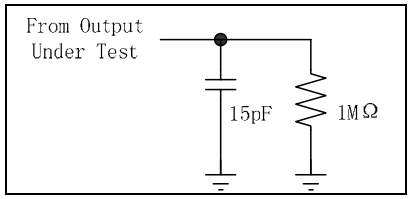
Parameter	From (INPUT)	To (OUTPUT)	V_{CCB}=3.3±0.3V		V_{CCB}=5±0.5V		Unit
			MIN	MAX	MIN	MAX	
t_{pd}	A	B	0.9	4.7	0.8	4.0	ns
	B	A	1.0	4.9	0.9	3.8	
t_{en}	OE	A	-	0.2	-	0.2	µs
		B	-	0.2	-	0.2	
t_{dis}	OE	A	-	0.3	-	0.3	µs
		B	-	0.3	-	0.3	
t_{rA}, t_{fA}	A-port rise and fall times		0.7	2.8	0.7	2.8	ns
t_{rB}, t_{fB}	B-port rise and fall times		0.5	2.7	0.4	2.7	ns
$t_{SK(O)}$	Channel-to-channel skew		-	0.5	-	0.5	ns
Max data rate	-		100	-	100	-	Mbps

Operating Characteristics

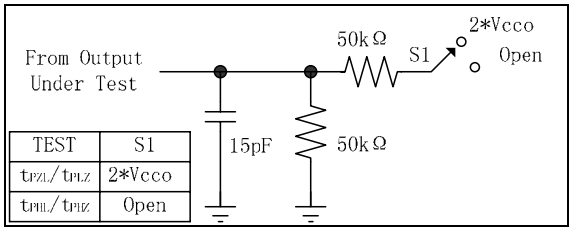
Parameter		Test Conditions	V_{CCA}							Unit
			1.2V	1.2V	1.5V	1.8V	2.5V	2.5V	3.3V	
			V_{CCB}							
			5V	1.8V	1.8V	1.8V	2.5V	5V	3.3V to 5.5V	
			TYP	TYP	TYP	TYP	TYP	TYP	TYP	
C_{pdA}	A-port input, B-port output.	C_L=0, f=10 MHz, tr = t_f=1ns, OE=V_{CCA} (outputs enabled)	7.8	10	9	8	8	8	9	pF
	B-port input, A-port output.		12	11	11	11	11	11	11	
C_{pdB}	A-port input, B-port output.		38.1	28	28	28	29	30	30	
	B-port input, A-port output.		25.4	18	18	18	18	21	21	
C_{pdA}	A-port input, B-port output.	C_L=0, f =10 MHz, tr = t_f=1ns, OE=GND (outputs disabled)	0.01	0.01	0.01	0.01	0.01	0.01	0.01	
	B-port input, A-port output.		0.01	0.01	0.01	0.01	0.01	0.01	0.01	
C_{pdB}	A-port input, B-port output.		0.01	0.01	0.01	0.01	0.01	0.01	0.03	
	B-port input, A-port output.		0.01	0.01	0.01	0.01	0.01	0.02	0.04	

Test Circuit

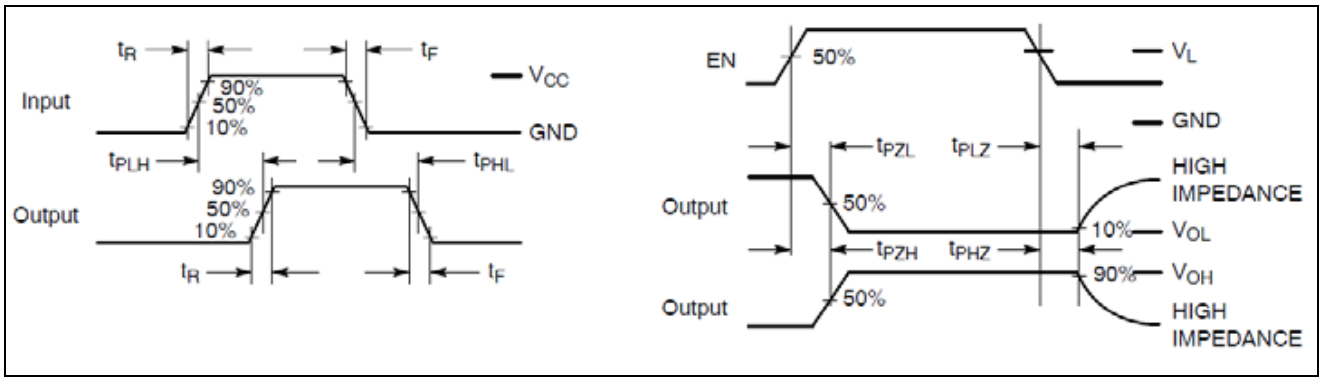
1> Load circuit for Max data rate, pulse duration propagation delay output rise and fall time measurement



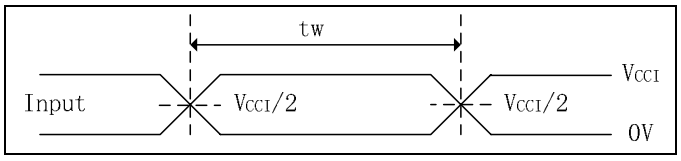
2> Load circuit for enable/disable time measurement



3> Timing Definitions for Propagation Delays and Enable/Disable Measurement



4> Voltage waveforms pulse duration



5> Notes

A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR_10 MHz, Z_O = 50 W, dv/dt ≥ 1 V/ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as tpd.
E. V_{CCI} is the V_{CC} associated with the input port.
F. V_{CCO} is the V_{CC} associated with the output port.
G. All parameters and waveforms are not applicable to all devices.

Principles of operation

Applications

The PI4ULS5V104 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another.

Architecture

The PI4ULS5V104 architecture(*see Figure1*) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a dc state, the output drivers of the PI4ULS5V104 can maintain a high or low, but are designed to be weak, so that they can be overdriven by an external driver when data on the bus starts flowing the opposite direction.

The output one shots detect rising or falling edges on the A or B ports. During a rising edge, the one shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition. The typical output impedance during output transition is 70 Ω at V_{CCO}=1.2 V to 1.8 V, 50 Ω at V_{CCO}=1.8 V to 3.3 V, and 40 Ω at V_{CCO}=3.3 V to 5 V.

Input Driver Requirements

Typical I_{IN} vs V_{IN} characteristics of the PI4ULS5V104 are shown in *Figure 2*. For proper operation, the device driving the data I/Os of the PI4ULS5V104 must have drive strength of at least ±2mA.

Power Up

During operation, ensure that $V_{CCA} \leq V_{CCB}$ at all times. During power-up sequencing, VCCA ≥ VCCB does not damage the device, so any power supply can be ramped up first. The PI4ULS5V104 has circuitry that disables all output ports when either V_{CC} is switched off ($V_{CCA/B}$ = 0 V).

Enable and Disable

The PI4ULS5V104 has an OE input that is used to disable the device by setting OE = low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time (t_{dis}) indicates the delay between when OE goes low and when the outputs acutally get disabled (Hi-Z). The enable time (ten) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

Pull-up or Pull-down Resistors on I/O Lines

The PI4ULS5V104 is designed to drive capacitive loads of up to 70 pF. The output drivers of the PI4ULS5V104 have low dc drive strength. If pullup or pulldown resistors are connected externally to the data I/Os, their values must be kept higher than 50 kΩ to ensure that they do not contend with the output drivers of the PI4ULS5V104.

For the same reason, the PI4ULS5V104 should not be used in applications such as I^2C or 1-Wire where an open-drain driver is connected on the bidirectional data I/O.

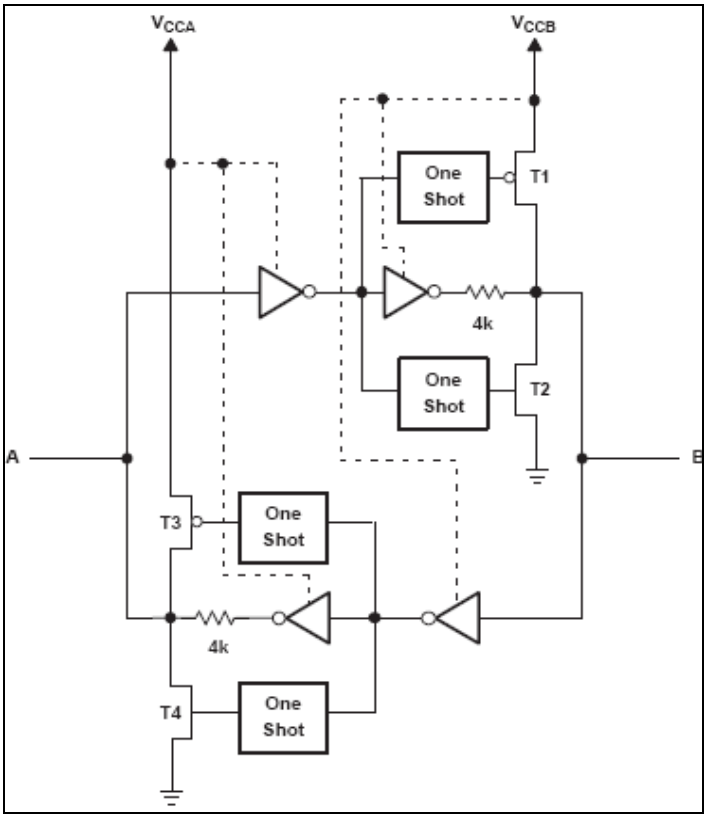


Figure1. Architecture of PI4ULS5V104 I/O Cell

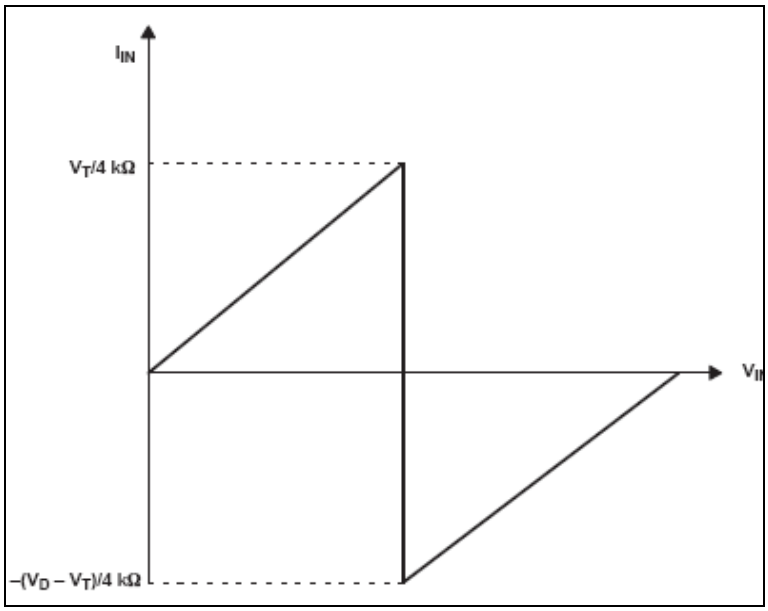
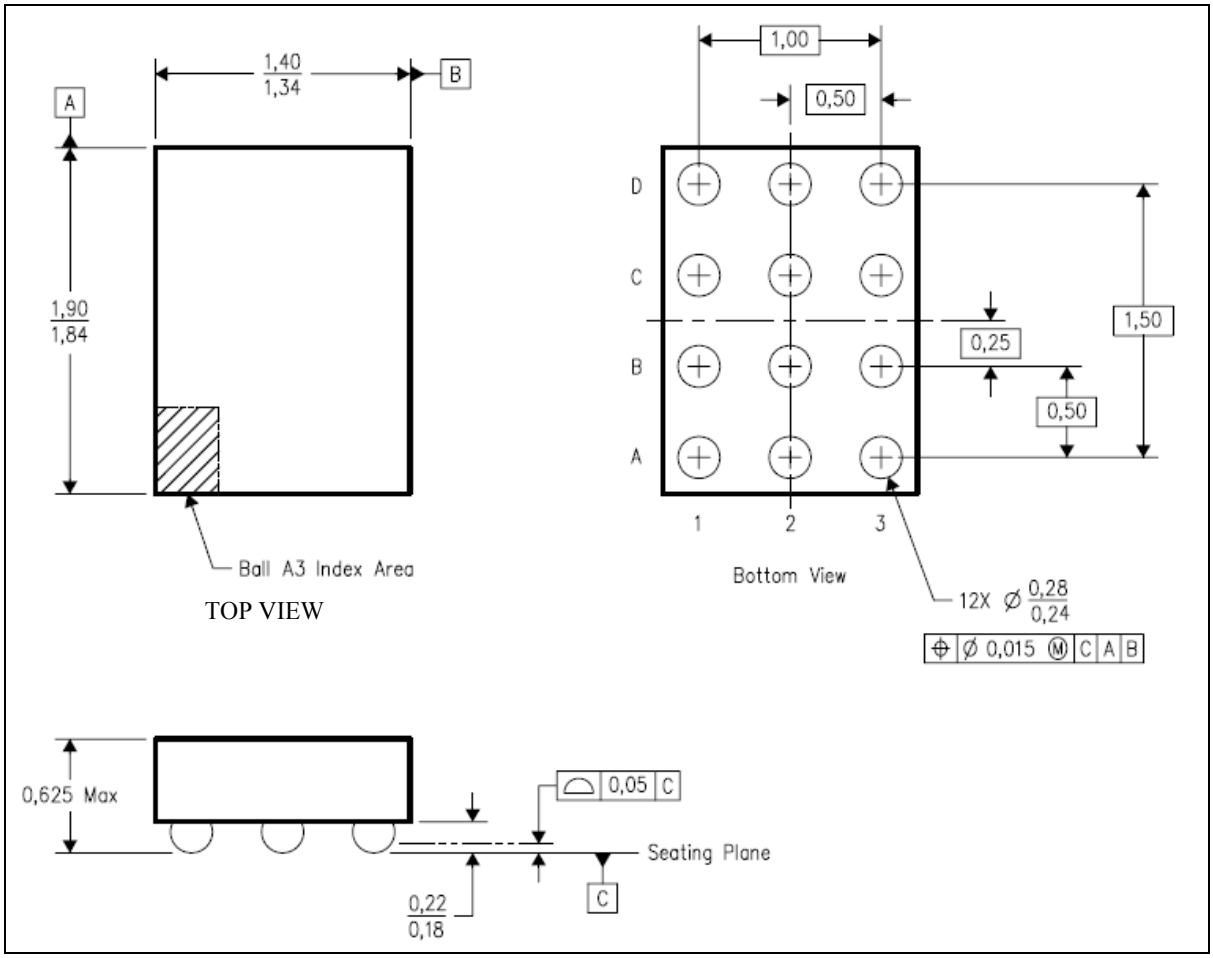


Figure2. Typical I_{IN} vs. V_{IN} Curve

Note:
A. VT is the input threshold voltage of the PI4ULS5V104 (typically $V_{CCI}/2$).
B. VD is the supply voltage of the external driver.

Mechanical Information

CSP-12



Ordering Information

Part Number	Package Code	Package
PI4ULS5V104GAE	GA	Lead free and Green 12-pin CSP

Notes:

- E = Pb-free and Green
- X Suffix= Tape and reel