MM8201

CMOS Harmonic Oscillator -CHO™
Ideal for USB 2.0 HS/FS/LS

Integrating Time™

PRELIMINARY

CMOS/3.3V/5x3.2mm

MM8201:

Powered by Mobius Microsystems' patented CMOS Harmonic Oscillator (CHO) technology, the MM8201 replaces quartz crystal based oscillators with a monolithic CMOS IC and offers programmable output frequencies at the thinnest possible form factors without the use of any mechanical frequency source or PLL.

Features:

- All-CMOS Temperature Compensated Oscillator
- No quartz or other mechanical resonators or PLL used
- Excellent reliability: Not affected by shock & vibration
- Low power operation (12mA typ)
- Low jitter leading to low Bit Error Rates (BER) on USB links
- Factory programmable output frequency (10 to 100MHz)
- Available in die form for thinnest and smallest MCP options

Ordering Information:

MM8201 -	48	V3	C	S56	C	+	T
1	2	3	4	5	6	7	8

1) Mobius Microsystems Part Number
2) Output frequency *(programmable)*
3) Supply Voltage *(V3: 3.3V)*
4) Output Signal Type *(C: CMOS)*
5) Package Type *(S56: 5x3.2mm package)*
6) Temperature Range *(C: 0 to 70°C)*
7) Environmental Compliancy *(+: Green, Pb-Free)*
8) Tape & Reel *(T: Tape& Reel shipment)*

Electrical Specifications:

VDD=3.0V to 3.6V, T_A=0 to 70°C unless otherwise noted. Typical values are measured at VDD=3.3V, T_A=35°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Storage Humidity	MSL	JEDEC Level, 85°C/85%, 168hours			1	
ElectroStaticDischarge	ESD	Human Body Model, tested per JESD D22-A114	2000			V
Supply Voltage	VDD	Normal Operation	3.0	3.3	3.6	V
Temperature	T_A	Ambient temperature in normal operation	0		70	°C
Input LOW level	V_{IL}	CE pin			30% x VDD	V
Input HIGH level	V_{IH}	CE pin	70% x VDD			V
Supply Current	IDD	Active supply current, VDD=3.3V, T=35oC, no output load		12		mA
Quiescent Current	IDDQ	CE=LOW, output disabled		0.2	1	µA
Output LOW level	V_{OL}	I_{OL} = -8mA			0.45	V
Output HIGH level	V_{OH}	I_{OH} = 8mA	VDD-0.6			V
Output Frequency	F_{OUT}	Factory Programmable.Contact Mobius for frequencies beyond the limit	10		100	MHz
Frequency Stability	F_{TOT}	Total Frequency Stability over temperature,supply variation,aging (1st year at 35oC),shock&vibration.		±400		ppm
Rise Time	RT	20% to 80% x VDD. Output load (C_L) =8pF			2.0	ns
Fall Time	FT	80% to 20% x VDD. Output load (C_L) =8pF			2.0	ns
Duty Cycle	DC	Clock output duty cycle. Measured at VDD/2, C_L=8pF	45		55	%
Power-up time	t_{on}	Output valid time after VDD meets the specified range&CE transition		1		ms
Period Jitter	PJ_{RMS}	Total RMS Period Jitter (including random and deterministic)[1,2]		3		ps_{RMS}
Cycle-cycle Jitter	CJ_{RMS}	Std dev of the max change in the periods of any 2 adjacent cycles[1,2]		6		ps_{RMS}
Phase Noise	PN	1MHz offset from carrier[1,2]		-140		dBc/Hz

Notes 1:Measured into 50Ω termination to GND
2: Measured at 40MHz output frequency

Package Drawing [mm]:

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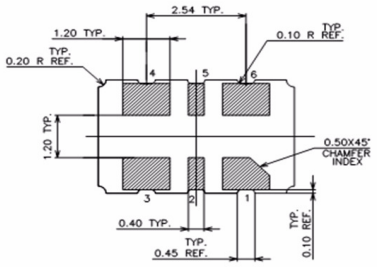
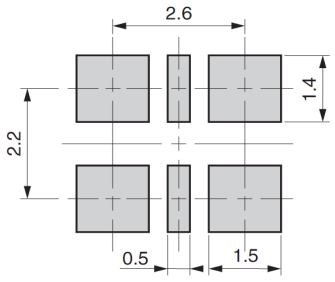


Recommended Land Pattern:



Pin Assignments:

1	CE	Chip Enable.Device active when CE is HIGH
2	NC	No Connect
3	GND	Ground
4	OUT	Clock output
5	NC	No Connect
6	VDD	Power Supply. Connect a 0.1µF cap between VDD and GND pins