DATA SHEET

CBT3857

10-bit bus switch with 10 kΩ pull-down termination resistors

Product specification
Supersedes data of 1998 Dec 10

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Philips
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10-bit bus switch with 10 kΩ pull-down termination resistors

CBT3857

FEATURES

- Enable signal is SSTL_2 compatible
- Optimized for use in Double Data Rate (DDR) SDRAM applications
- Flow-through architecture optimizes PCB layout
- Designed to be used with 200 Mbps
- Switch on resistance is designed to eliminate the need for series resistor to DDR SDRAM
- Internal 10 kΩ pull-down resistors on B port
- Internal 50 kΩ pull-up resistor on output enable input
- Full DDR solution provided when used with SSTL16857 and PCK857
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101

DESCRIPTION

This 10-bit bus switch is designed for 3 V to 3.6 V V_{CC} operation and SSTL_2 output enable ($\overline{OE}$) input levels.

When $\overline{OE}$ is LOW, the 10-bit bus switch is on and port A is connected to port B. When $\overline{OE}$ is HIGH, the switch is open, and a high-impedance state exists between the two ports.

The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The CBT3857 is characterized for operation from 0°C to +85°C.

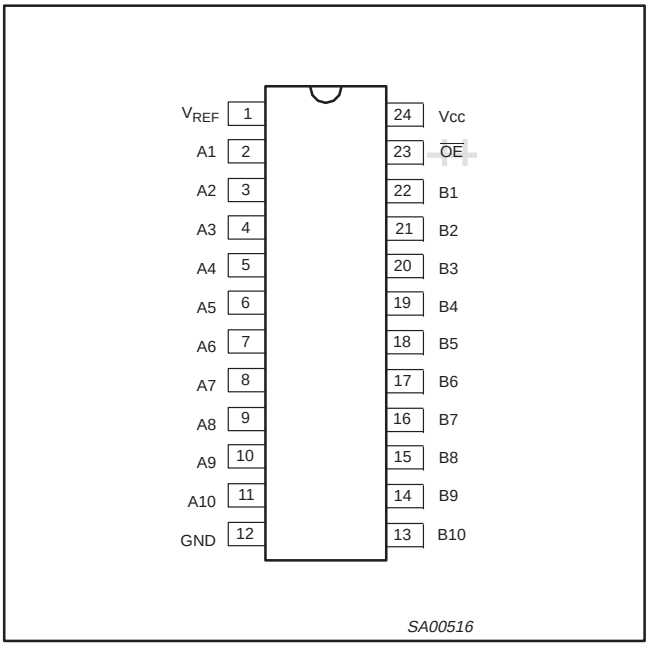
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0 V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	C_L = 30 pF; V_{CC} = 3.3 V	720	ps
C_{IN}	Input capacitance	V_I = 0 V or V_{CC}	2.8	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0 V or V_{CC}	6.4	pF
I_{CCZ}	Total supply current	V_{CC} = 3.6 V	1	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
24-Pin Plastic TSSOP Type I	0°C to +85°C	CBT3857 PW	SOT355–1

PIN CONFIGURATION



PIN DESCRIPTION

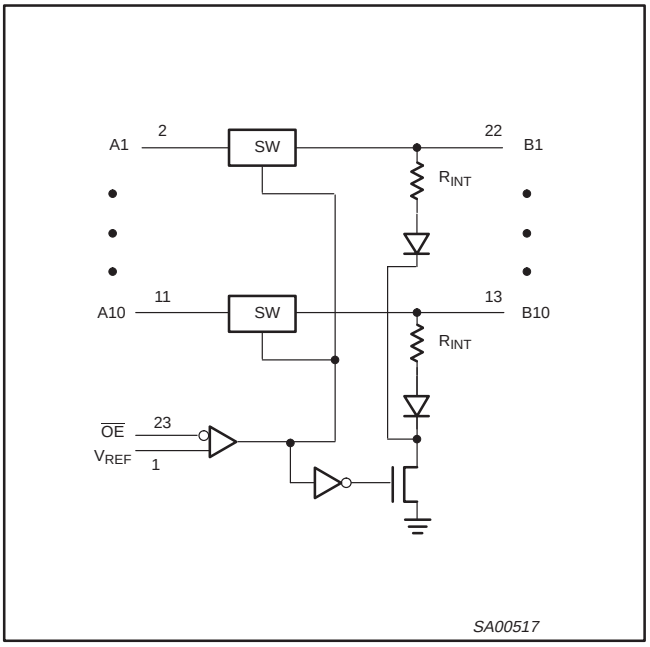
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	V_{REF}	Reference output voltage
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	A1–A10	Inputs
12	GND	Ground (V)
22, 21, 20, 19, 18, 17, 16, 15, 14, 13	B1–B10	Outputs
23	$\overline{OE}$	Output enable
24	V_{CC}	Positive supply voltage

FUNCTION TABLE

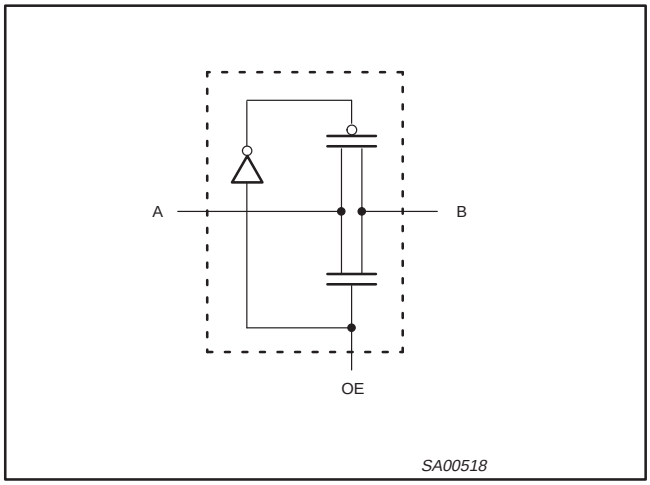
INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

H = High voltage level
L = Low voltage level

LOGIC DIAGRAM (POSITIVE LOGIC)



SIMPLIFIED SCHEMATIC, EACH FET SWITCH



ABSOLUTE MAXIMUM RATINGS[1, 3]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input clamp current	$V_{I/O} < 0$	–50	mA
V_I	DC input voltage range ($\overline{OE}$ only)[2]		V_{CC} + 0.5	V
T_{stg}	Storage temperature range		–65 to 150	°C
V_I	DC input voltage range (except $\overline{OE}$)[2]		–0.5 to 4.6	V

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. The package thermal impedance is calculated in accordance with JESD 51.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	DC supply voltage	3	3.3	3.6	V
V_{REF}	Reference voltage (0.38 x V_{CC})	1.15	1.25	1.35	V
V_{IH}	AC high-level input voltage	V_{REF} + 350 mV			V
V_{IL}	AC low-level Input voltage			V_{REF} – 350 mV	V
V_{IH}	DC high-level input voltage	V_{REF} + 180 mV			V
V_{IL}	DC low-level Input voltage			V_{REF} – 180 mV	V
T_{amb}	Operating free-air temperature range	0		+85	°C

NOTE:
1. All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

DC ELECTRICAL CHARACTERISTICS

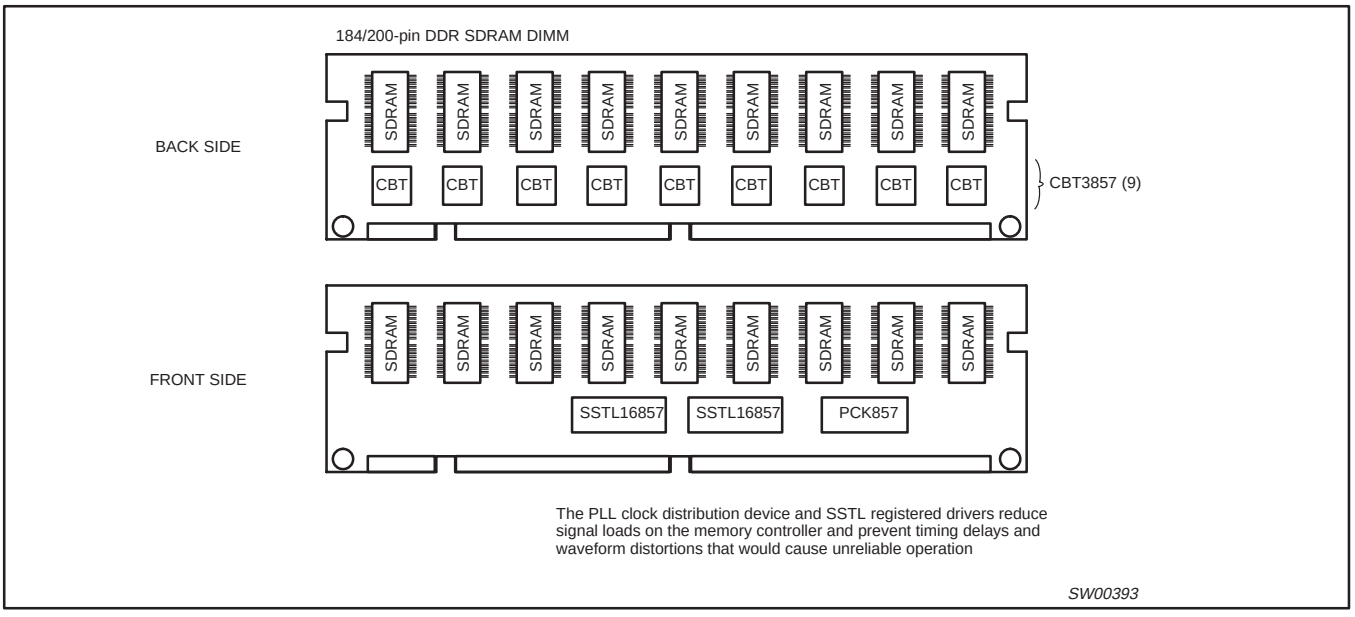
SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS T_{amb} = 0°C to +85°C			UNIT
				Min	Typ[1]	Max	
V_{IK}	Input clamp voltage	V_{CC} = 3 V; I_I = –18 mA				–1.2	V
I_I	Input leakage current	V_{CC} = 3.6 V; V_I = V_{CC} or GND	$\overline{OE}$		±0.73	±500	µA
			A Port		±0.1	±1	µA
			B Port		±20	±500	µA
			V_{REF}		±0.1	±1	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6 V; I_O = 0, V_I = V_{CC} or GND			0.7	1.5	mA
C_I	Control pins	V_I= 3 V or 0			2.8		pF
$Ci_{O(OFF)}$	Power-off leakage current	V_O = 3 V or 0; $\overline{OE}$ = V_{CC}			6.4		pF
r_{on}[2]	On-resistance	V_{CC} = 3 V to 3.6 V; V_A = 0.8 V; V_B = 1.15 V		20	24	30	Ω
		V_{CC} = 3 V to 3.6 V; V_A = 1.7 V; V_B = 1.35 V		20	24	30	
		V_{CC} = 3 V to 3.6 V; V_I = 1.25 V; I_I = ±10 mA		20	24	30	
r_{off}[2]	Off-resistance	V_{CC} = 3 V to 3.6 V; V_I = 1.65 V		1			MΩ

NOTES:
1. All typical values are at V_{CC} = 3.3 V, T_{amb} = 25°C
2. Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On–state resistance is determined by the lowest voltage of the two (A or B) terminals.

AC CHARACTERISTICS

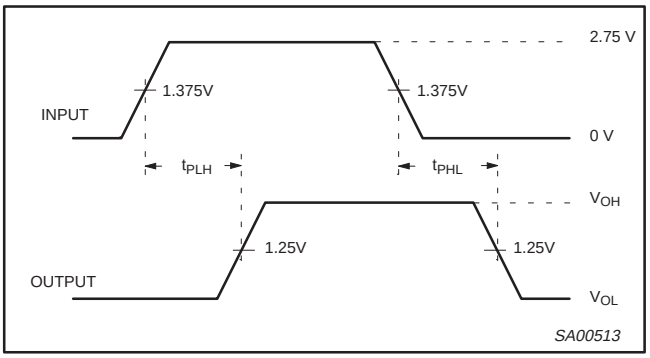
SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = +3.3 V ±0.3 V		UNIT
				Min	Max	
t_{pd}	Propagation delay[1]	A or B	B or A		750	ps
t_{en}	enable	$\overline{OE}$	A or B	1	3	ns
t_{dis}	disable	$\overline{OE}$	A or B	1	3	ns

NOTE:
1. The propagation delay is based on the RC time constant of the typical on–state resistance of the switch and a load capacitance, when driven by an ideal voltage source (zero output impedance); 24 Ω × 30 pF.

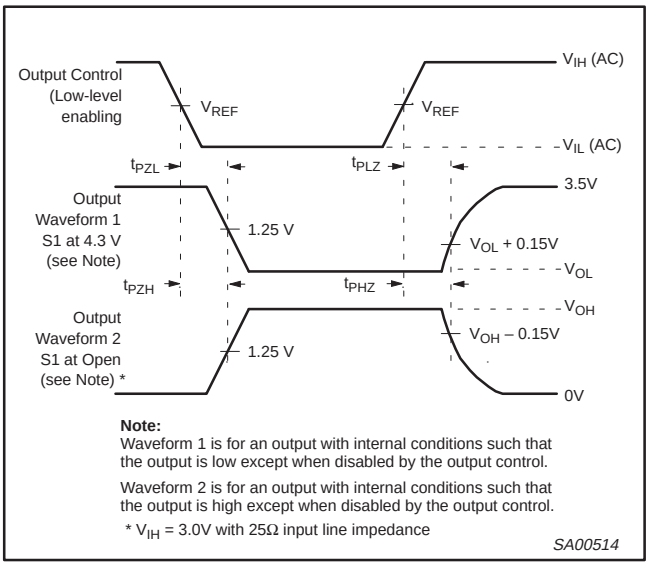


AC WAVEFORMS

V_M = 1.5 V, V_{IN} = GND to 3.0 V

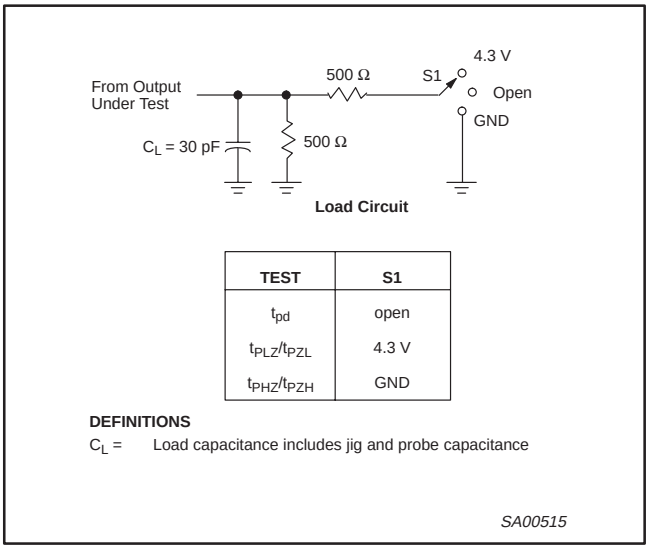


Waveform 1. Input (An) to Output (Yn) Propagation Delays



Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



TEST	S1
t_{pd}	open
t_{PLZ}/t_{PZL}	4.3 V
t_{PHZ}/t_{PZH}	GND

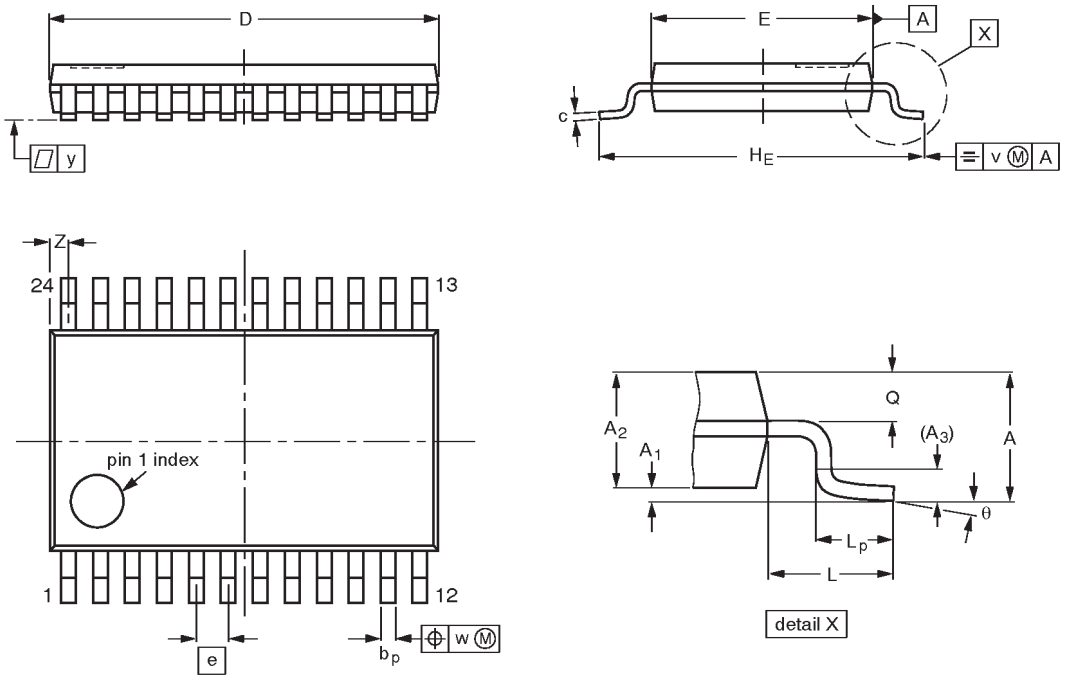
DEFINITIONS

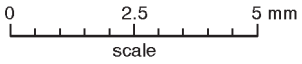
C_L = Load capacitance includes jig and probe capacitance

NOTES:

1. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
2. The outputs are measured one at a time with one transition per measurement.

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm SOT355-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				~~93-06-16~~ 95-02-04

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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