INTEGRATED CIRCUITS

DATA SHEET

CBT3245 Octal bus switch

Product data Supersedes data of 2000 Jun 19 File under Integrated Circuits ICL03





Octal bus switch CBT3245

FEATURES

- Standard '245-type pinout
- ullet 5 Ω switch connection between two ports
- TTL compatible control input levels
- Package options include plastic small outline (D), shrink small outline (DB), thin shrink small outline (TSSOP)
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection exceeds 2000 V HBM per JESD22-A114,
 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101

DESCRIPTION

The CBT3245 provides eight bits of high-speed TTL-compatible bus switching in a standard '245 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The CBT3245 device is organized as one 8-bit switch. When enable (\overline{OE}) is low, the switch is on and port A is connected to port B. When \overline{OE} is high, the switch is open and a high-impedance state exists between the two ports.

The CBT3245 is characterized for operation from -40 to 85 °C.

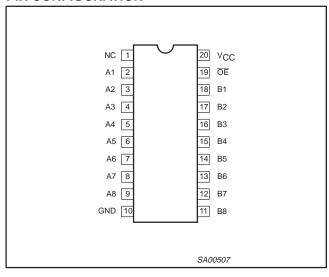
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T _{amb} = 25 °C; GND = 0 V	TYPICAL	UNIT
t _{PLH} t _{PHL}	Propagation delay An to Yn	$C_L = 50 \text{ pF}; V_{CC} = 5 \text{ V}$	250	ps
C _{IO(OFF)}	Pin capacitance (OFF state)	V _O = 3 V or 0 V	6	pF
Icc	Quiescent supply current	$V_{CC} = 5.5 \text{ V}; I_O = 0; V_I = V_{CC} \text{ or GND}$	1	μΑ

ORDERING INFORMATION

<u> </u>			
PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
20-Pin Plastic TSSOP Type I	−40 to 85 °C	CBT3245PW	SOT360-1
20-Pin Plastic SSOP Type I	−40 to 85 °C	CBT3245DB	SOT339-1
20-Pin Plastic SOP Type I	−40 to 85 °C	CBT3245D	SOT163-1

PIN CONFIGURATION

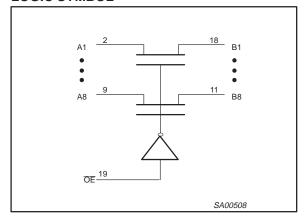


PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION			
1	NC	No internal connection			
19	ŌĒ	Output enable input			
2, 3, 4, 5, 6, 7, 8, 9	A1–A8	Inputs			
18, 17, 16, 15, 14, 13, 12, 11	B1-B8	Outputs			
10	GND	Ground (0V)			
20	V _{CC}	Positive supply voltage			

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LOGIC SYMBOL



FUNCTION TABLE

INPUT	INPUTS/OUTPUTS				
ŌĒ	A, B				
L	A = B				
Н	Z				

H = High voltage level L = Low voltage level

Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT	
V _{CC}	DC supply voltage		-0.5 to +7.0	V	
I _{IK}	DC input diode current	V ₁ < 0	-50	mA	
VI	DC input voltage ³		-0.5 to +7.0	V	
I _{OK}	DC output diode current	V _O < 0	-50	mA	
V _{OUT}	DC output voltage ³	output in Off or High state	−0.5 to +7	V	
I _{OUT}	DC output current	output in Low state	128	mA	
T _{stg}	Storage temperature range		-65 to 150	°C	

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the
 device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to
 absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
- 3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIM	UNIT	
STWIBUL	PARAMETER	Min	Max	UNII
V _{CC}	DC supply voltage	4.0	5.5	V
V _{IH}	High-level input voltage	2.0	_	V
V _{IL}	Low-level Input voltage	_	0.8	V
T _{amb}	Operating free-air temperature range	-40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

				LIMITS		
SYMBOL	PARAMETER	TEST CONDITIONS	T _{amb}	UNIT		
			Min	Typ ¹	Max	1
V _{IK}	Input clamp voltage	$V_{CC} = 4.5 \text{ V; } I_I = -18 \text{ mA}$	_	_	-1.2	V
II	Input leakage current	V _{CC} = 5.5 V; V _I = GND or 5.5 V	_	_	±5	μА
I _{CC}	Quiescent supply current	$V_{CC} = 5.5 \text{ V}; I_O = 0, V_I = V_{CC} \text{ or GND}$	_	1	3	μА
Δl _{CC}	Additional supply current per input pin ²	V_{CC} = 5.5 V, one input at 3.4 V, other inputs at V_{CC} or GND	_	_	3.5	mA
Cl	Control pins	$V_I = 3 \text{ V or } 0, \overline{OE} = V_{CC}$	_	3	_	pF
C _{IO(OFF)}	Power-off leakage current	$V_O = 3 \text{ V or } 0$	_	6	_	pF
		$V_{CC} = 4.5 \text{ V}; V_1 = 0 \text{ V}; I_1 = 64 \text{ mA}$	_	5	7	
r _{on} 3	On-resistance	$V_{CC} = 4.5 \text{ V}; V_1 = 0 \text{ V}; I_1 = 30 \text{ mA}$	_	5	7	Ω
		V _{CC} = 4.5 V; V ₁ = 2.4 V; I _I = 15 mA	_	10	15	1

NOTES:

- 1. All typical values are at V_{CC} = 5 V, TA = 25 °C
- This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND
 Measured by the voltage drop between the A and the B terminals at the indicated current through the switch.
 On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

AC CHARACTERISTICS

 $GND = 0 V; t_{R;} C_{L} = 50 pF$

				74CB	Г3245		
SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _{amb} = -40 V _{CC} = +5.0	UNIT		
				Min	Max		
t _{pd}	Propagation delay ¹	A or B	B or A	_	0.25	ns	
t _{en}	Output enable time to High and Low level	ŌĒ	A or B	1.0	6.7	ns	
t _{dis}	Output disable time from High and Low level	ŌĒ	A or B	1.0	6.4	ns	

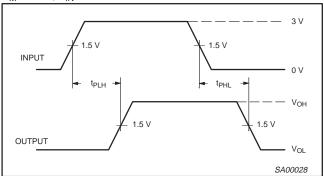
NOTES:

^{1.} This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

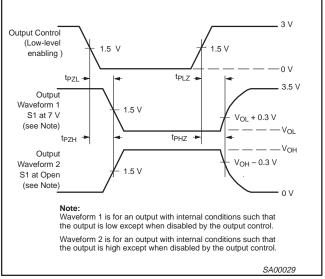
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AC WAVEFORMS

 $V_M = 1.5 \text{ V}, V_{IN} = \text{GND to } 3.0 \text{ V}$

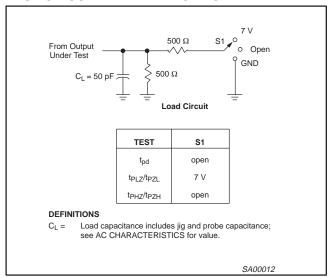


Waveform 1. Input to Output Propagation Delays



Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



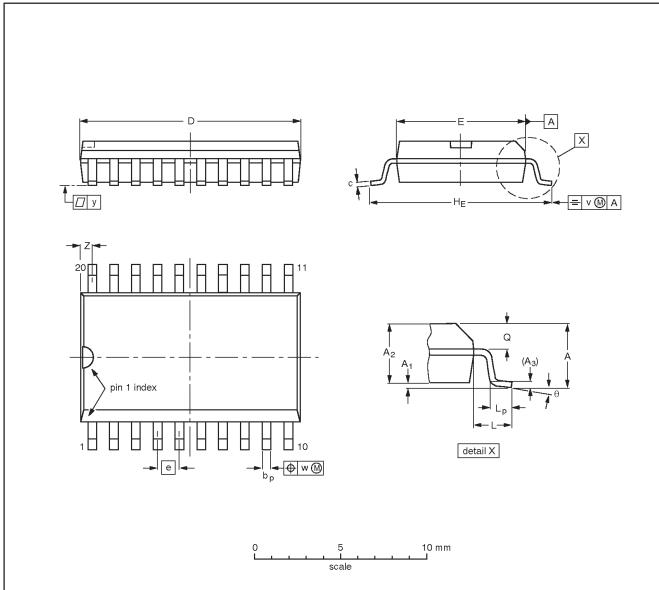
NOTES:

- 1. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \ \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- 2. The outputs are measured one at a time with one transition per measurement.

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	А3	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016		0.01	0.01	0.004	0.035 0.016	0°

Note

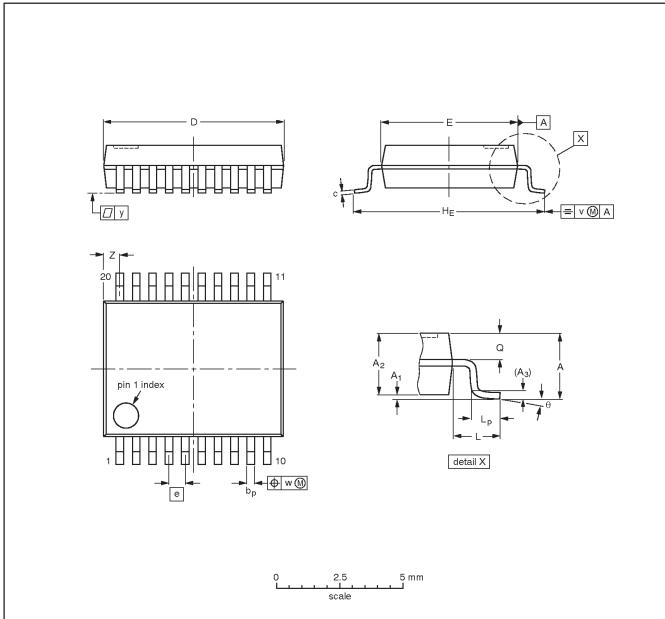
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	EIAJ		PROJECTION	1330E DATE
SOT163-1	075E04	MS-013				-97-05-22 99-12-27

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SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	А3	bp	c	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	٧	w	у	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note

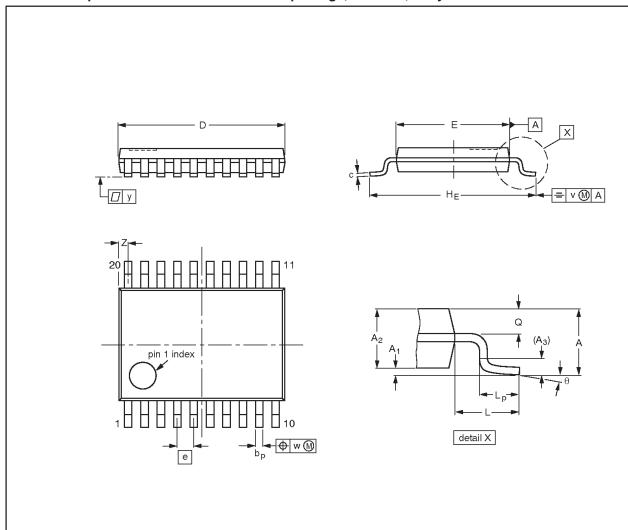
1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

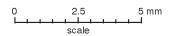
OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE
SOT339-1		MO-150				-95-02-04 99-12-27

Octal bus switch CBT3245

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	А3	bp	С	D ⁽¹⁾	E ⁽²⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE	
SOT360-1		MO-153				-95-02-04 99-12-27	

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NOTES

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