INTEGRATED CIRCUITS

DATA SHEET

CBT3253

Dual 1-of-4 FET multiplexer/demultiplexer

Product data 2002 Nov 04





Dual 1-of-4 FET multiplexer/demultiplexer

CBT3253

FEATURES

- ullet 5 Ω switch connection between two ports
- TTL-compatible input levels
- Minimal propagation delay through the switch
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA

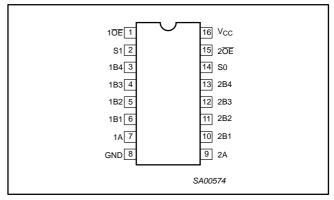
DESCRIPTION

The CBT3253 is a dual 1-of-4 high-speed TTL-compatible FET multiplexer/demultiplexer. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

 $1\overline{\text{OE}}, 2\overline{\text{OE}},$ S0, and S1 select the appropriate B output for the A-input data.

The CBT3251 is characterized for operation from -40 to +85°C.

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	1 OE	Output enable
2	S1	Select-control input
3, 4, 5, 6	1B[1-4]	B outputs
7	1A	A input
8	GND	Ground (0 V)
9	2A	A input
10, 11, 12, 13	2B[1-4]	Select-control input
14	S0	Select-control input
15	2 OE	Output enable
16	V _{CC}	Positive supply voltage

ORDERING INFORMATION

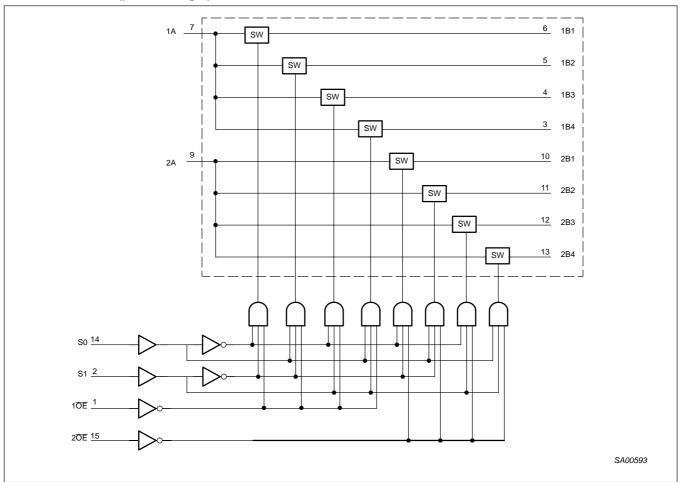
PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DWG NUMBER
16-pin plastic SO	–40 to 85 °C	CBT3253D	CBT3253D	SOT109-1
16-pin plastic SSOP	–40 to 85 °C	CBT3253DB	CT3253	SOT338-1
16-pin plastic SSOP (QSOP)	–40 to 85 °C	CBT3253DS	CBT3253	SOT519-1
16-pin plastic TSSOP	-40 to 85 °C	CBT3253PW	CBT3253	SOT403-1

Standard packing quantities and other packaging data is available at www.philipslogic.com/packaging.

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LOGIC DIAGRAM (positive logic)



FUNCTION TABLE

	INP	JTS		FUNCTION
OE1	OE2	S1	S0	FUNCTION
Н	Х	Х	Х	Disconnect 1A
Х	Н	Х	Х	Disconnect 2A
L	L	L	L	1A to 1B1 and 2A to 2B1
L	L	L	Н	1A to 1B2 and 2A to 2B2
L	L	Н	L	1A to 1B3 and 2A to 2B3
L	L	Н	Н	1A to 1B4 and 2A to 2B4

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ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +7.0	V
VI	DC input voltage ²		-0.5 to +7.0	V
	Continuous channel current		128	mA
Ι _Κ	Input clamp current	V _{I/O} < 0	-50	mA
T _{stg}	Storage temperature range		-65 to +150	°C

NOTES

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIM	UNIT	
STWIBUL	PARAMETER	MIN	MAX	UNIT
V _{CC}	DC supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2	_	V
V_{IL}	Low-level Input voltage	_	0.8	V
T _{amb}	Operating free-air temperature range	-40	+85	°C

NOTE:

DC ELECTRICAL CHARACTERISTICS

					LIMITS		
SYMBOL	PARAMETER		TEST CONDITIONS	T _{amb}	, = -40 to +8	35 °C	UNIT
				MIN	TYP ¹	MAX	
V_{IK}	Input clamp voltage		$V_{CC} = 4.5 \text{ V}; I_I = -18 \text{ mA}$	_	_	-1.2	V
V_{P}	Pass voltage		$V_I = V_{CC} = 5.5 \text{ V}; I/O = -100 \mu\text{A}$	3.4	3.6	3.9	V
lį	Input leakage current		$V_{CC} = 5 \text{ V}; V_I = 5.5 \text{ or GND}$	_	_	±1	μΑ
I _{CC}	Quiescent supply current		$V_{CC} = 5.5 \text{ V}; I_{O} = 0, V_{I} = V_{CC} \text{ or GND}$	_	_	3	μΑ
ΔI_{CC}	Control inputs ²		V_{CC} = 5.5 V, one input at 3.4 V, other inputs at V_{CC} or GND	_	_	2.5	mA
C _I	Control pins		V _I = 3 V or 0	_	4.5	_	pF
C	Dower off looked autront	A port	$V_O = 3 \text{ V or 0}; \overline{OE} = V_{CC}$	_	23.5	_	~F
C _{IO(OFF)}	Power-off leakage current	B port	$V_O = 3 \text{ V or 0}; \overline{OE} = V_{CC}$	_	6.5	_	pF
			V _I = 0 V; I _I = 64 mA	_	5	7	
r_{on}^3	On-resistance	$V_{CC} = 4.5 \text{ V}$	V _I = 0 V; I _I = 30 mA	_	5	7	Ω
			V _I = 2.4 V; I _I = -15 mA	_	10	15	1

NOTES:

- 1. All typical values are at V_{CC} = 5 V, T_{amb} = 25 °C.
- 2. This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND
- Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

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^{1.} Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

^{2.} The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Dual 1-of-4 FET multiplexer/demultiplexer

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AC CHARACTERISTICS

 T_{amb} = -40 to +85 °C; C_L = 50 pF

				LIM	ITS	
SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = +5.0$	UNIT	
			(0011 01)	MIN	MAX	
	Dronagation delay1	A or B	B or A	_	0.25	20
t _{pd}	Propagation delay ¹	S	A or B	1.2	6.2	ns
	Output enable time	S	A or B	1.3	6.3	20
t _{en}	to High and Low level	ŌĒ	AUIB	1.4	6.4	ns
	Output disable time	S	A or D	1.1	7.2	20
t _{dis}	from High and Low level	ŌĒ	A or B	1.0	7	ns

NOTE:

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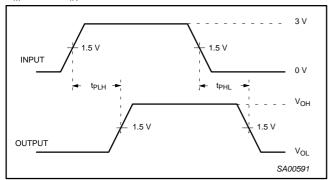
^{1.} The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

Dual 1-of-4 FET multiplexer/demultiplexer

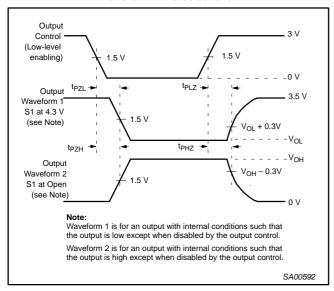
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AC WAVEFORMS

 $V_M = 1.5 \text{ V}, V_{IN} = \text{GND to } 3.0 \text{ V}$



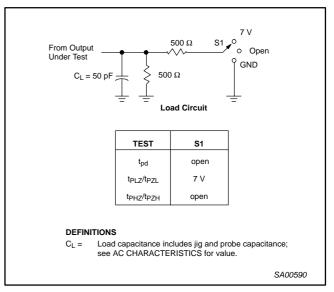
Waveform 1. Pulse duration



Waveform 2. 3-State Output Enable and Disable Times NOTES:

- 1. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en}.
 t_{PLH} and t_{PHL} are the same as t_{pd}.

TEST CIRCUIT AND WAVEFORMS



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- All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
- The outputs are measured one at a time with one transition per measurement.

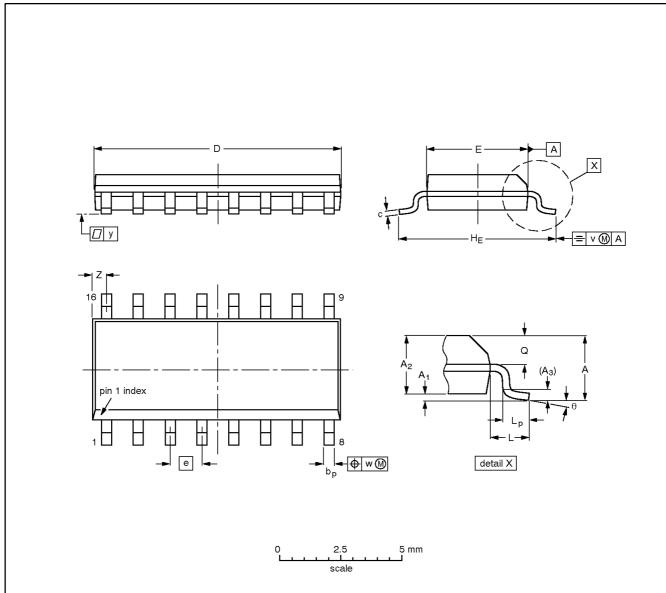
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Dual 1-of-4 FET multiplexer/demultiplexer

CBT3253

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	bр	c	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Ö	>	w	у	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016		0.01	0.01	0.004	0.028 0.012	o°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

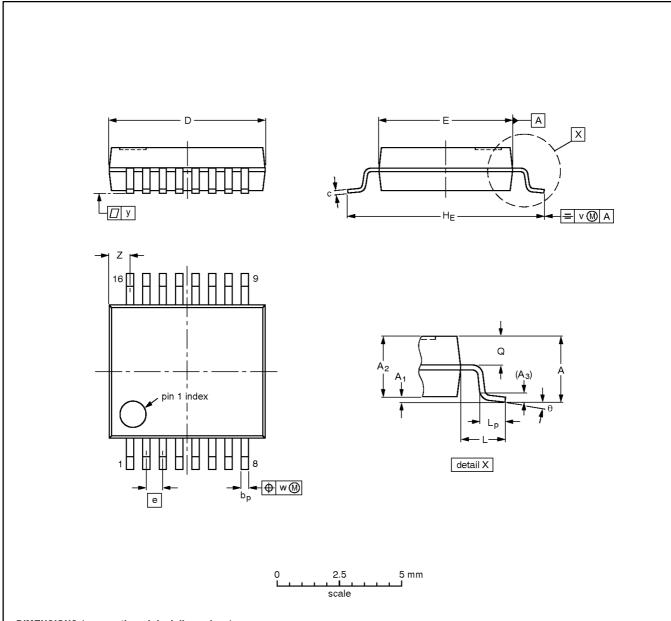
OUTLINE		REFER	EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	EIAJ	PROJECTION	1330E DATE
SOT109-1	076E07	MS-012			97-05-22 99-12-27

Dual 1-of-4 FET multiplexer/demultiplexer

CBT3253

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



DIMENSIONS (mm are the original dimensions)

U	NIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
r	mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

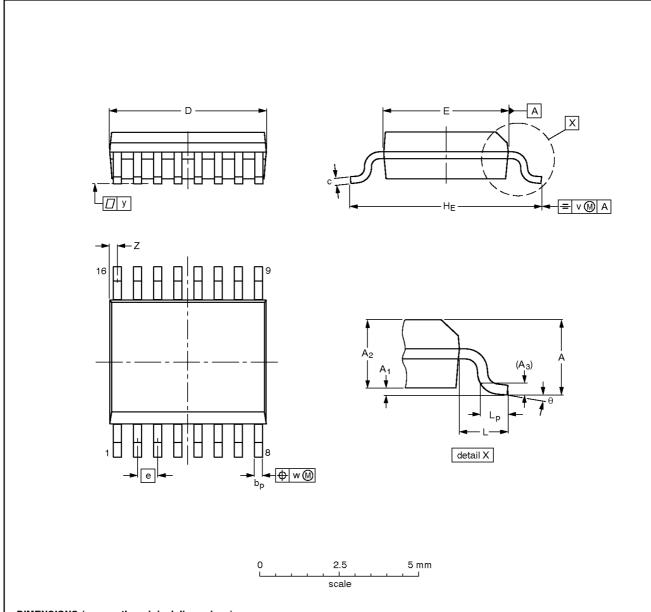
OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE
SOT338-1		MO-150				-95-02-04- 99-12-27

Dual 1-of-4 FET multiplexer/demultiplexer

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SSOP16: plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm

SOT519-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	v	w	у	Z ⁽¹⁾	θ
mm	1.73	0.25 0.10	1.55 1.40	0.25	0.31 0.20	0.25 0.18	5.0 4.8	4.0 3.8	0.635	6.2 5.8	1.0	0.89 0.41	0.2	0.18	0.09	0.18 0.05	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

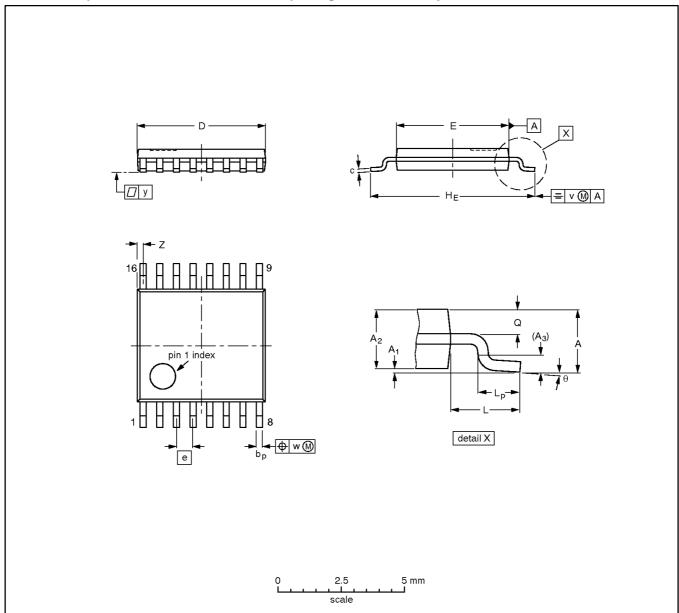
OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE	
SOT519-1						99-05-04	

Dual 1-of-4 FET multiplexer/demultiplexer

CBT3253

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	bр	С	D ⁽¹⁾	E ⁽²⁾	е	HE	L	Lp	Q	٧	w	у	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	EIAJ		PROJECTION	1350E DATE	
SOT403-1		MO-153				-95-04-04 99-12-27	

Dual 1-of-4 FET multiplexer/demultiplexer

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REVISION HISTORY

Rev	Date	Description
_1	2002 Nov 04	Product data (9397 750 10664); initial version
		Engineering Change Notice: 853–2389 29065 (2002 Oct 15)

Dual 1-of-4 FET multiplexer/demultiplexer

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Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definitions
ı	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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^[1] Please consult the most recently issued data sheet before initiating or completing a design.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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