

CBT3257A

Quad 1-of-2 multiplexer/demultiplexer

Rev. 02 — 4 July 2007

Product data sheet

1. General description

The CBT3257A is a quad 1-of-2 high-speed TTL-compatible multiplexer/demultiplexer. The low ON-state resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

Output enable (\overline{OE}) and select-control (S) inputs select the appropriate nB1 and nB2 outputs for the nA input data.

The CBT3257A is characterized for operation from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$.

2. Features

- $5\ \Omega$ switch connection between two ports
- TTL-compatible input levels
- Minimal propagation delay through the switch
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC standard JESD78 which exceeds 100 mA

3. Ordering information

Table 1. Ordering information

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$.

Type number	Topside mark	Package		
		Name	Description	Version
CBT3257AD	CBT3257AD	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
CBT3257ADB	3257A	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
CBT3257ADS	CT3257A	SSOP16 ^[1]	plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm	SOT519-1
CBT3257APW	CT3257A	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

[1] Also known as QSOP16.

4. Functional diagram

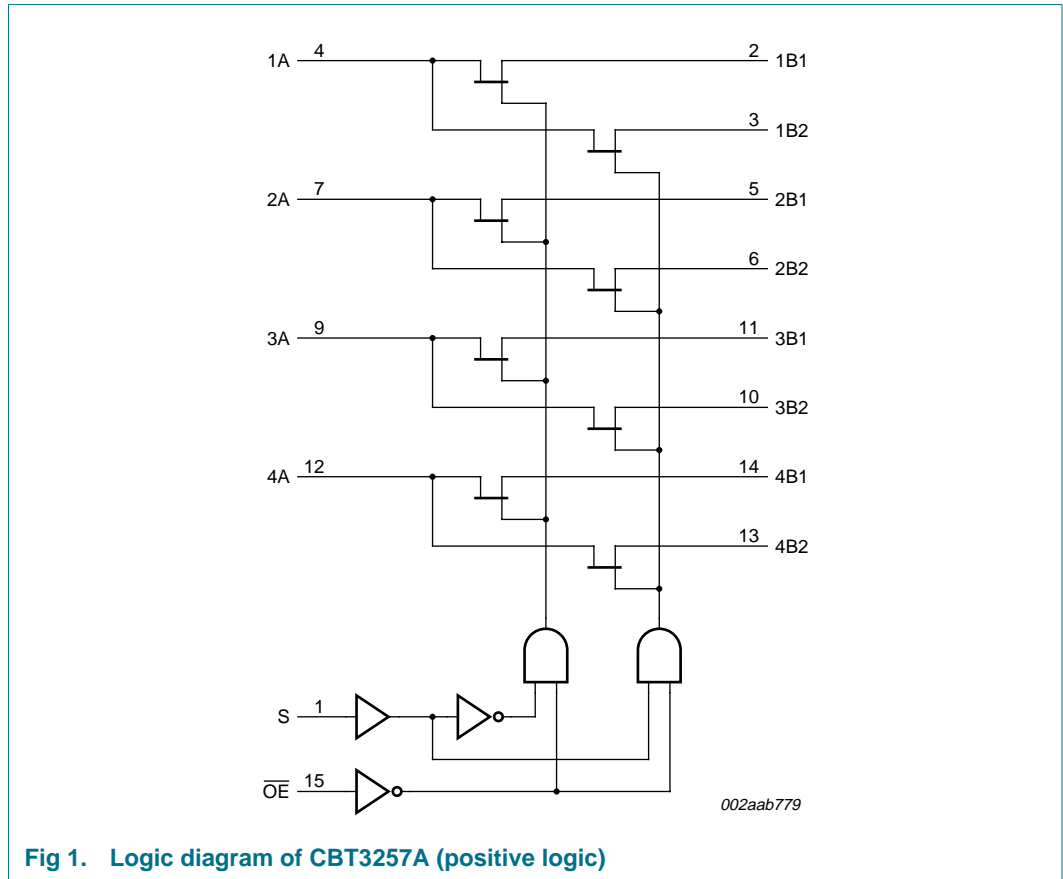
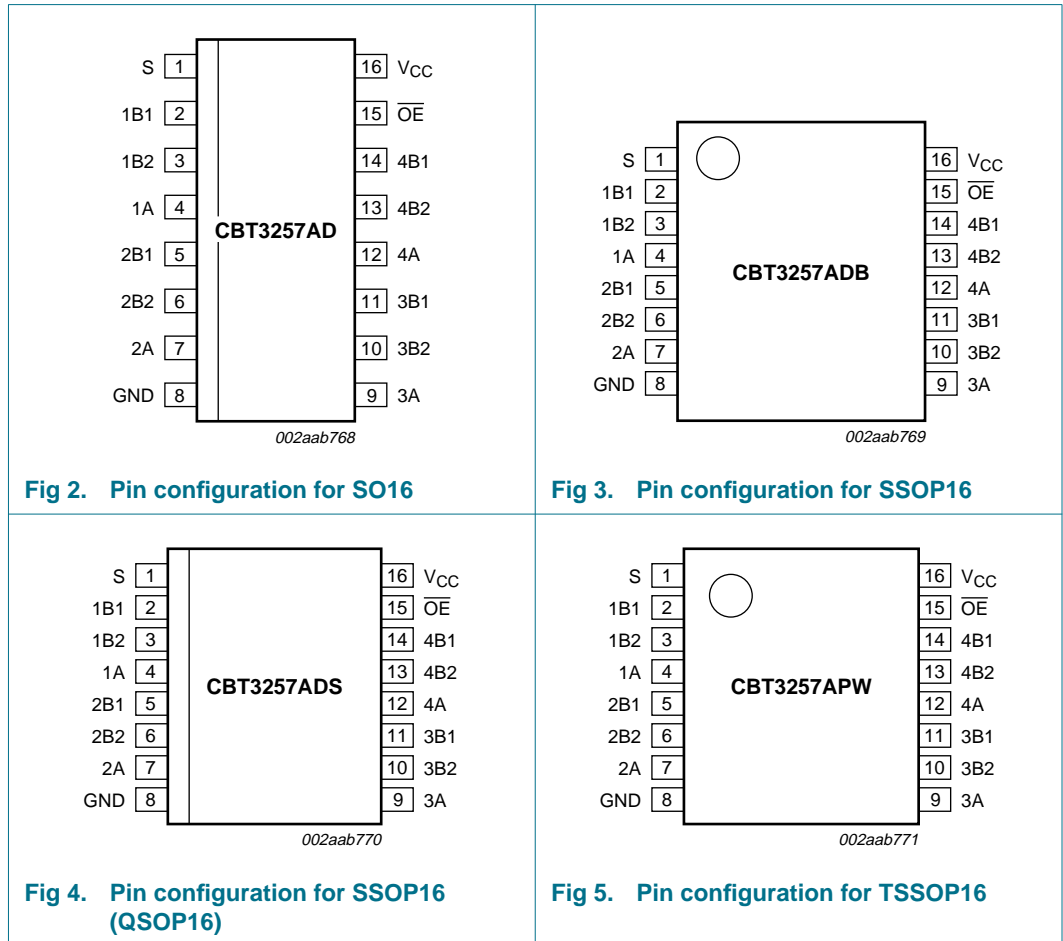


Fig 1. Logic diagram of CBT3257A (positive logic)

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
S	1	select control input
1B1, 1B2, 2B1, 2B2, 3B1, 3B2, 4B1, 4B2	2, 3, 5, 6, 10, 11, 13, 14	B outputs ^[1]
1A, 2A, 3A, 4A	4, 7, 9, 12	A inputs
GND	8	ground (0 V)
\overline{OE}	15	output enable (active LOW)
V _{CC}	16	positive supply voltage

[1] B outputs are inputs if A inputs are outputs.

6. Functional description

Refer to [Figure 1 “Logic diagram of CBT3257A \(positive logic\)”](#).

6.1 Function table

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; X = Don't care.

Inputs		Function
OE	S	
L	L	A port = B1 port
L	H	A port = B2 port
H	X	disconnect

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage		[1] -0.5	+7.0	V
I_{CCC}	continuous current through each V_{CC} or GND pin		-	128	mA
I_{IK}	input clamping current	$V_I < 0\text{ V}$	-	-50	mA
T_{stg}	storage temperature		-65	+150	°C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

8. Recommended operating conditions

Table 5. Operating conditions

All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
T_{amb}	ambient temperature	operating in free-air	-40	-	+85	°C

9. Static characteristics

Table 6. Static characteristics

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
V_{IK}	input clamping voltage	$V_{CC} = 4.5\text{ V}$; $I_I = -18\text{ mA}$	-	-	-1.2	V
V_{pass}	pass voltage	$V_I = V_{CC} = 5.0\text{ V}$; $I_O = -100\text{ }\mu\text{A}$	3.4	3.6	3.9	V
I_{LI}	input leakage current	$V_{CC} = 5.5\text{ V}$; $V_I = \text{GND}$ or 5.5 V	-	-	± 1	μA
I_{CC}	supply current	$V_{CC} = 5.5\text{ V}$; $I_O = 0\text{ mA}$; $V_I = V_{CC}$ or GND	-	-	3	μA
ΔI_{CC}	additional supply current	per input; $V_{CC} = 5.5\text{ V}$; one input at 3.4 V , other inputs at V_{CC} or GND	^[2] -	-	2.5	mA
C_I	input capacitance	control pins; $V_I = 3\text{ V}$ or 0 V	-	3.3	-	pF
$C_{io(off)}$	off-state input/output capacitance	A port; $V_O = 3\text{ V}$ or 0 V ; $\overline{OE} = V_{CC}$	-	9.9	-	pF
		B port; $V_O = 3\text{ V}$ or 0 V ; $\overline{OE} = V_{CC}$	-	6.4	-	pF
R_{on}	ON-state resistance	$V_{CC} = 4.5\text{ V}$	^[3] -	-	-	-
		$V_I = 0\text{ V}$; $I_I = 64\text{ mA}$	-	5	7	Ω
		$V_I = 0\text{ V}$; $I_I = 30\text{ mA}$	-	5	7	Ω
		$V_I = 2.4\text{ V}$; $I_I = 15\text{ mA}$	-	10	15	Ω

[1] All typical values are measured at $V_{CC} = 5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

[2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND .

[3] Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two (A or B) terminals.

10. Dynamic characteristics

Table 7. Dynamic characteristics

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; $V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$; $C_L = 50\text{ pF}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{pd}	propagation delay	from nA input to nBn output, or from nBn input to nA output	^[1] -	-	0.25	ns
		from S input to nA output	^[1] 1.6	-	5.0	ns
t_{en}	enable time	from \overline{OE} input to nA or nBn output	^[2] 1.8	-	5.1	ns
		from S input to nBn output	^[2] 1.6	-	5.2	ns
t_{dis}	disable time	from \overline{OE} input to nA or nBn output	^[3] 2.2	-	5.5	ns
		from S input to nBn output	^[3] 1.0	-	5.0	ns

[1] This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical ON-state resistance of the switch and a load capacitance, when driven by an ideal voltage source (zero output impedance).

[2] Output enable time to HIGH and LOW level.

[3] Output disable time from HIGH and LOW level.

10.1 AC waveforms

$V_I = \text{GND to } 3.0 \text{ V.}$

t_{PLZ} and t_{PHZ} are the same as t_{dis} .

t_{PZL} and t_{PZH} are the same as t_{en} .

t_{PLH} and t_{PHL} are the same as t_{pd} .

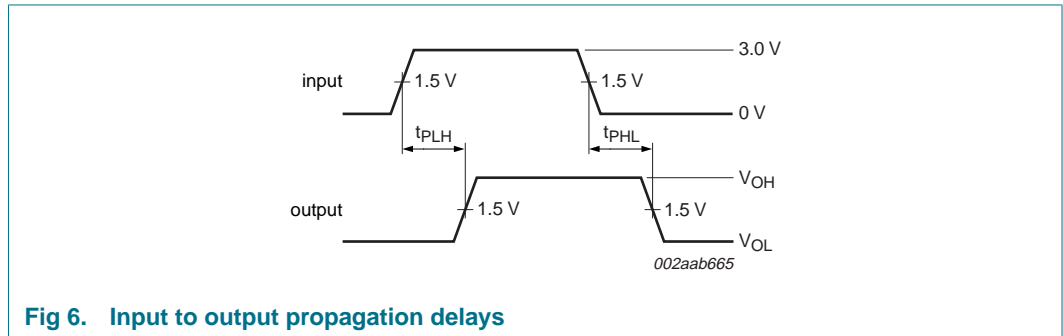
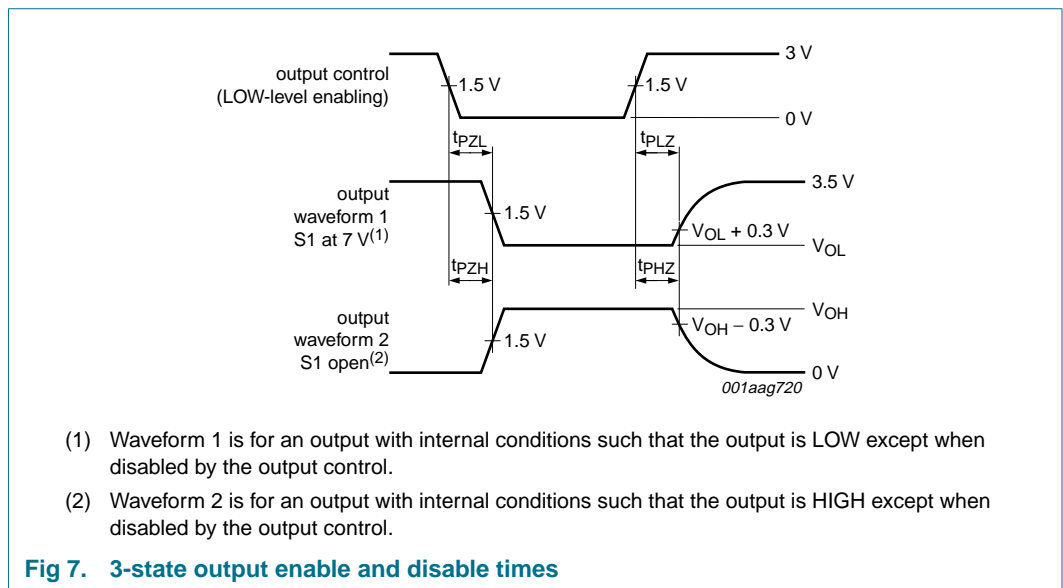


Fig 6. Input to output propagation delays



- (1) Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control.
- (2) Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.

Fig 7. 3-state output enable and disable times

11. Test information

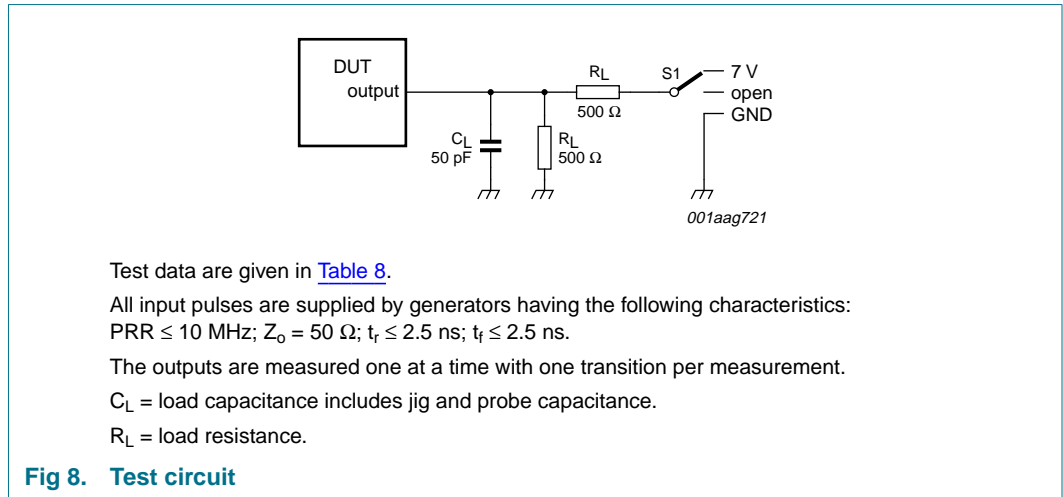


Table 8. Test data

Test	Load		Switch
	C_L	R_L	
t_{pd}	50 pF	500 Ω	open
t_{PLZ} , t_{PZL}	50 pF	500 Ω	7 V
t_{PHZ} , t_{PZH}	50 pF	500 Ω	open

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

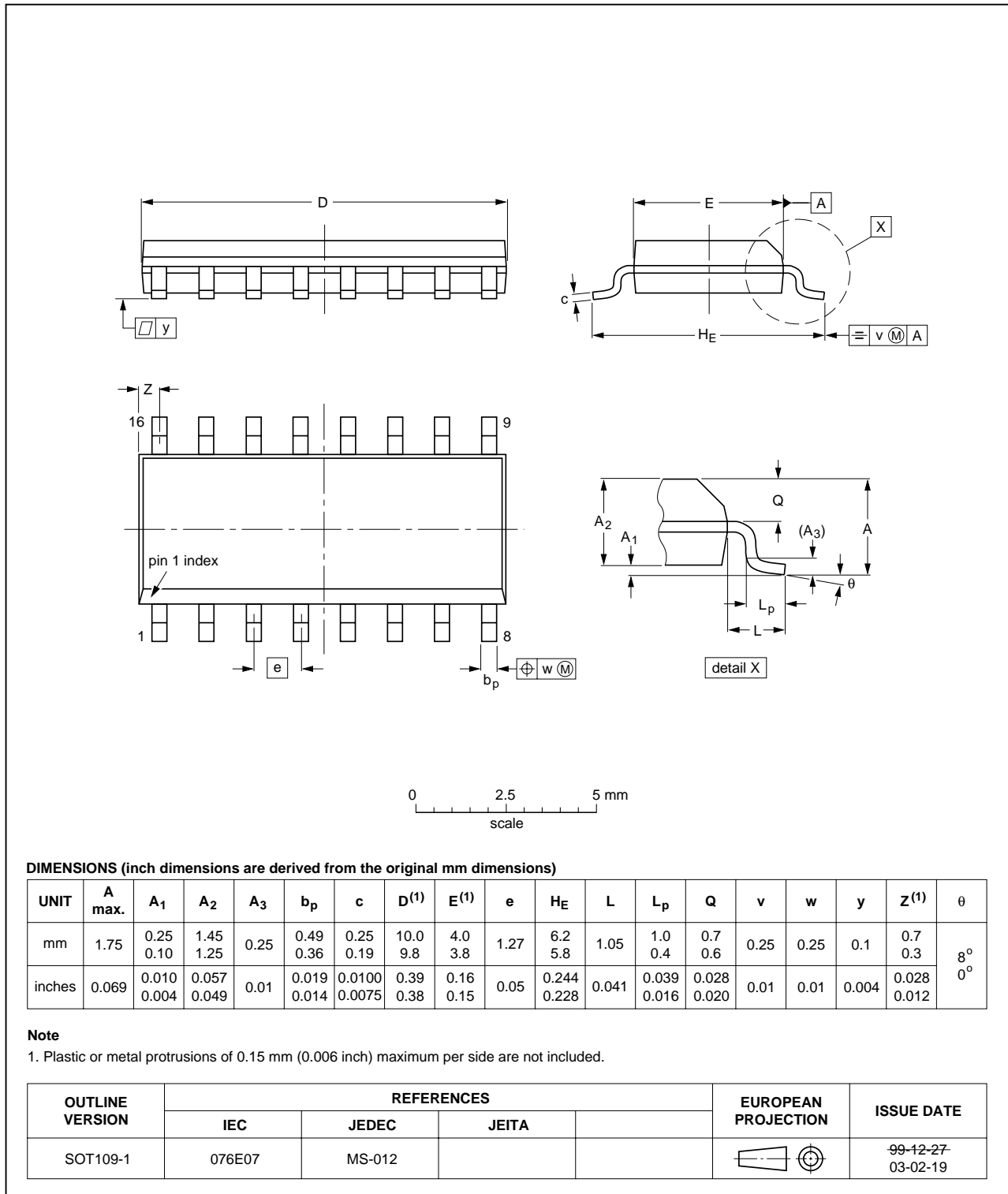


Fig 9. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

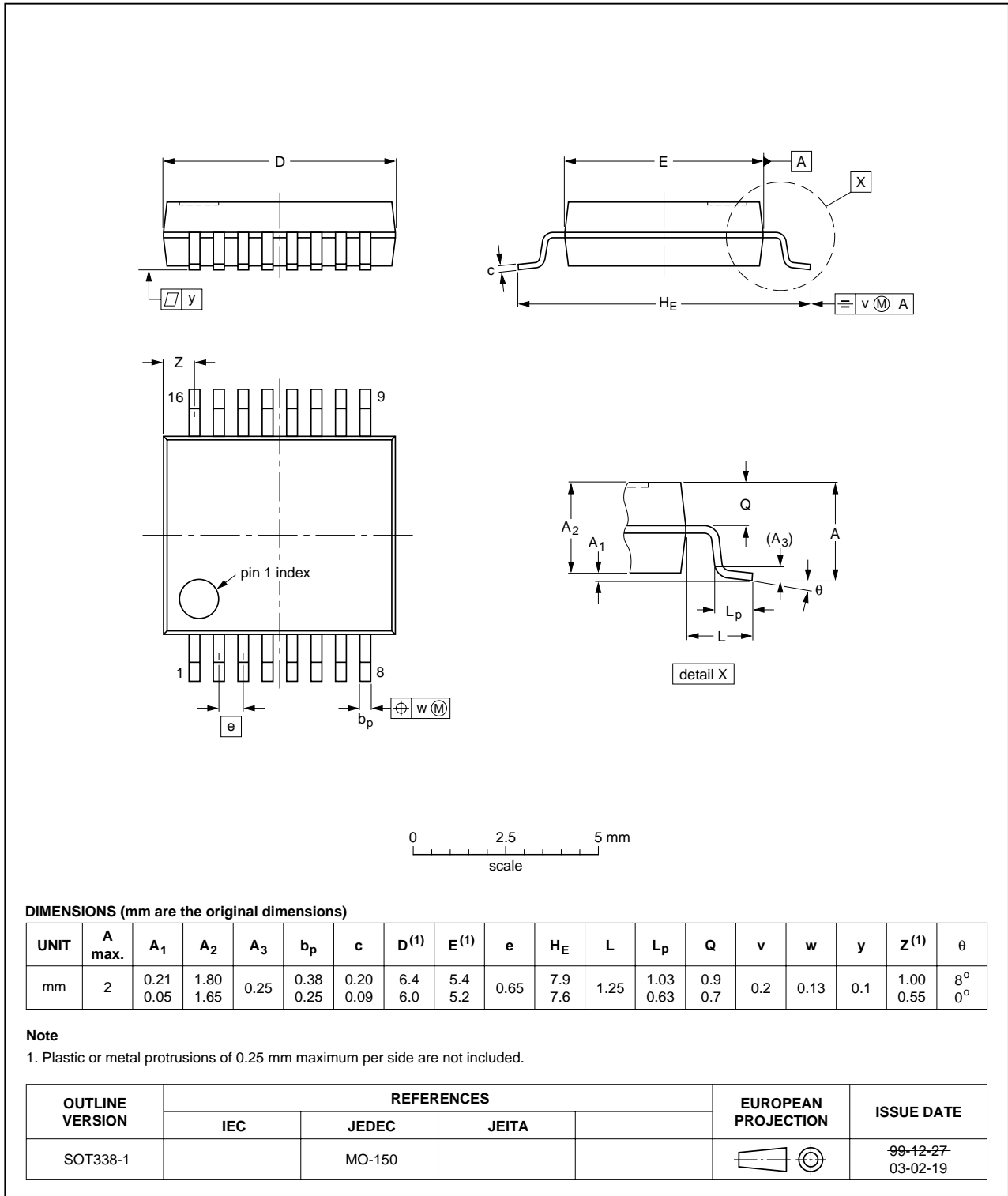


Fig 10. Package outline SOT338-1 (SSOP16)

SSOP16: plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm SOT519-1

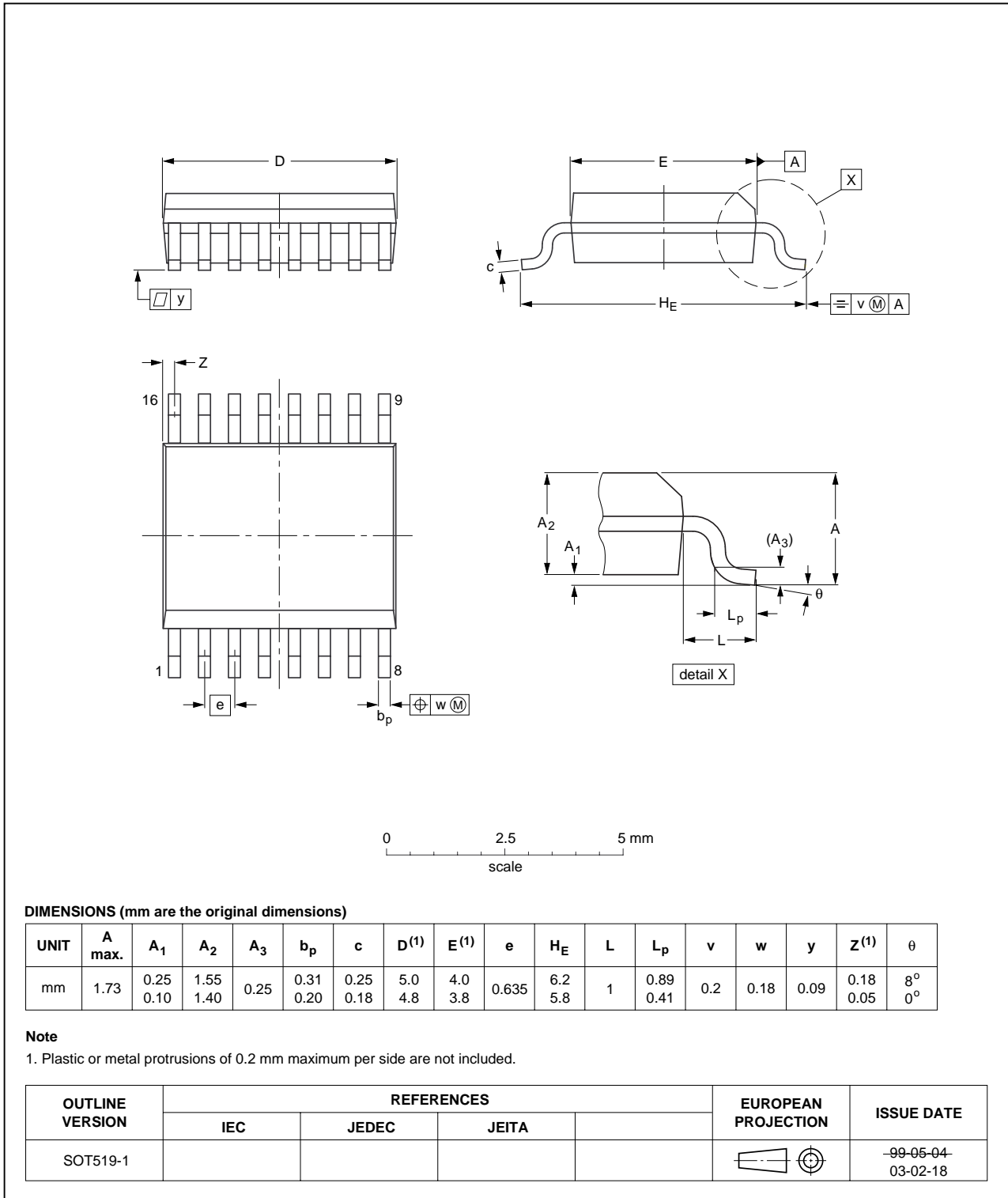


Fig 11. Package outline SOT519-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



Fig 12. Package outline SOT403-1 (TSSOP16)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
PRR	Pulse Rate Repetition
TTL	Transistor-Transistor Logic

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBT3257A_2	20070704	Product data sheet	-	CBT3257A_1
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 1: Topside marking changed for versions SOT338-1 and SOT403-1. • Soldering information removed. 			
CBT3257A_1	20051027	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

15.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or

malfunction of a NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For additional information, please visit: <http://www.nxp.com>

For sales office addresses, send an email to: salesaddresses@nxp.com

17. Contents

1 General description 1

2 Features 1

3 Ordering information 1

4 Functional diagram 2

5 Pinning information 3

5.1 Pinning 3

5.2 Pin description 3

6 Functional description 4

6.1 Function table 4

7 Limiting values 4

8 Recommended operating conditions 4

9 Static characteristics 5

10 Dynamic characteristics 5

10.1 AC waveforms 6

11 Test information 7

12 Package outline 8

13 Abbreviations 12

14 Revision history 12

15 Legal information 13

15.1 Data sheet status 13

15.2 Definitions 13

15.3 Disclaimers 13

15.4 Trademarks 13

16 Contact information 13

17 Contents 14

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



© NXP B.V. 2007.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 4 July 2007

Document identifier: CBT3257A_2