FAIRCHILD SEMICONDUCTOR™

August 1986
Revised February 2000

DM9334
8-Bit Addressable Latch

General Description

The DM9334 is a high speed 8-bit Addressable Latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and being a one-of-eight decoder and demultiplexer with active level HIGH outputs. The device also incorporates an active level LOW common clear for resetting all latches, as well as an active level LOW enable.

The DM9334 has four modes of operation which are shown in the mode selection table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the data or address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other inputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs.

When operating the device as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

The function tables summarize the operation of the product.

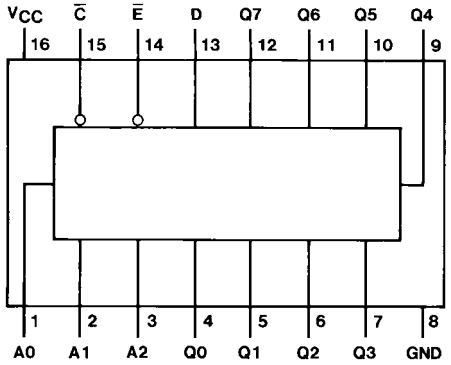
Features

- Common clear
- Easily expandable
- Random (addressable) data entry
- Serial to parallel capability
- 8 bits of storage/output of each bit available
- Active high demultiplexing/decoding capability

Ordering Code:

Order Number	Package Number	Package Description
DM9334N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Connection Diagram



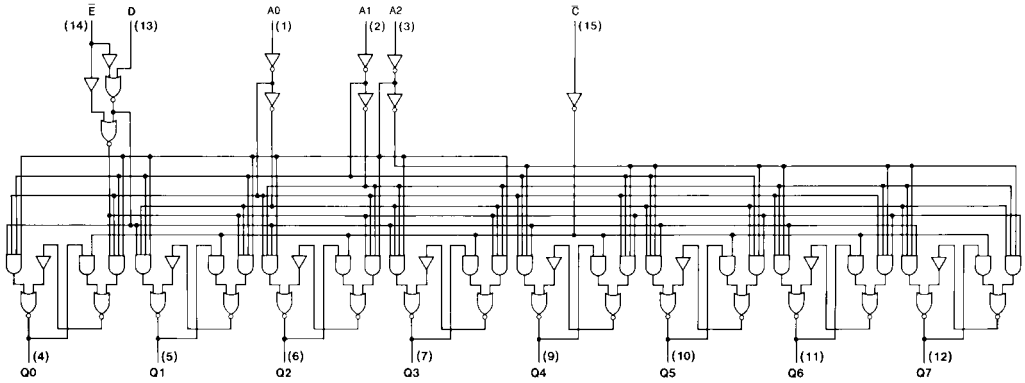
Function Tables

$\overline{E}$	$\overline{C}$	Mode
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH Eight Channel Demultiplexer
H	L	Clear

Inputs						Present Output States								Mode
$\overline{C}$	$\overline{E}$	D	A0	A1	A2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	
L	H	X	X	X	X	L	L	L	L	L	L	L	L	Clear
L	L	L	L	L	L	L	L	L	L	L	L	L	L	Demultiplex
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	L	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
•	•	•		•					•					
•	•	•		•					•					
•	•	•		•					•					
L	L	H	H	H	H	L	L	L	L	L	L	L	H	
H	H	X	X	X	X	Q_{N-1}								Memory
H	L	L	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1}					Addressable Latch
H	L	H	L	L	L	H	Q_{N-1}	Q_{N-1}						
H	L	L	H	L	L	Q_{N-1}	L	Q_{N-1}						
H	L	H	H	L	L	Q_{N-1}	H	Q_{N-1}						
•	•	•		•				•						
•	•	•		•				•						
•	•	•		•				•						
H	L	L	H	H	H	Q_{N-1}						Q_{N-1}	L	
H	L	H	H	H	H	Q_{N-1}						Q_{N-1}	H	

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care Condition
Q_{N-1} = Previous Output State

Logic Diagram



Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0° to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage		2			V
V_{IL}	LOW Level Input Voltage				0.8	V
I_{OH}	HIGH Level Output Current				−0.8	mA
I_{OL}	LOW Level Output Current				16	mA
t_W	ENABLE Pulse Width (Figure 1) (Note 3)		19	13		ns
t_{SU}	Setup Time (Note 3)	Data 1 (Figure 5)	20	13		ns
		Data 0 (Figure 5)	20	14		
		Address (Figure 6) (Note 2)	10	5		
t_H	Hold Time (Note 3)	Data 1 (Figure 5)	0	−10		ns
		Data 0 (Figure 5)	0	−13		
T_A	Free Air Operating Temperature		0		70	°C

Note 2: The ADDRESS setup time is the time before the negative ENABLE transition that the ADDRESS must be stable so that the correct latch is addressed without affecting the other latches.

Note 3: $T_A = 25°C$ and $V_{CC} = 5V$.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.6		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max V_I = 2.4V	$\overline{E}$ Input			60	µA
			Others			40	
I_{IL}	LOW Level Input Current	V_{CC} = Max V_I = 0.4V	$\overline{E}$ Input			−2.4	mA
			Others			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)		−30		−100	mA
I_{CC}	Supply Current	V_{CC} = Max			56	86	mA

Note 4: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

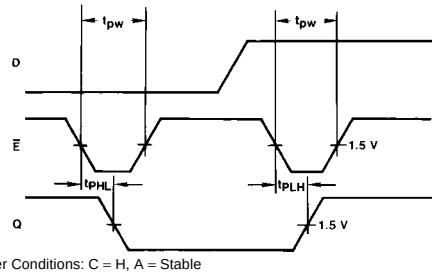
Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

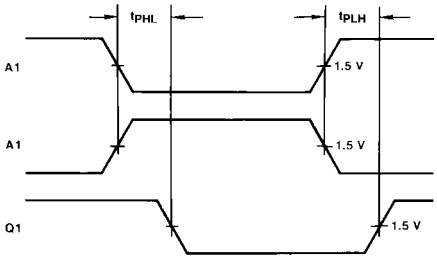
Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Enable to Output, (Figure 1)		28	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Enable to Output, (Figure 1)		27	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Data to Output, (Figure 4)		35	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Data to Output, (Figure 4)		28	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Address to Output, (Figure 2)		35	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Address to Output, (Figure 2)		35	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Output, (Figure 3)		31	ns

Switching Time Waveforms



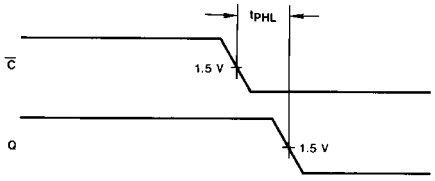
Other Conditions: C = H, A = Stable

FIGURE 1.



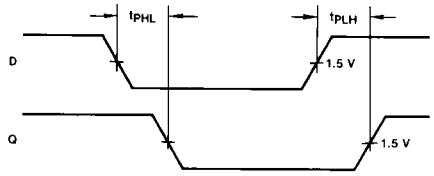
Other Conditions: $\overline{E}$ = L, $\overline{C}$ = L, D = H

FIGURE 2.



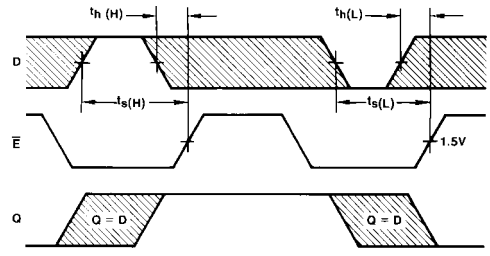
Other Conditions: $\overline{E}$ = H

FIGURE 3.



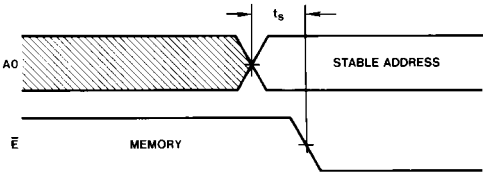
Other Conditions: $\overline{E}$ = L, $\overline{C}$ = H, A = Stable

FIGURE 4.



Other Conditions: C = H, A = Stable

FIGURE 5.

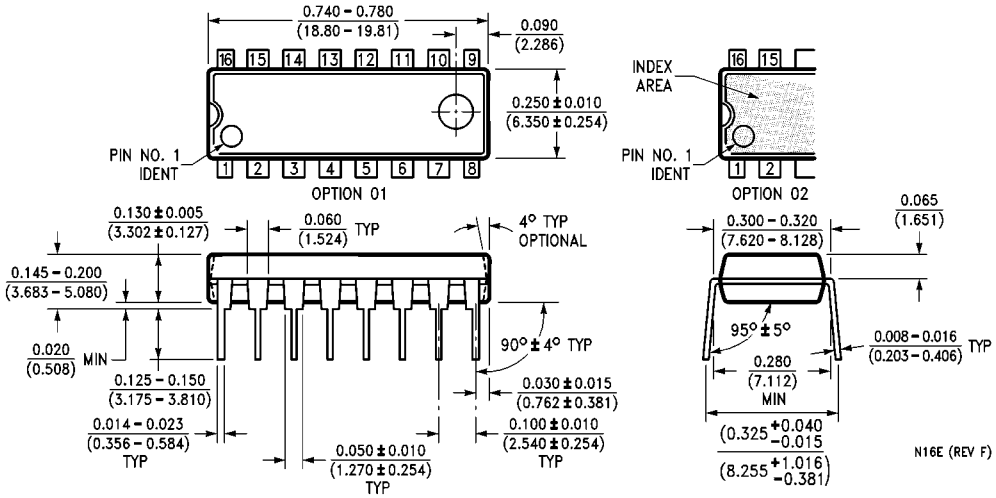


Other Conditions: $\overline{C}$ = H

Note: The shaded areas indicate when the inputs are permitted to change for predictable output performance.

FIGURE 6.

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com