National Semiconductor

February 1995

LM6313 High Speed, High Power Operational Amplifier

General Description

The LM6313 is a high-speed, high-power operational amplifier. This operational amplifier features a 35 MHz small signal bandwidth, and 250 V/μs slew rate. A compensation pin is included for adjusting the open loop bandwidth. The input stage (A1) and output stage (A2) are pinned out separately, and can be used independently. The operational amplifier is designed for low impedance loads and will deliver ±300 mA. The LM6313 has both overcurrent and thermal shutdown protection with an error flag to signal both these fault conditions.

These amplifiers are built with National's VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

Features

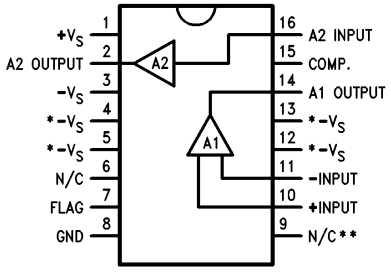
- High slew rate 250 V/μs
- Wide bandwidth 35 MHz
- Peak output current ±300 mA
- Input and output stages pinned out separately
- Single or dual supply operation
- Thermal protection
- Error flag warns of faults
- Wide supply voltage range ±5V to ±15V

Applications

- High speed ATE pin driver
- Data acquisition
- Driving capacitive loads
- Flash A-D input driver
- Precision 50Ω–75Ω video line driver
- Laser diode driver

Connection Diagram

Dual-In-Line Package



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Top View

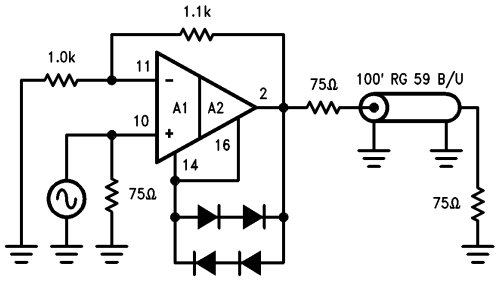
Order Number LM6313N
See NS Package Number N16A

*Heat sink pins

See Note 5 and Applications.

**Do not ground or otherwise connect to this pin.

Typical Application



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Absolute Maximum Ratings (Note 1)

Total Supply Voltage ($+V_S$ to $-V_S$)	36V (±18)
A1 Differential Input Voltage (Note 2)	±7V
A1 Input Voltage	(V^+ −0.7) to (V^- −7V)
A2 Input to Output Voltage	±7V
A2 Input Voltage	$\pm V_S$
Flag Output Voltage	GND to $+V_S$
Short-Circuit to Ground	(Note 3)
Storage Temperature Range	$-65°C \le T \le +150°C$
Lead Temperature (Soldering, 5 seconds)	260°C
ESD Tolerance (Note 4)	
Pins 10 and 11	±600V
All Other Pins	±1500V
Operating Temperature Range	
LM6313N	0°C to 70°C
Thermal Derating Information (Note 5)	
θ_{JA}	40°C/W
T_J (Max)	125°C

Operational Amplifier DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = 25°C$, and Supply Voltage $V_S = \pm 15V$. **Boldface** limits apply at temperature extremes. $V_{CM} = 0V$, $R_S = 50\Omega$, the circuit configured as in *Figure 1*.

Symbol	Parameter	Conditions	Typical	25°C Limit	0°C to 70°C Limit	Units
V_{OS}	Input Offset Voltage		5	20	**22**	mV (Max)
$\Delta V_{OS}/\Delta T$	Average Input Offset Voltage Drift		10			µV/°C
I_b	Input Bias Current		2	5	**7**	µA (Max)
I_{OS}	Input Offset Current		0.15	1.5	**1.9**	µA (Max)
$\Delta I_{OS}/\Delta T$	Average Input Offset Current Drift		0.4			nA/°C
R_{IN}	Input Resistance	Differential	325			kΩ
C_{IN}	Input Capacitance	$A_V = +1$, f = 10 MHz	2.2			pF
V_{CM}	Common-Mode Voltage Range		+14.2 −13.2	+13.8 −12.8	**+13.7** **−12.7**	V (Min)
A_{V1} A_{V2}	Voltage Gain 1 Voltage Gain 2	$R_L = 1 k\Omega$, $V_O = \pm 10V$ $R_L = 50\Omega$, $V_O = \pm 8V$	6000 5000	2500 2000	**2000** **1500**	V/V (Min)
CMRR	Common-Mode Rejection Ratio	$-10V \le V_{CM} \le +10V$	90	72	**70**	dB (Min)
PSRR	Power Supply Rejection Ratio	$\pm 5V \le V_S \le \pm 16V$	90	72	**70**	dB (Min)
V_{O1} V_{O2} V_{O3}	Output Voltage Swing 1 Output Voltage Swing 2 Output Voltage Swing 3	$R_L = 1 k\Omega$ $R_L = 100\Omega$ $R_L = 50\Omega$	13.1 12.0 11.0	11.8 10.5 9.0	**11.2** **10.0** **8.5**	±V (Min)
I_S	Supply Current	$T_J = 0°C$ $T_J = 25°C$ $T_J = 125°C$	18	23	**24** **21**	mA (Max)
I_{SC}	Peak Short-Circuit Output	(See *Figure 3*)	300			mA

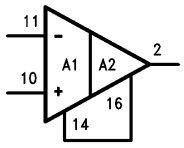

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FIGURE 1

Electrical Characteristics (Continued)

Operational Amplifier AC Electrical Characteristics Unless otherwise specified, all limits guaranteed for T_A = 25°C, and Supply Voltage V_S = ±15V. **Boldface** limits apply at temperature extremes. V_{CM} = 0V, R_S = 50Ω, the circuit configured as in *Figure 1*.

Symbol	Parameter	Conditions	Typical	Units
GBW	Gain-Bandwidth Product	@ f = 30 MHz	35	MHz
SR	Slew Rate	A_V = −1, R_L = 50Ω (Note 6)	250	V/μs
PBW	Power Bandwidth	V_{OUT} = 20 V_{PP}	3.0	MHz
t_S	Settling Time	10V Step to 0.1% (See *Figure 2*)	200	ns
	Phase Margin	A_V = −1, R_L = 1 kΩ, C_L = 50 pF	53	Deg
	Differential Gain		0.1	%
	Differential Phase		0.1	Deg
e_n	Input Noise Voltage	f = 10 kHz	14	nV/√ Hz
i_n	Input Noise Current	f = 10 kHz	1.8	pA/√ Hz

A1 DC Electrical Characteristics Unless otherwise specified, all limits guaranteed for T_A = 25°C, and Supply Voltage V_S = ±15V. **Boldface** limits apply at temperature extremes. V_{CM} = 0V, R_S = 50Ω.

Symbol	Parameter	Conditions	Typical	25°C Limit	0°C to 70°C Limit	Units
A_{VOL}	Large Signal Voltage Gain	V_{OUT} = ±10V, R_L = 2 kΩ V_{OUT} = ±10V, R_L = ∞	650 6000	300 2500	**250** **2000**	V/V (Min)
CMRR	Common-Mode Rejection Ratio	−10V ≤ V_{CM} ≤ +10V	90	72	**70**	dB (Min)
PSRR	Power Supply Rejection Ratio	±5V ≤ ±V_S ≤ +16V	90	72	**70**	dB (Min)
I_{SC}	Output Short Circuit Current		±60	±30	±**25**	mA (Min)

A1 AC Electrical Characteristics Unless otherwise specified, all limits guaranteed for T_A = 25°C, and Supply Voltage V_S = ±15V. **Boldface** limits apply at temperature extremes. R_S = 50Ω.

Symbol	Parameter	Conditions	Typical	25°C Limit	Units
GBW	Gain-Bandwidth	f = 30 MHz	37	25	MHz (Min)
SR	Slew Rate	A_V = +1, R_L = 100 kΩ, ±4 V_{IN}, ±2 V_{OUT}	250	150	V/μs (Min)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test condition listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors. Degradation of the input parameters (especially V_{OS}, I_{OS}, and Noise) is proportional to the level of the externally limited breakdown current and the accumulated duration of the breakdown condition.

Note 3: Continuous short-circuit operation of A1 at elevated temperature can result in exceeding the maximum allowed junction temperature of 125°C. A2 contains current limit and thermal shutdown to protect against fault conditions. The device may be damaged by shorts to the supplies.

Note 4: Human body model, C = 100 pF, R_S = 1500Ω.

Electrical Characteristics (Continued)

A2 DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = 25°C$, and Supply Voltage $V_S = \pm 15V$. **Boldface** limits apply at temperature extremes. $R_S = 50\Omega$.

Symbol	Parameter	Conditions	Typical	25°C Limit	0°C to 70°C Limit	Units
A_{V1}	Voltage Gain 1	$R_L = 1\ k\Omega$, $V_{IN} = \pm 10V$	0.99	0.97	**0.95**	V/mV (Min)
A_{V2}	Voltage Gain 2	$R_L = 50\Omega$, $V_{IN} = \pm 10V$	0.9	0.85	**0.82**	V/V (Min)
V_{OS}	Offset Voltage	$R_L = 1\ k\Omega$	15	70	**100**	mV (Max)
I_b	Input Bias Current	$R_L = 1\ k\Omega$, $R_S = 10\ k\Omega$	1	6	**8**	μA (Max)
R_{IN}	Input Resistance	$R_L = 50\Omega$	5			MΩ
C_{IN}	Input Capacitance		3.5			pF
R_O	Output Resistance	$I_{OUT} = \pm 10$ mA	3.5	5.0	**8.0**	Ω (Min)
V_O	Voltage Output Swing	$R_L = 1\ k\Omega$ $R_L = 100\Omega$ $R_L = 50\Omega$	13.7 12.5 11.0	13.0 10.5 9.0	**12.7** **10.0** **8.5**	V (Min)
PSRR	Power Supply Rejection Ratio	$V_S = \pm 5V$ to $\pm 16V$	70	60	**50**	dB (Min)

A2 AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = 25°C$, and Supply Voltage $V_S = \pm 15V$. **Boldface** limits apply at temperature extremes. $R_S = 50\Omega$.

Symbol	Parameter	Conditions	Typical	25°C Limit	Units
SR 1 SR 2	Slew Rate 1 Slew Rate 2	$V_{IN} = \pm 11V$, $R_L = 1\ k\Omega$ $V_{IN} = \pm 11V$, $R_L = 50\Omega$ (Note 7)	1200 750	 550	V/μs (Min)
BW	−3 dB Bandwidth	$V_{IN} = \pm 100$ mVpp $R_L = 50\Omega$, $C_L \leq 10$ pF	65	30	MHz (Min)
t_r, t_f	Rise Time Fall Time	$R_L = 1\ k\Omega$, $C_L \leq 10$ pF $V_O = 100$ mVpp	8		ns
P_D	Propagation Delay	$R_L = 50\Omega$, $C_L \leq 10$ pF $V_O = 100$ mVpp	4		ns
	Overshoot	$R_L = 1\ k\Omega$, $C_L = 100$ pF $R_L = 50\Omega$, $C_L = 1000$ pF	13 21		%

Additional (A2) Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = 25°C$, and Supply Voltage $V_S = \pm 15V$. **Boldface** limits apply at temperature extremes.

Symbol	Parameter	Conditions	Typical	25°C Limit	0°C to 70°C Limit	Units
V_{OL}	Flag Pin Output Low Voltage	I_{SINK} Flag Pin = 500 μA	220	340	**400**	mV (Max)
I_{OH}	Flag Pin Output High Current	V_{OH} Flag Pin = 15V (Note 8)	0.01	10	**20**	μA (Max)

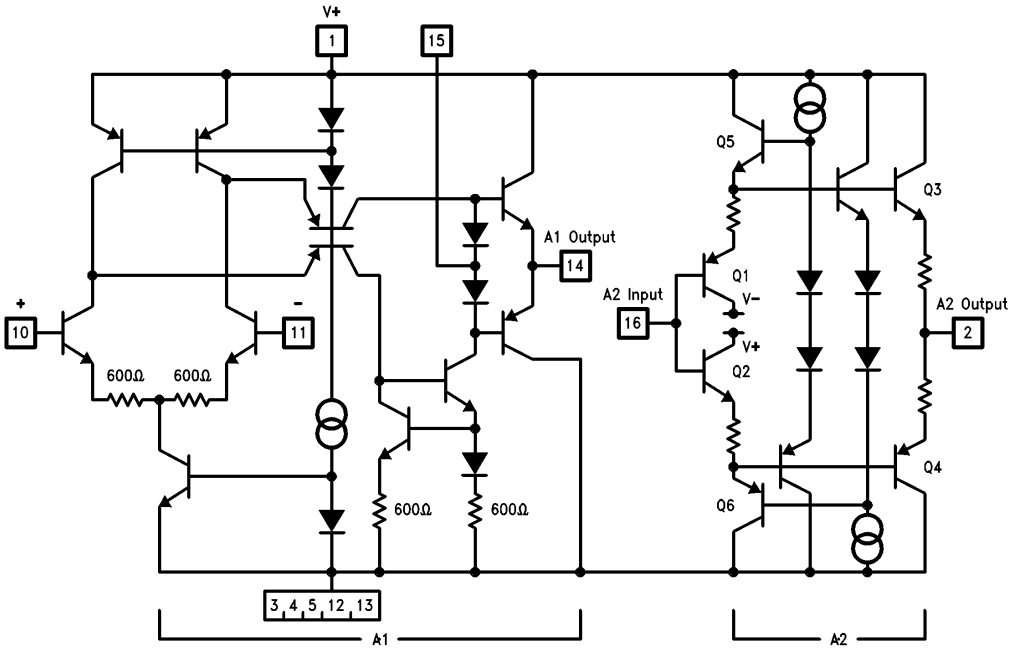
Note 5: For operation at elevated temperature, these devices must be derated to insure $T_J \leq 125°C$. $T_J = T_A + (P_D \times \theta_{JA})$. θ_{JA} for the N package mounted flush to the PCB, is 40°C/W when pins 4, 5, 12 and 13 are soldered to a total of 2 in^2 of copper trace.

Note 6: Measured between $\pm 5V$.

Note 7: $V_{IN} = \pm 9V$ step input, measured between $\pm 5V$ out.

Note 8: The error flag is set during current limit or thermal shut-down. The flag is an open collector, low on fault.

Simplified Schematic



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Settling Time Test Circuit

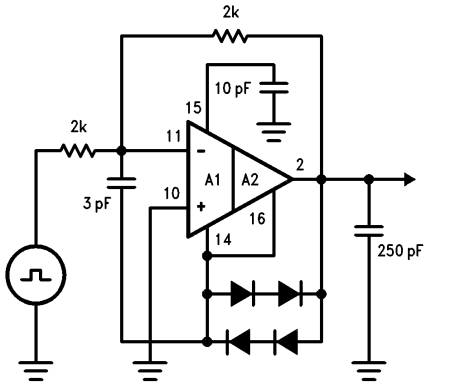

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FIGURE 2

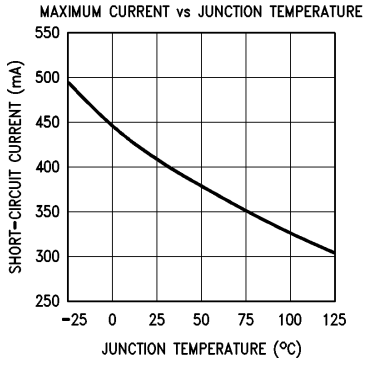

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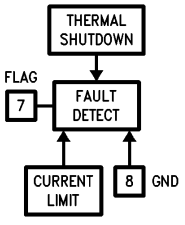
FIGURE 3

Protection Circuit Block Diagram



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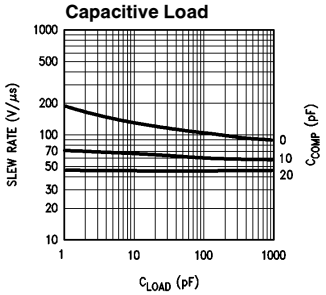
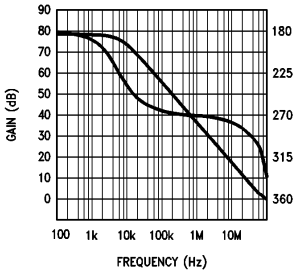
Typical Performance Characteristics Op Amp

(Unless otherwise specified, $T_A = 25°C$, $V_S = \pm 15V$, and $R_L = 10\ k\Omega$.)

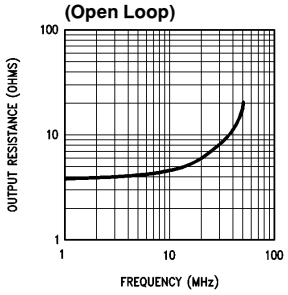
Slew Rate vs Capacitive Load



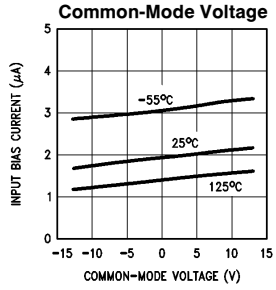
Bode Plot



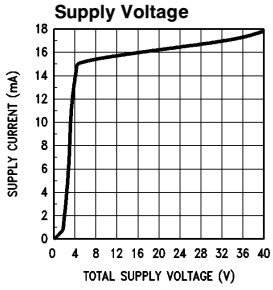
Output Resistance (Open Loop)



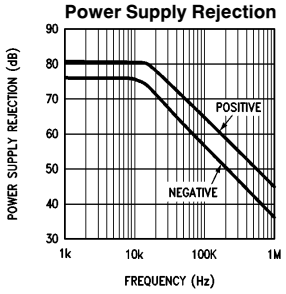
Bias Current vs Common-Mode Voltage



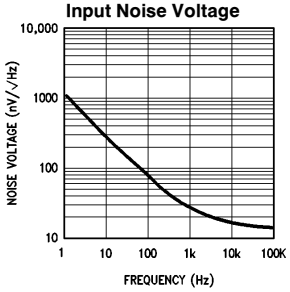
Supply Current vs Supply Voltage



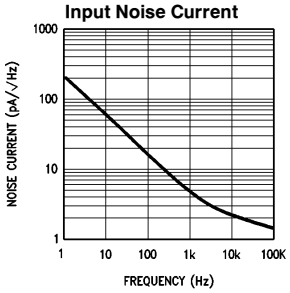
Power Supply Rejection



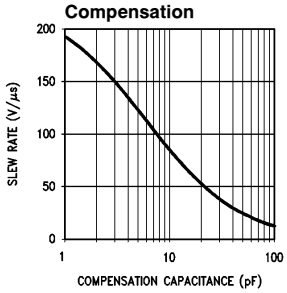
Input Noise Voltage



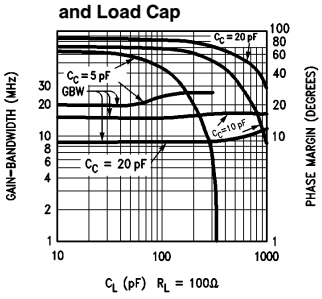
Input Noise Current



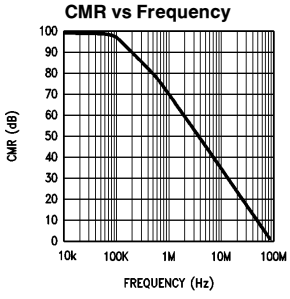
Slew Rate vs Compensation



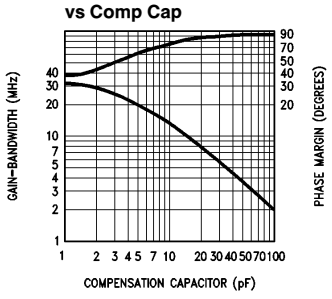
Gain-Bandwidth, Phase Margin vs Comp Cap and Load Cap



CMR vs Frequency



GBW and Phase Margin vs Comp Cap



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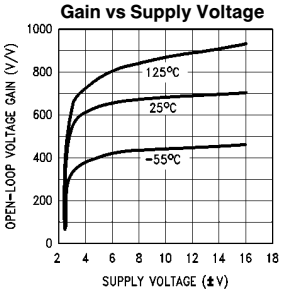
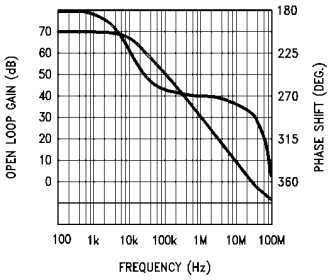
Typical Performance Characteristics A1 Only

(Unless otherwise specified, T_A = 25°C, V_S = ±15V, and R_L = 10 kΩ.)

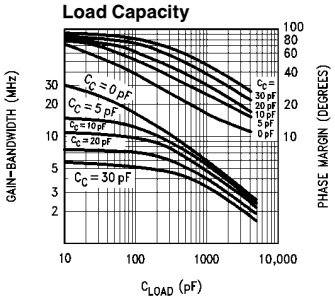
Gain vs Supply Voltage



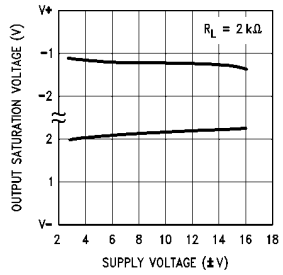
Bode Plot



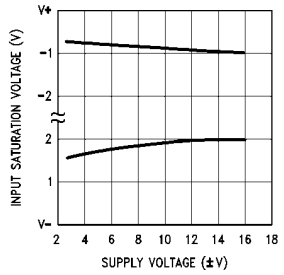
Gain-Bandwidth and Phase Margin vs Load Capacity



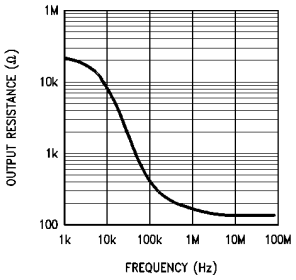
Output Saturation Voltage



Common-Mode Input Saturation Voltage



Output Resistance (Open Loop)



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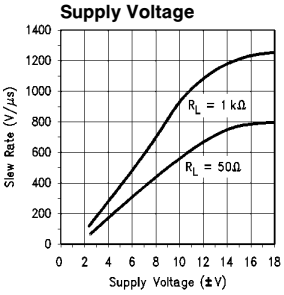
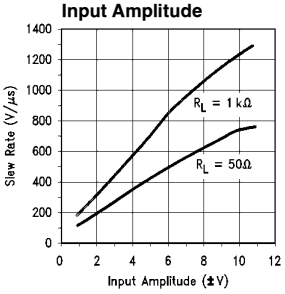
Typical Performance Characteristics A2 Only

(Unless otherwise specified, T_A = 25°C and V_S = ±15V.)

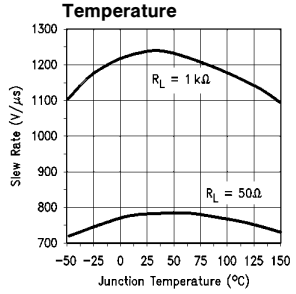
Slew Rate vs Supply Voltage



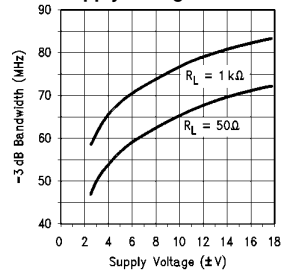
Slew Rate vs Input Amplitude



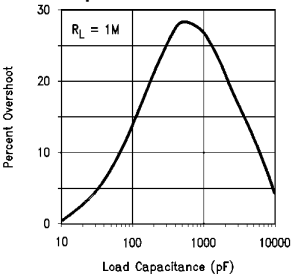
Slew Rate vs Temperature



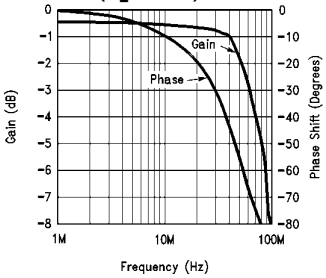
Bandwidth vs Supply Voltage



Overshoot vs Capacitive Load



Gain and Phase Shift (R_L = 50Ω)



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Application Hints

The LM6313 is a high-speed, high power operational amplifier that is designed for driving low-impedance loads such as 50Ω and 75Ω cables. Available in the standard, low cost, 16-pin DIP, this amplifier will drive back terminated video cables with up to 10 Vp-p. The ability to add additional compensation allows the LM6313 to drive capacitive loads of any size at bandwidths previously possible only with very expensive hybrid devices.

The LM6313 is excellent for driving high-speed flash A-to-D converters that require low-impedance drive at high frequencies. At 1 MHz, when used as a buffer, the LM6313 output impedance is below 0.1Ω. This very low output impedance also means that cables can be accurately back-terminated by just placing the characteristic impedance in series with the LM6313 output.

OVER-VOLTAGE PROTECTION

If the LM6313 is being operated on supply voltages of greater than ±5V, the possibility of damaging the output stage transistors exists. At higher supply voltages, if the output is shorted or excessive power dissipation causes the output stage to shut down, the maximum A2 input-to-output voltage, can be exceeded. This occurs when the input stage tries to drive the output while the output is at ground. To prevent this from happening, an easy solution is to place diodes around the output stage (See *Figure 4*). This will limit the maximum differential voltage to about 1.3V. Any signal diode, such as the 1N914 or the 1N4148 will work fine.

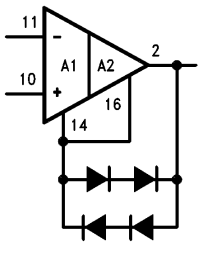

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FIGURE 4

HEAT SINKING

When driving a low impedance load such as 50Ω, and operating from ±15V supplies, the internal power dissipation of the LM6313 can rise above 3W. To prevent overheating of the chip, which would cause the thermal protection circuitry to shut the system down, the following guidelines should be followed:

1. Reduce the supply voltage. The LM6313 will operate with little change in performance, except output voltage swing, on ±5V supplies. This will reduce the dissipation to the level where no precautions against overheating are necessary for loads of 10Ω or more.
2. Solder pins 4, 5, 12 and 13 to copper traces which are at least 0.100 inch wide and have a total area of at least 2 square inches, to obtain a θ_{JA} of 40°C/W. These four pins are connected to the back of the chip and will be at V−. They should not be used as a V− connection unless pin 3 is also connected to this same point.

SUPPLY BYPASSING

Because of the large currents required to drive low-impedance loads, supply bypassing as close as possible to the I.C. is important. At 50 MHz, a few inches of wire or circuit trace can have 20Ω or 30Ω of inductive reactance. This inductance in series with a 0.1 μF bypass capacitor can resonate at 1 MHz to 2 MHz and just appear as an inductor at higher frequencies. A 0.1 μF and a 10μF to 15 μF capacitor connected in parallel and as close as possible to the LM6313 supply pins, from each supply to ground, will give best performance.

SELECTION OF COMPENSATION CAPACITOR

The compensation pin, pin 15, makes it possible to drive any load at any closed loop gain without stability problems. In most cases, where the gain is −1 or greater and the load is resistive, no compensation capacitor is required. When used at unity gain or when driving reactive loads, a small capacitor of 5 pF to 20 pF will insure optimum performance. The easiest way to determine the best value of compensation capacitor is to temporarily connect a trimmer capacitor (typical range of 2 pF to 15 pF) between pin 15, and ground, and adjust it for little or no overshoot at the output while driving the input with a square wave.

If the actual load capacitance is known, the typical graphs ''Gain-Bandwidth and Phase Margin vs. Load Capacitance'' can be used to select a value.

VIDEO CABLE DRIVER

The LM6313 is ideally suited for driving 50Ω or 75Ω cables. Unlike a buffer that requires a separate gain stage to make up for the losses involved in termination, the LM6313 gain can be set to 1 plus the line losses when the transmission line is end-terminated. If back-termination is needed, adding the line impedance in series with the output and raising the gain to 2 plus the expected line losses will provide a 0 dB loss system. *Figure 5* illustrates the back and end terminated video system including compensation for line losses. The excellent stability of the LM6313 with changes in supply voltages allow running the amplifier on unregulated supplies. The typical change in phase shift when the supplies are changed from ±5V to ±15V is less than 3° at 10 MHz.

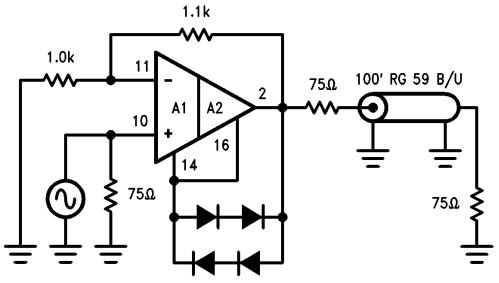

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FIGURE 5

Application Hints (Continued)

LASER DIODE MODULATOR

Figure 6 is a minimum component count example of a video modulator for a CW laser diode. This example biases the diode at 200 mA and modulates the current at ±200 mA per volt of signal. If it is desired to reduce power consumption and ±5V supplies are available, all that is necessary is to change R2 to 5 kΩ and R4 to 15Ω.

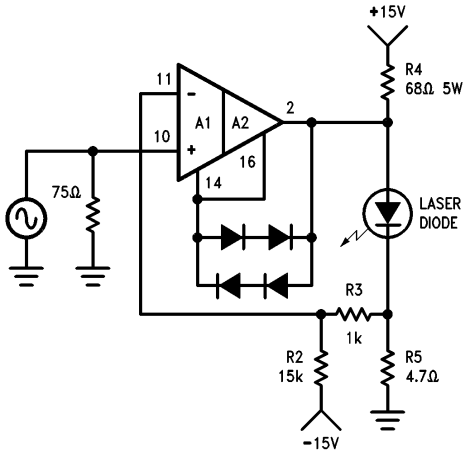

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FIGURE 6

In photo 1, C_L is 1000 pF. The LM6313 is slewing at 250 V/μs, from −5V to +5V. The slew rate is 450 V/μs from +5V to −5V. This requires the op amp to deliver 450 mA into the load and remain stable.

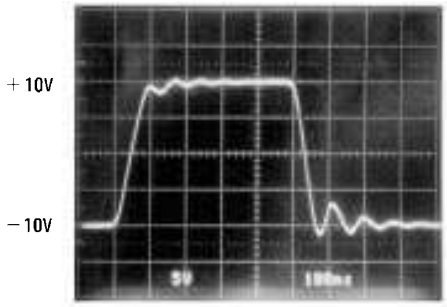

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Photo 1

CAPACITIVE LOAD DRIVING

Figure 7 is the circuit used to demonstrate the ability of the LM6313 to drive capacitive loads at speeds not previously possible with monolithic op amps.

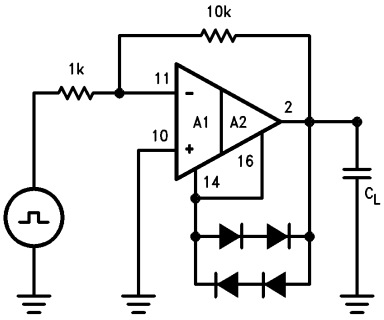

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FIGURE 7

In photo 2, C_L is changed to 1 μF. Under these conditions, the op amp is forced into current limiting. Here the current is internally limited to about ±400 mA. Note the rapid and complete recovery to normal operation at the end of slewing.

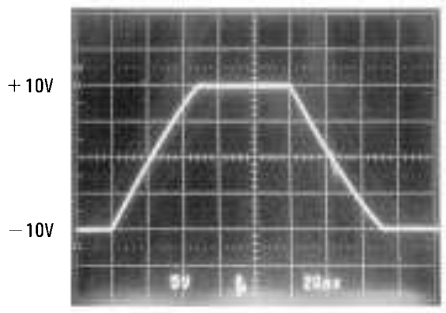

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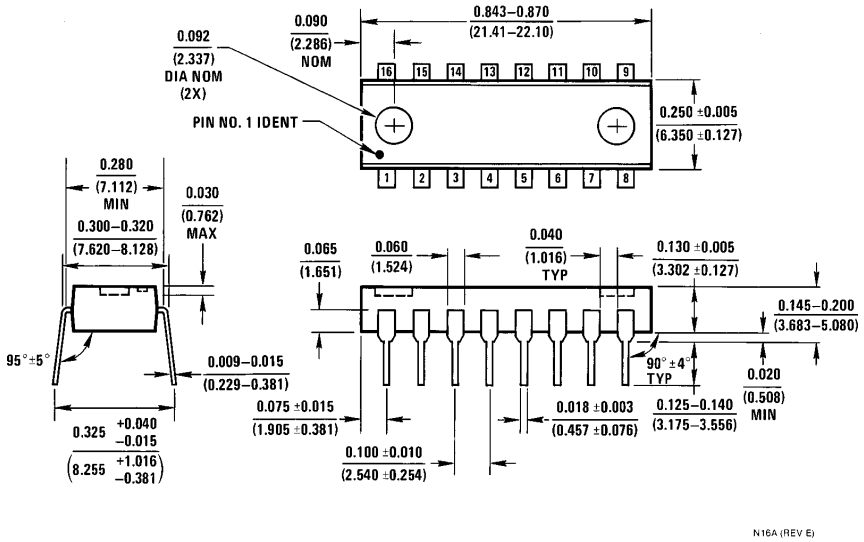
Photo 2

Physical Dimensions inches (millimeters)

Lit. # 108290



N16A (REV E)

16-Lead Molded Dual-In-Line Package (N)
Order Number LM6313N
NS Package Number N16A

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