Dual Inverter

The NLU2G04 is an advanced high-speed CMOS dual inverter in ultra-small footprint.

The NLU2G04 input and output structures provide protection when voltages up to 7.0 V are applied, irregardless of the supply voltage.

Features

- High Speed: $t_{PD} = 3.5 \text{ ns}$ (Typ) @ $V_{CC} = 5.0 \text{ V}$
- Low Power Dissipation: $I_{CC} = 1 \mu A (Max)$ at $T_A = 25^{\circ}C$
- Power Down Protection Provided on inputs
- Balanced Propagation Delays
- Overvoltage Tolerant (OVT) Input and Output Pins
- Ultra-Small Pb-Free Package
- This is a Pb-Free Device

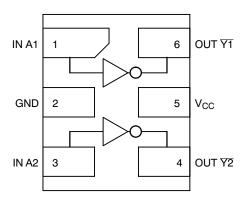


Figure 1. Pinout (Top View)

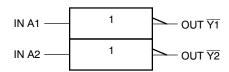


Figure 2. Logic Symbol



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MARKING DIAGRAM





UDFN6 MU SUFFIX CASE 517AA

U = Device Marking
M = Date Code
• Pb-Free Package

PIN ASSIGNMENT

IN A1
GND
IN A2
OUT Y2
V _{CC}
OUT Y1

FUNCTION TABLE

Α	7
L	H
H	L

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MAXIMUM RATINGS

Symbol	Paramete	Value	Unit	
V _{CC}	DC Supply Voltage		-0.5 to +7.0	V
V _{IN}	DC Input Voltage		-0.5 to +7.0	V
V _{OUT}	DC Output Voltage		-0.5 to +7.0	V
I _{IK}	DC Input Diode Current	V _{IN} < GND	-20	mA
lok	DC Output Diode Current	V _{OUT} < GND	±20	mA
Io	DC Output Source/Sink Current	±12.5	mA	
I _{CC}	DC Supply Current Per Supply Pin	±25	mA	
I _{GND}	DC Ground Current per Ground Pin	±25	mA	
T _{STG}	Storage Temperature Range	-65 to +150	°C	
T _L	Lead Temperature, 1 mm from Case for 10 Se	econds	TBD	°C
T_J	Junction Temperature Under Bias		TBD	°C
$\theta_{\sf JA}$	Thermal Resistance (Note 1)	UDFN6	TBD	°C/W
P_{D}	Power Dissipation in Still Air at 85°C	TBD	mW	
MSL	Moisture Sensitivity	Level 1		
F _R	Flammability Rating Oxygen	UL 94 V-0 @ 0.125 in		
I _{LATCHUP}	Latchup Performance Above V _{CC} and Below 0	±500	mA	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- 1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow.
- 2. Tested to EIA / JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Positive DC Supply Voltage	1.65	5.5	V
V _{IN}	Digital Input Voltage	0	5.5	V
V _{OUT}	Output Voltage	0	5.5	V
T _A	Operating Free-Air Temperature	-55	+125	°C
Δt/ΔV	Input Transition Rise or Fail Rate $ V_{CC} = 3.3 \ V \pm 0.3 \ V $ $ V_{CC} = 5.0 \ V \pm 0.5 \ V $	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

		V _{CC}		Т	T _A = 25 °C		T _A = -	+85°C		55°C to 25°C	
Symbol	Parameter	(V)	Conditions	Min	Тур	Max	Min	Max	Min	Max	Unit
V _{IH}	Low-Level Input Voltage	1.65		0.75 x V _{CC}			0.75 x V _{CC}				٧
		2.3 to 5.5		0.70 x V _{CC}			0.70 x V _{CC}				
V_{IL}	Low-Level Input Voltage	1.65				0.25 x V _{CC}		0.25 x V _{CC}		0.25 x V _{CC}	V
		2.3 to 5.5				0.30 x V _{CC}		0.30 x V _{CC}		0.30 x V _{CC}	
V _{OH}	High-Level Output Voltage	2.0 3.0 4.5	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -50 \mu A$	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
V _{OH}	High-Level Output Voltage	3.0 4.5	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -4 \text{ mA}$ $I_{OH} = -8 \text{ mA}$	2.58 3.94			2.48 3.80		2.34 3.66		V
V _{OL}	Low-Level Output Voltage	2.0 3.0 4.5	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 50 \mu\text{A}$		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		3.0 4.5	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$			0.36 0.36		0.44 0.44		0.52 0.52	
I _{IN}	Input Leakage Current	0 to 5.5	$0 \le V_{IN} \le 5.5 V$			±0.1		±1.0		±1.0	μА
I _{CC}	Quiescent Supply Current	5.5	$0 \le V_{IN} \le V_{CC}$			1.0		10		40	μΑ

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0 \text{ nS}$)

		V _{CC}	Test	т,	_A = 25 °	С	T _A = +	-85°C	T _A = -5 +12		
Symbol	Parameter	(V)	Condition	Min	Тур	Max	Min	Max	Min	Max	Unit
t _{PLH} ,	Propagation Delay,	3.0 to	C _L = 15 pF		4.5	7.1		8.5		10.0	ns
t _{PHL}	Input A to Output ₹	3.6	C _L = 50 pF		6.4	10.6		12.0		14.5	
		4.5 to	C _L = 15 pF		3.5	5.5		6.5		8.0	
		5.5	C _L = 50 pF		4.5	7.5		8.5		10.0	
C _{IN}	Input Capacitance				4	10		10		10.0	pF
C _{PD}	Power Dissipation Capacitance (Note 3)	5.0			8.0						pF

^{3.} C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption: P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

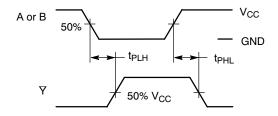
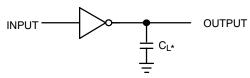


Figure 3. Switching Waveforms



*Includes all probe and jig capacitance.

A 1- MHz square input wave is recommended for propagation delay tests.

Figure 4. Test Circuit

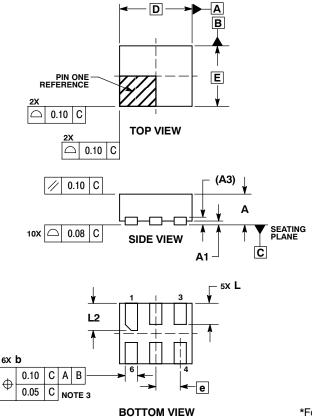
ORDERING INFORMATION

Device	Package	Shipping [†]
NLU2G04MUTCG	UDFN6 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

UDFN6, 1.2x1.0, 0.4P CASE 517AA-01 **ISSUE B**

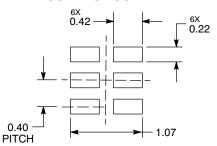


NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- ASME 114.5M, 1994. CONTROLLING DIMENSION: MILLIMETERS. DIMENSION & APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND
- 0.30 mm FROM TERMINAL. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS						
DIM	MIN MA						
Α	0.45	0.55					
A1	0.00	0.05					
А3	0.127 REF						
b	0.15	0.25					
D	1.20 BSC						
E	1.00 BSC						
е	0.40 BSC						
L	0.30	0.40					
12	0.40 0.50						

MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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