

NL27WZ06

Dual Inverter with Open Drain Outputs

The NL27WZ06 is a high performance dual inverter with open drain outputs operating from a 1.65 V to 5.5 V supply.

The internal circuit is composed of multiple stages, including an open drain output which provides the capability to set output switching level. This allows the NL27WZ06 to be used to interface 5 V circuits to circuits of any voltage between V_{CC} and 7 V using an external resistor and power supply.

Features

- Extremely High Speed: t_{PD} 2.4 ns (typical) at $V_{CC} = 5$ V
- Designed for 1.65 V to 5.5 V V_{CC} Operation
- Over Voltage Tolerant Inputs
- LVTTTL Compatible – Interface Capability With 5 V TTL Logic with $V_{CC} = 3$ V
- LVC MOS Compatible
- 24 mA Output Sink Capability
- Near Zero Static Supply Current Substantially Reduces System Power Requirements
- Chip Complexity: FET = 72; Equivalent Gate = 18
- Pb-Free Packages are Available

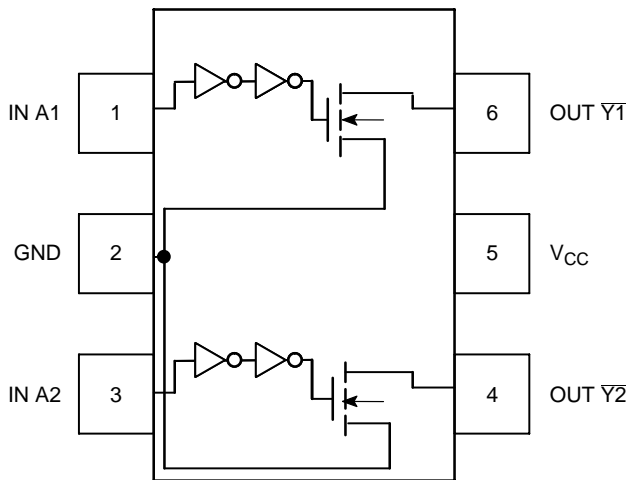


Figure 1. Pinout (Top View)

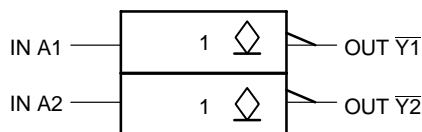


Figure 2. Logic Symbol



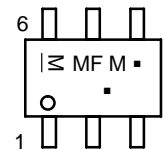
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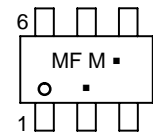
MARKING DIAGRAMS



SC-88
DF SUFFIX
CASE 419B



TSOP-6
DT SUFFIX
CASE 318G



MF = Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)
*Date Code orientation and/or position may vary depending upon manufacturing location.

PIN ASSIGNMENT

1	IN A1
2	GND
3	IN A2
4	OUT $\bar{Y}2$
5	V_{CC}
6	OUT $\bar{Y}1$

FUNCTION TABLE

A Input	\bar{Y} Output
L	Z
H	L

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NL27WZ06

MAXIMUM RATINGS

Symbol	Characteristics	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V
V _I	DC Input Voltage	-0.5 ≤ V _I ≤ +7.0	V
V _O	DC Output Voltage Output in Z or LOW State (Note 1)	-0.5 ≤ V _O ≤ 7.0	V
I _{IK}	DC Input Diode Current V _I < GND	-50	mA
I _{OK}	DC Output Diode Current V _O < GND	-50	mA
I _O	DC Output Sink Current	±50	mA
I _{CC}	DC Supply Current Per Supply Pin	±100	mA
I _{GND}	DC Ground Current Per Ground Pin	±100	mA
T _{STG}	Storage Temperature Range	-65 to +150	°C
P _D	Power Dissipation in Still Air SC-88, TSOP-6	200	mW
θ _{JA}	Thermal Resistance SC-88, TSOP-6	333	°C/W
T _L	Lead temperature, 1 mm from case for 10 s	260	°C
T _J	Junction temperature under bias	+150	°C
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A	V
I _{Latchup}	Latchup Performance Above V _{CC} and Below GND at 85°C (Note 5)	±500	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. I_O absolute maximum rating must be observed.
2. Tested to EIA/JESD22-A114-A
3. Tested to EIA/JESD22-A115-A
4. Tested to JESD22-C101-A
5. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage Operating Data Retention Only	1.65 1.5	5.5 5.5	V
V _I	Input Voltage	0	5.5	V
V _O	Output Voltage (Z or LOW State)	0	5.5	V
T _A	Operating Free-Air Temperature	-55	+125	°C
Δt/ΔV	Input Transition Rise or Fall Rate V _{CC} = 2.5 V ±0.2 V V _{CC} = 3.0 V ±0.3 V V _{CC} = 5.0 V ±0.5 V	0 0 0	20 10 5	ns/V

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	High-Level Input Voltage		1.65 2.3 to 5.5	0.75 V _{CC} 0.70 V _{CC}			0.75 V _{CC} 0.70 V _{CC}		V
V _{IL}	Low-Level Input Voltage		1.65 2.3 to 5.5			0.25 V _{CC} 0.30 V _{CC}		0.25 V _{CC} 0.30 V _{CC}	V
I _{LKG}	Z-State Output Leakage Current	V _{IN} = V _{IL} V _{OUT} = V _{CC} or GND	1.65 to 5.5			±5.0		±10.0	μA
V _{OL}	Low-Level Output Voltage V _{IN} = V _{IH}	I _{OL} = 100 μA	1.65 to 5.5		0.0	0.1		0.1	V
		I _{OL} = 3 mA	1.65		0.08	0.24			
		I _{OL} = 8 mA	2.3		0.22	0.3		0.3	
		I _{OL} = 12 mA	2.7		0.22	0.4		0.4	
		I _{OL} = 16 mA	3.0		0.28	0.4		0.4	
		I _{OL} = 24 mA	3.0		0.38	0.55		0.55	
		I _{OL} = 32 mA	4.5		0.42	0.55		0.55	
I _{IN}	Input Leakage Current	V _{IN} or V _{OUT} = V _{CC} or GND	0 to 5.5			±0.1		±1.0	μA
I _{OFF}	Power Off-Output Leakage Current	V _{OUT} = 5.5 V	0			1		10	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5			1		10	μA

AC ELECTRICAL CHARACTERISTICS t_R = t_F = 2.5 ns; C_L = 50 pF; R_L = 500 Ω

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
t _{PZL}	Propagation Delay (Figure 3 and 4)	R _L = R ₁ = 5000 Ω, C _L = 15 pF	1.8 ± 0.15	2.0	5.7	10.5	2.0	11.0	ns
		R _L = R ₁ = 500 Ω, C _L = 50 pF	2.5 ± 0.20	0.8	3.0	3.6	0.8	4.1	
		R _L = R ₁ = 500 Ω, C _L = 50 pF	3.3 ± 0.30	0.8	2.4	3.2	0.8	3.7	
		R _L = R ₁ = 500 Ω, C _L = 50 pF	5.0 ± 0.50	0.5	2.4	3.0	0.5	3.5	
t _{PLZ}	Propagation Delay (Figure 3 and 4)	R _L = R ₁ = 5000 Ω, C _L = 15 pF	1.8 ± 0.15	2.0	5.7	10.5	2.0	11.0	ns
		R _L = R ₁ = 500 Ω, C _L = 50 pF	2.5 ± 0.20	0.8	3.0	3.6	0.8	4.1	
		R _L = R ₁ = 500 Ω, C _L = 50 pF	3.3 ± 0.30	0.8	2.1	3.2	0.8	3.7	
		R _L = R ₁ = 500 Ω, C _L = 50 pF	5.0 ± 0.50	0.5	1.2	3.0	0.5	3.5	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C _{IN}	Input Capacitance	V _{CC} = 5.5 V, V _I = 0 V or V _{CC}	2.5	pF
C _{OUT}	Output Capacitance	V _{CC} = 5.5 V, V _I = 0 V or V _{CC}	4	pF
C _{PD}	Power Dissipation Capacitance (Note 6)	10 MHz, V _{CC} = 5.5 V, V _I = 0 V or V _{CC}	4	pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-55°C ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	High-Level Input Voltage		1.65 2.3 to 5.5	0.75 V _{CC} 0.70 V _{CC}			0.75 V _{CC} 0.70 V _{CC}		V
V _{IL}	Low-Level Input Voltage		1.65 2.3 to 5.5			0.25 V _{CC} 0.30 V _{CC}		0.25 V _{CC} 0.30 V _{CC}	V
I _{LKG}	Z-State Output Leakage Current	V _{IN} = V _{IL} V _{OUT} = V _{CC} or GND	1.65 to 5.5			±5.0		±10.0	μA
V _{OL}	Low-Level Output Voltage V _{IN} = V _{IH}	I _{OL} = 100 μA	1.65 to 5.5		0.0	0.1		0.1	V
		I _{OL} = 3 mA	1.65		0.08	0.24			
		I _{OL} = 8 mA	2.3		0.22	0.3		0.35	
		I _{OL} = 12 mA	2.7		0.22	0.4		0.45	
		I _{OL} = 16 mA	3.0		0.28	0.4		0.5	
		I _{OL} = 24 mA	3.0		0.38	0.55		0.65	
		I _{OL} = 32 mA	4.5		0.42	0.55		0.65	
I _{IN}	Input Leakage Current	V _{IN} or V _{OUT} = V _{CC} or GND	0 to 5.5			±0.1		±1.0	μA
I _{OFF}	Power Off-Output Leakage Current	V _{OUT} = 5.5 V	0			1		10	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5			1		10	μA

AC ELECTRICAL CHARACTERISTICS t_R = t_F = 2.5 ns; C_L = 50 pF; R_L = 500 Ω

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-55°C ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
t _{PZL}	Propagation Delay (Figure 3 and 4)	R _L = R ₁ = 5000 Ω, C _L = 15 pF	1.8 ± 0.15	2.0	5.7	10.5	2.0	11.0	ns
		R _L = R ₁ = 500 Ω, C _L = 50 pF	2.5 ± 0.20	0.8	3.0	3.6	0.8	4.1	
		R _L = R ₁ = 500 Ω, C _L = 50 pF	3.3 ± 0.30	0.8	2.4	3.2	0.8	3.7	
		R _L = R ₁ = 500 Ω, C _L = 50 pF	5.0 ± 0.50	0.5	2.4	3.0	0.5	3.5	
t _{PLZ}	Propagation Delay (Figure 3 and 4)	R _L = R ₁ = 5000 Ω, C _L = 15 pF	1.8 ± 0.15	2.0	5.7	10.5	2.0	11.0	ns
		R _L = R ₁ = 500 Ω, C _L = 50 pF	2.5 ± 0.20	0.8	3.8	4.5	0.8	5.0	
		R _L = R ₁ = 500 Ω, C _L = 50 pF	3.3 ± 0.30	0.8	2.9	3.2	0.8	3.7	
		R _L = R ₁ = 500 Ω, C _L = 50 pF	5.0 ± 0.50	0.5	1.2	3.0	0.5	3.5	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C _{IN}	Input Capacitance	V _{CC} = 5.5 V, V _I = 0 V or V _{CC}	2.5	pF
C _{OUT}	Output Capacitance	V _{CC} = 5.5 V, V _I = 0 V or V _{CC}	4	pF
C _{PD}	Power Dissipation Capacitance (Note 6)	10 MHz, V _{CC} = 5.5 V, V _I = 0 V or V _{CC}	4	pF

7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

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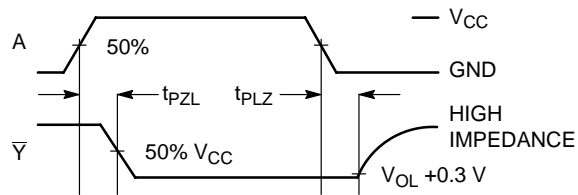


Figure 3. Switching Waveforms

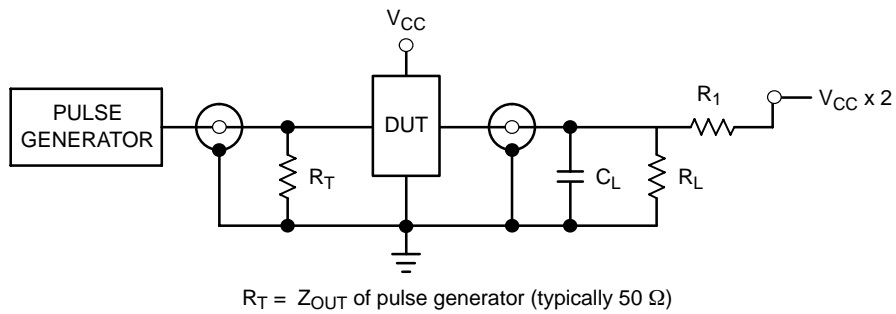


Figure 4. Test Circuit

ORDERING INFORMATION

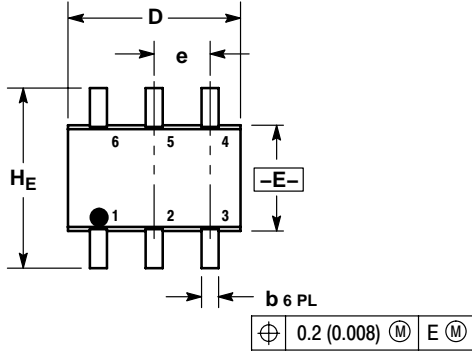
Device	Package	Shipping [†]
NL27WZ06DFT2	SC-88	3000 / Tape & Reel
NL27WZ06DFT2G	SC-88 (Pb-Free)	
NL27WZ06DTT1	TSOP-6	
NL27WZ06DTT1G	TSOP-6 (Pb-Free)	

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS

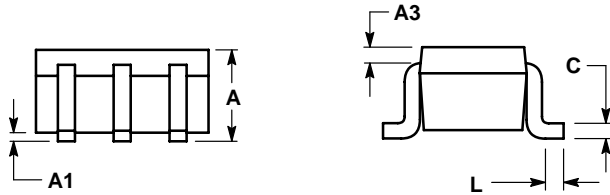
SC-88/SC70-6/SOT-363
CASE 419B-02
ISSUE W



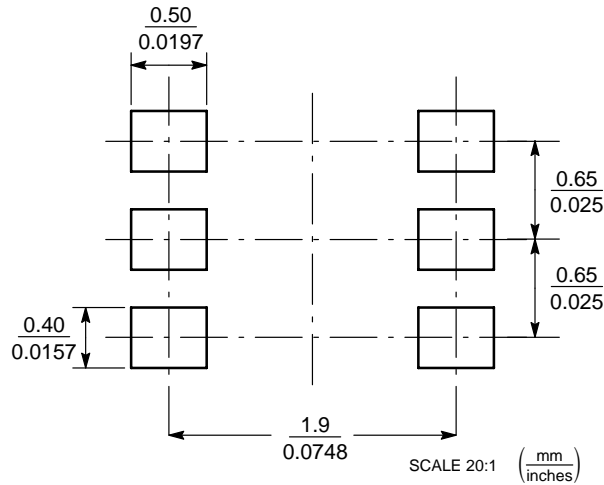
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419B-01 OBSOLETE, NEW STANDARD 419B-02.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.95	1.10	0.031	0.037	0.043
A1	0.00	0.05	0.10	0.000	0.002	0.004
A3	0.20 REF			0.008 REF		
b	0.10	0.21	0.30	0.004	0.008	0.012
C	0.10	0.14	0.25	0.004	0.005	0.010
D	1.80	2.00	2.20	0.070	0.078	0.086
E	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
HE	2.00	2.10	2.20	0.078	0.082	0.086



SOLDERING FOOTPRINT*

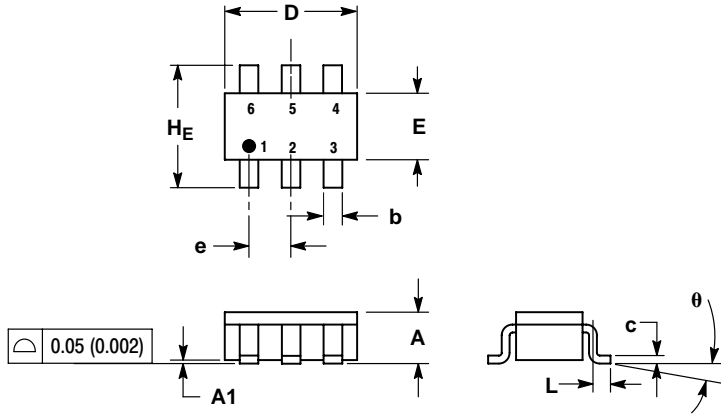


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

TSOP-6
CASE 318G-02
ISSUE S

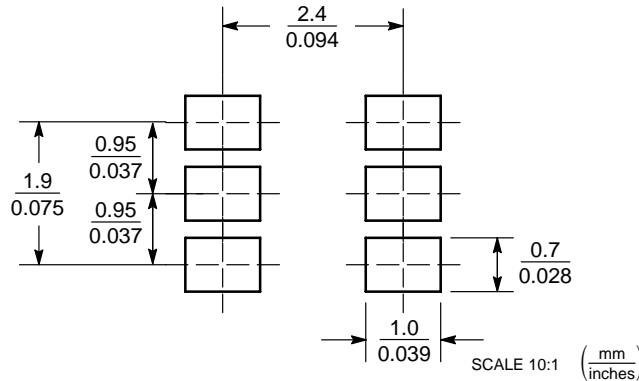


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.38	0.50	0.010	0.014	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
HE	2.50	2.75	3.00	0.099	0.108	0.118
theta	0°	-	10°	0°	-	10°

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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