

DATA SHEET

74AVC16835

18-bit registered driver (3-State)

Preliminary specification

1999 Jul 23

Replaces datasheet 74AVC16835/74AVCH16835 dated 1998 Dec 07

18-bit Registered Driver (3-State)

74AVC16835

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- Complies with JEDEC standard no. 8-1A/5/7.
- CMOS low power consumption
- Input/output tolerant up to 3.6 V
- DCO (Dynamic Controlled Output) circuit dynamically changes output impedance, resulting in noise reduction without speed degradation
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- Power off disables 74AVC16835 outputs, permitting Live Insertion

DESCRIPTION

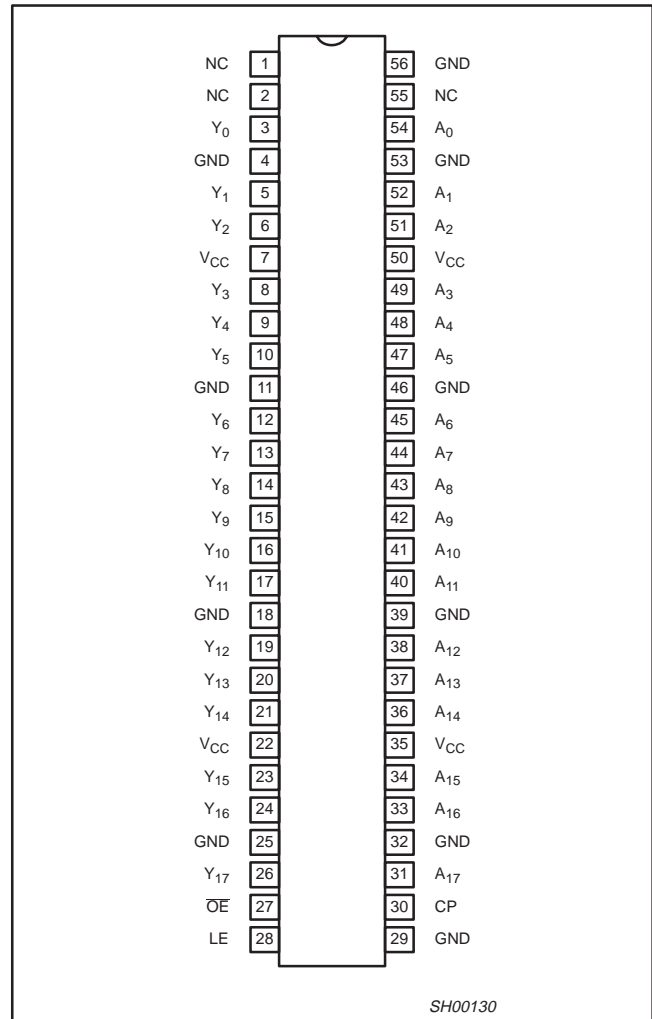
The 74AVC16835 is a 18-bit universal bus driver. Data flow is controlled by output enable (\overline{OE}), latch enable (LE) and clock inputs (CP).

This product is designed to have an extremely fast propagation delay and a minimum amount of power consumption.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor (Live Insertion).

A Dynamic Controlled Output (DCO) circuitry is implemented to support termination line drive during transient. See the graphs on page 8 for typical curves.

PIN CONFIGURATION



QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; t_r = t_f ≤ 2.0 ns; C_L = 30 pF.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT	
t _{PHL} /t _{PLH}	Propagation delay An to Yn	V _{CC} = 1.8 V V _{CC} = 2.5 V V _{CC} = 3.3 V	2.6 2.0 1.7	ns	
t _{PHL} /t _{PLH}	Propagation delay LE to Yn; CP to Yn	V _{CC} = 1.8 V V _{CC} = 2.5 V V _{CC} = 3.3 V	2.8 2.2 1.8	ns	
C _I	Input capacitance		5.0	pF	
C _{PD}	Power dissipation capacitance per buffer	V _I = GND to V _{CC} ¹	Outputs enabled Output disabled	25 6	pF

NOTES:

- C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; C_L = output load capacitance in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V; $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
56-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	-40°C to +85°C	74AVC16835 DGG	SOT364-1

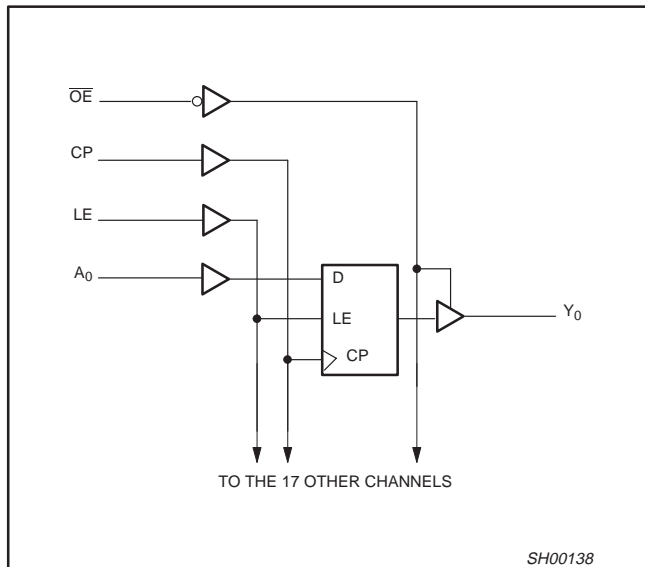
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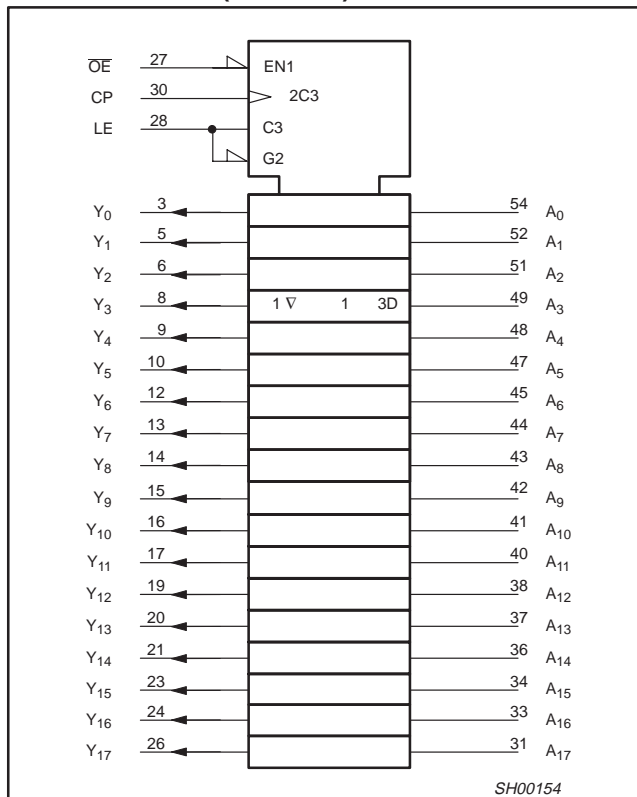
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 55	NC	No connection
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	Y ₀ to Y ₁₇	Data outputs
4, 11, 18, 25, 32, 39, 46, 53, 56	GND	Ground (0V)
7, 22, 35, 50	V _{CC}	Positive supply voltage
27	\overline{OE}	Output enable input (active LOW)
28	LE	Latch enable input (active HIGH)
30	CP	Clock input
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	A ₀ to A ₁₇	Data inputs

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS				OUTPUTS
\overline{OE}	LE	CP	A	
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	H	X	Y ₀ ¹
L	L	L	X	Y ₀ ²

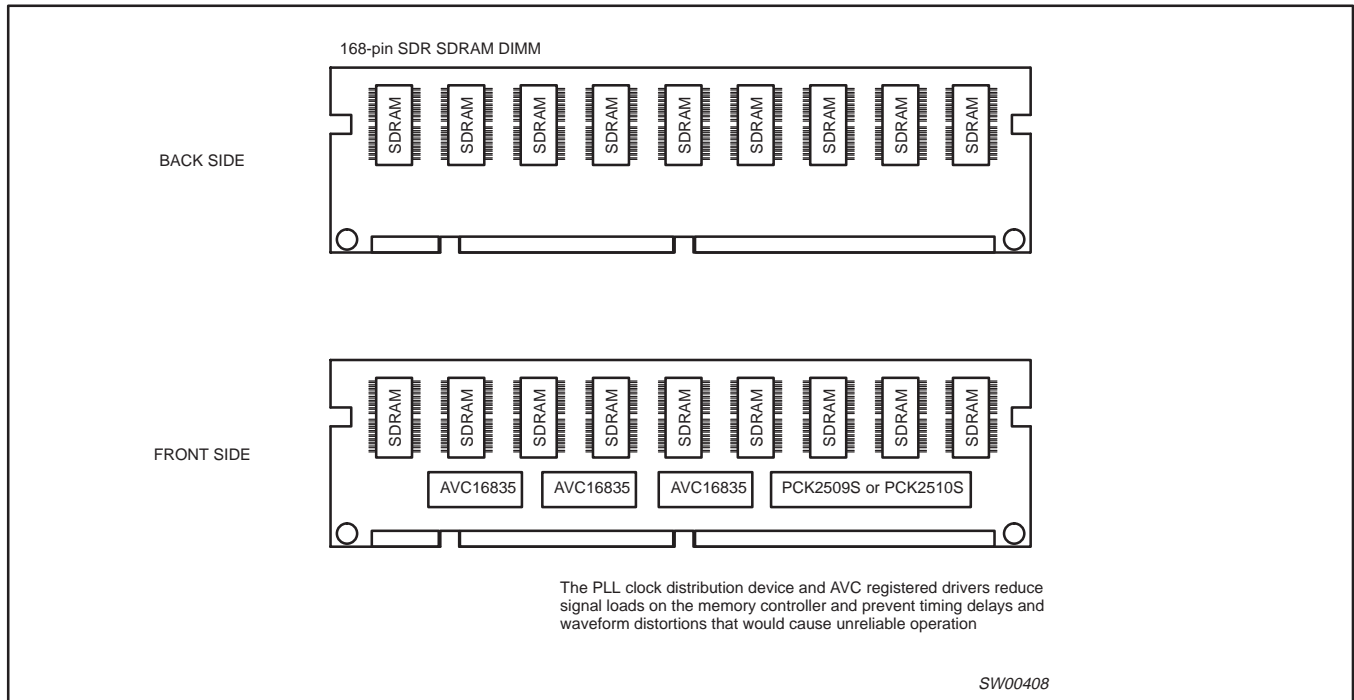
- H = HIGH voltage level
- L = LOW voltage level
- X = Don't care
- Z = High impedance "off" state
- ↑ = LOW-to-HIGH level transition

NOTES:

- Output level before the indicated steady-state input conditions were established, provided that CP is high before LE goes low.
- Output level before the indicated steady-state input conditions were established.

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V _{CC}	DC supply voltage (according to JEDEC Low Voltage Standards)		1.65 2.3 3.0	1.95 2.7 3.6	V
	DC supply voltage (for low voltage applications)		1.2	3.6	
V _I	DC Input voltage range		0	3.6	V
V _O	DC output voltage range; output 3-State		0	3.6	V
	DC output voltage range; output HIGH or LOW state		0	V _{CC}	
T _{amb}	Operating free-air temperature range		-40	+85	°C
t _r , t _f	Input rise and fall times	V _{CC} = 1.65 to 2.3 V V _{CC} = 2.3 to 3.0 V V _{CC} = 3.0 to 3.6 V	0 0 0	30 20 10	ns/V

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ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage	For all inputs ¹	-0.5 to 4.6	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage; output 3-State	Note 1	-0.5 to 4.6	V
V_O	DC output voltage; output HIGH or LOW state	Note 1	-0.5 to $V_{CC} + 0.5$	V
I_O	DC output source or sink current	$V_O = 0$ to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		-65 to +150	°C
P_{TOT}	Power dissipation per package -plastic thin-medium-shrink (TSSOP)	For temperature range: -40 to +125 °C above +55°C derate linearly with 8 mW/K	600	mW

NOTE:

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V_{IH}	HIGH level Input voltage	$V_{CC} = 1.2$ V	V_{CC}	-	-	V
		$V_{CC} = 1.65$ to 1.95 V	$0.65V_{CC}$	0.9	-	
		$V_{CC} = 2.3$ to 2.7 V	1.7	1.2	-	
		$V_{CC} = 3.0$ to 3.6 V	2.0	1.5	-	
V_{IL}	LOW level Input voltage	$V_{CC} = 1.2$ V	-	-	GND	V
		$V_{CC} = 1.65$ to 1.95 V	-	0.9	$0.35V_{CC}$	
		$V_{CC} = 2.3$ to 2.7 V	-	1.2	0.7	
		$V_{CC} = 3.0$ to 3.6 V	-	1.5	0.8	
V_{OH}	HIGH level output voltage	$V_{CC} = 1.65$ to 3.6 V; $V_I = V_{IH}$ or V_{IL} ; $I_O = -100$ μ A	$V_{CC} - 0.20$	V_{CC}	-	V
		$V_{CC} = 1.65$ V; $V_I = V_{IH}$ or V_{IL} ; $I_O = -4$ mA	$V_{CC} - 0.45$	$V_{CC} - 0.10$	-	
		$V_{CC} = 2.3$ V; $V_I = V_{IH}$ or V_{IL} ; $I_O = -8$ mA	$V_{CC} - 0.55$	$V_{CC} - 0.28$	-	
		$V_{CC} = 3.0$ V; $V_I = V_{IH}$ or V_{IL} ; $I_O = -12$ mA	$V_{CC} - 0.70$	$V_{CC} - 0.32$	-	
V_{OL}	LOW level output voltage	$V_{CC} = 1.65$ to 3.6 V; $V_I = V_{IH}$ or V_{IL} ; $I_O = 100$ μ A	-	GND	0.20	V
		$V_{CC} = 1.65$ V; $V_I = V_{IH}$ or V_{IL} ; $I_O = 4$ mA	-	0.10	0.45	
		$V_{CC} = 2.3$ V; $V_I = V_{IH}$ or V_{IL} ; $I_O = 8$ mA	-	0.26	0.55	
		$V_{CC} = 3.0$ V; $V_I = V_{IH}$ or V_{IL} ; $I_O = 12$ mA	-	0.36	0.70	
I_I	Input leakage current	$V_{CC} = 1.65$ to 3.6 V; $V_I = V_{CC}$ or GND	-	0.1	2.5	μ A
I_{OFF}	3-State output OFF-state current	$V_{CC} = 0$ V; V_I or $V_O = 3.6$ V	-	0.1	±10	μ A
I_{IHZ}/I_{ILZ}	3-State output OFF-state current	$V_{CC} = 1.65$ to 3.6 V; $V_I = V_{CC}$ or GND	-	0.1	12.5	μ A
I_{OZ}	3-State output OFF-state current	$V_{CC} = 1.65$ to 2.7 V; $V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND	-	0.1	5	μ A
		$V_{CC} = 3.0$ to 3.6 V; $V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND	-	0.1	10	
I_{CC}	Quiescent supply current	$V_{CC} = 1.65$ to 2.7 V; $V_I = V_{CC}$ or GND; $I_O = 0$	-	0.1	20	μ A
		$V_{CC} = 3.0$ to 3.6 V; $V_I = V_{CC}$ or GND; $I_O = 0$	-	0.2	40	

NOTES:1. All typical values are at $T_{amb} = 25^\circ\text{C}$.

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AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.0\text{ns}$; $C_L = 30\text{pF}$

SYMBOL	PARAMETER	WAVEFORM	LIMITS										UNIT
			$V_{CC} = 3.3 \pm 0.3\text{V}$			$V_{CC} = 2.5 \pm 0.2\text{V}$			$V_{CC} = 1.8 \pm 0.15\text{V}$			$V_{CC} = 1.2\text{V}$	
			MIN	TYP ¹	MAX	MIN	TYP ¹	MAX	MIN	TYP ¹	MAX	TYP	
t_{PHL}/t_{PLH}	Propagation delay An to Yn	1, 7	0.7	1.7	2.5	0.8	2.0	3.0	1.0	2.6	4.5	5.2	ns
	Propagation delay LE to Yn	2, 7	0.7	1.8	2.7	0.8	2.2	3.3	1.0	2.8	5.0	5.6	
	Propagation delay CP to Yn	3, 7	0.7	1.7	2.5	0.8	2.0	3.0	1.0	2.6	4.5	5.2	
t_{PZH}/t_{PZL}	3-State output enable time \overline{OE} to Yn	6, 7	1.0	2.3	4.0	1.0	2.5	4.5	1.5	3.0	6.5	5.5	ns
t_{PHZ}/t_{PLZ}	3-State output disable time \overline{OE} to Yn	6, 7	1.0	2.3	3.5	1.0	2.2	4.0	1.5	3.5	6.5	5.5	ns
t_w	CP pulse width HIGH or LOW	3, 7	1.0	-	-	1.2	-	-	2.0	-	-	-	ns
	LE pulse width HIGH	2, 7	1.0	-	-	1.2	-	-	2.0	-	-	-	
t_{SU}	Set-up time An to CP	5, 7	0.3	-	-	0.4	-	-	0.5	-	-	-	ns
	Set-up time An to LE	4, 7	0.3	-	-	0.4	-	-	0.5	-	-	-	
t_h	Hold time An to CP	5, 7	0.3	-	-	0.4	-	-	0.5	-	-	-	ns
	Hold time An to LE	4, 7	0.3	-	-	0.4	-	-	0.5	-	-	-	
F_{max}	Maximum clock pulse frequency	3, 7	500	-	-	400	-	-	250	-	-	-	MHz

NOTES:

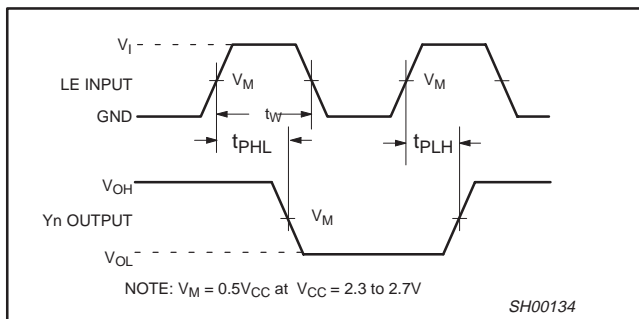
1. All typical values are measured at $T_{amb} = 25^\circ\text{C}$ and at $V_{CC} = 1.8\text{V}, 2.5\text{V}, 3.3\text{V}$.

AC WAVEFORMS FOR $V_{CC} = 3.0\text{V TO } 3.6\text{V RANGE}$

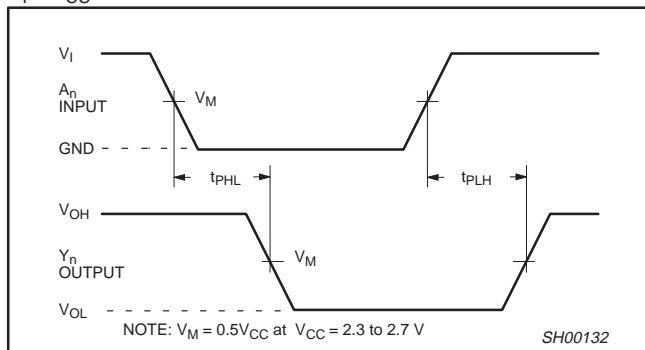
$V_M = 0.5 V_{CC}$
 $V_X = V_{OL} + 0.300\text{V}$
 $V_Y = V_{OH} - 0.300\text{V}$
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
 $V_I = V_{CC}$

AC WAVEFORMS FOR $V_{CC} = 2.3\text{V TO } 2.7\text{V AND } V_{CC} < 2.3\text{V RANGE}$

$V_M = 0.5 V_{CC}$
 $V_X = V_{OL} + 0.15\text{V}$
 $V_Y = V_{OH} - 0.15\text{V}$
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
 $V_I = V_{CC}$



Waveform 2. Latch enable input (LE) pulse width, the latch enable input to output (Yn) propagation delays.



Waveform 1. Input (An) to output (Yn) propagation delay

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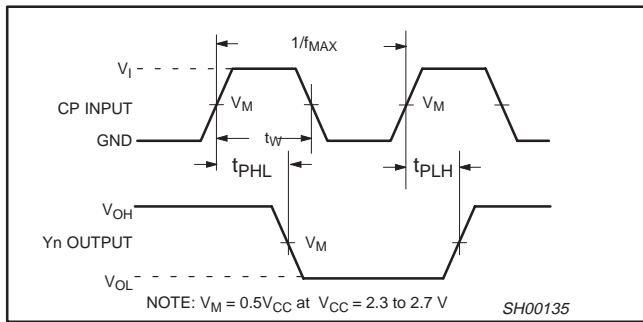
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AC WAVEFORMS FOR $V_{CC} = 3.0\text{ V TO }3.6\text{ V RANGE}$ (Continued)

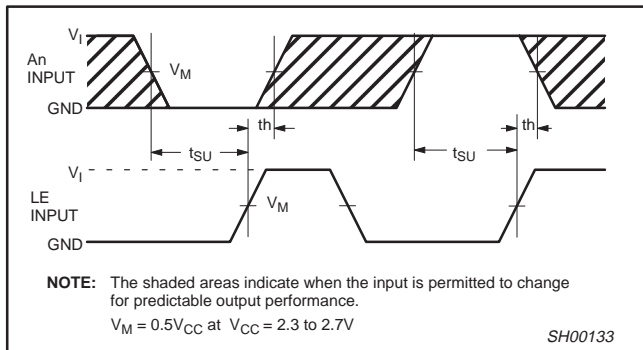
$V_M = 0.5 V_{CC}$
 $V_X = V_{OL} + 0.300\text{ V}$
 $V_Y = V_{OH} - 0.300\text{ V}$
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
 $V_I = V_{CC}$

AC WAVEFORMS FOR $V_{CC} = 2.3\text{ V TO }2.7\text{ V AND }V_{CC} < 2.3\text{ V RANGE}$ (Continued)

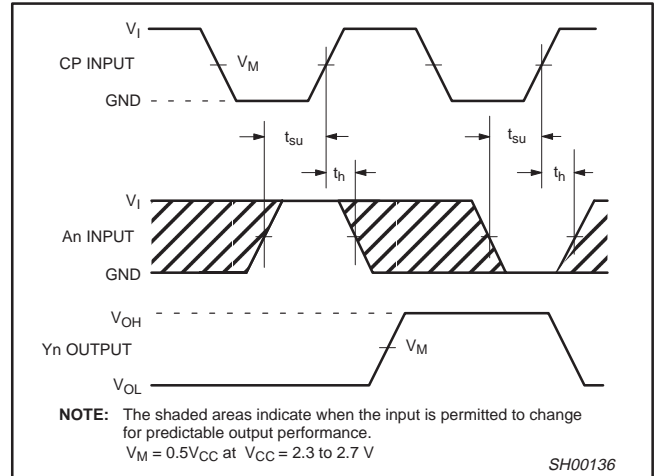
$V_M = 0.5 V_{CC}$
 $V_X = V_{OL} + 0.15\text{ V}$
 $V_Y = V_{OH} - 0.15\text{ V}$
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
 $V_I = V_{CC}$



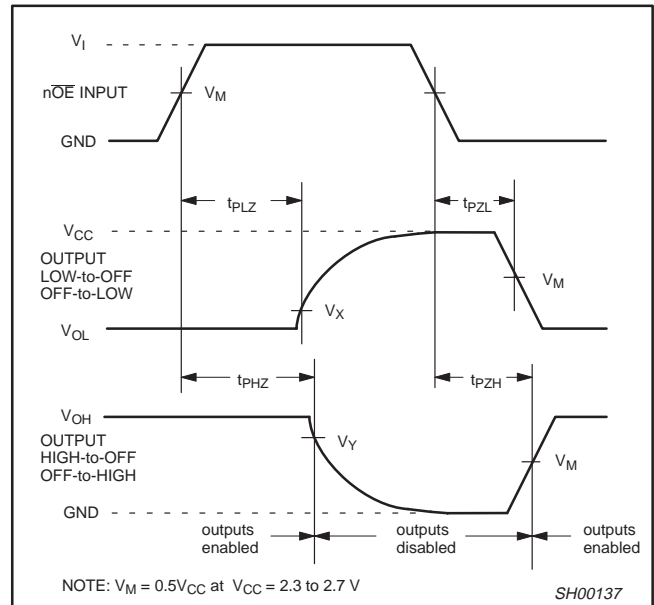
Waveform 3. The clock (CP) to Yn propagation delays, the clock pulse width and the maximum clock frequency.



Waveform 4. Data set-up and hold times for the An input to the LE input



Waveform 5. Data set-up and hold times for the An input to the clock CP input

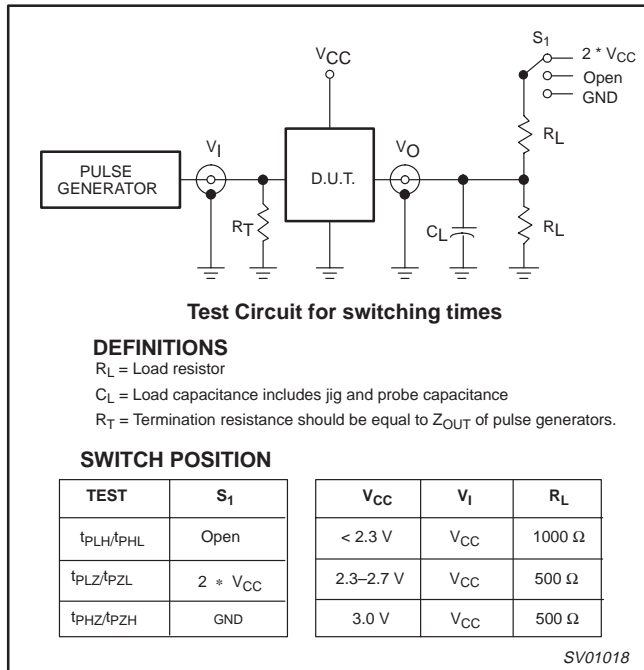


Waveform 6. 3-State enable and disable times

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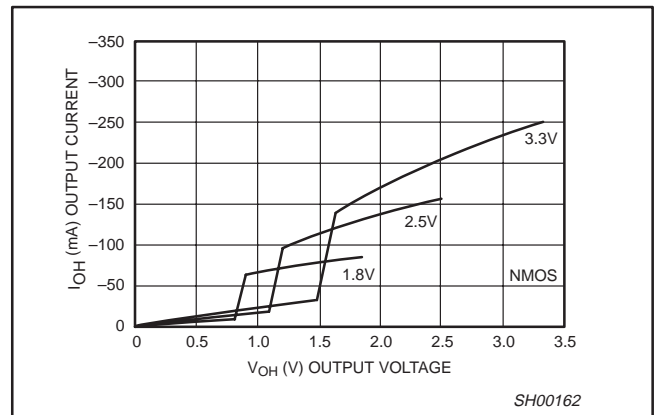
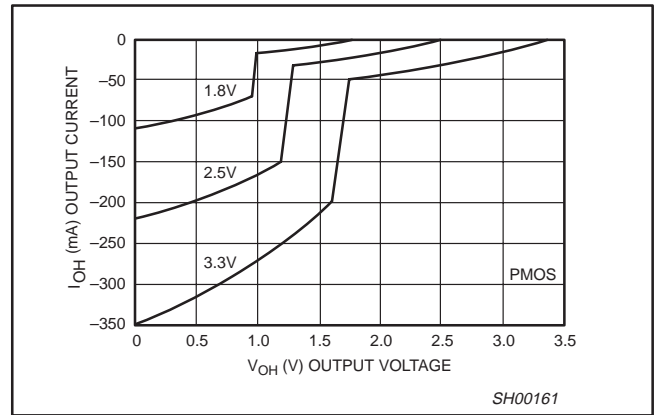
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TEST CIRCUIT



Waveform 7. Load circuitry for switching times

GRAPHS

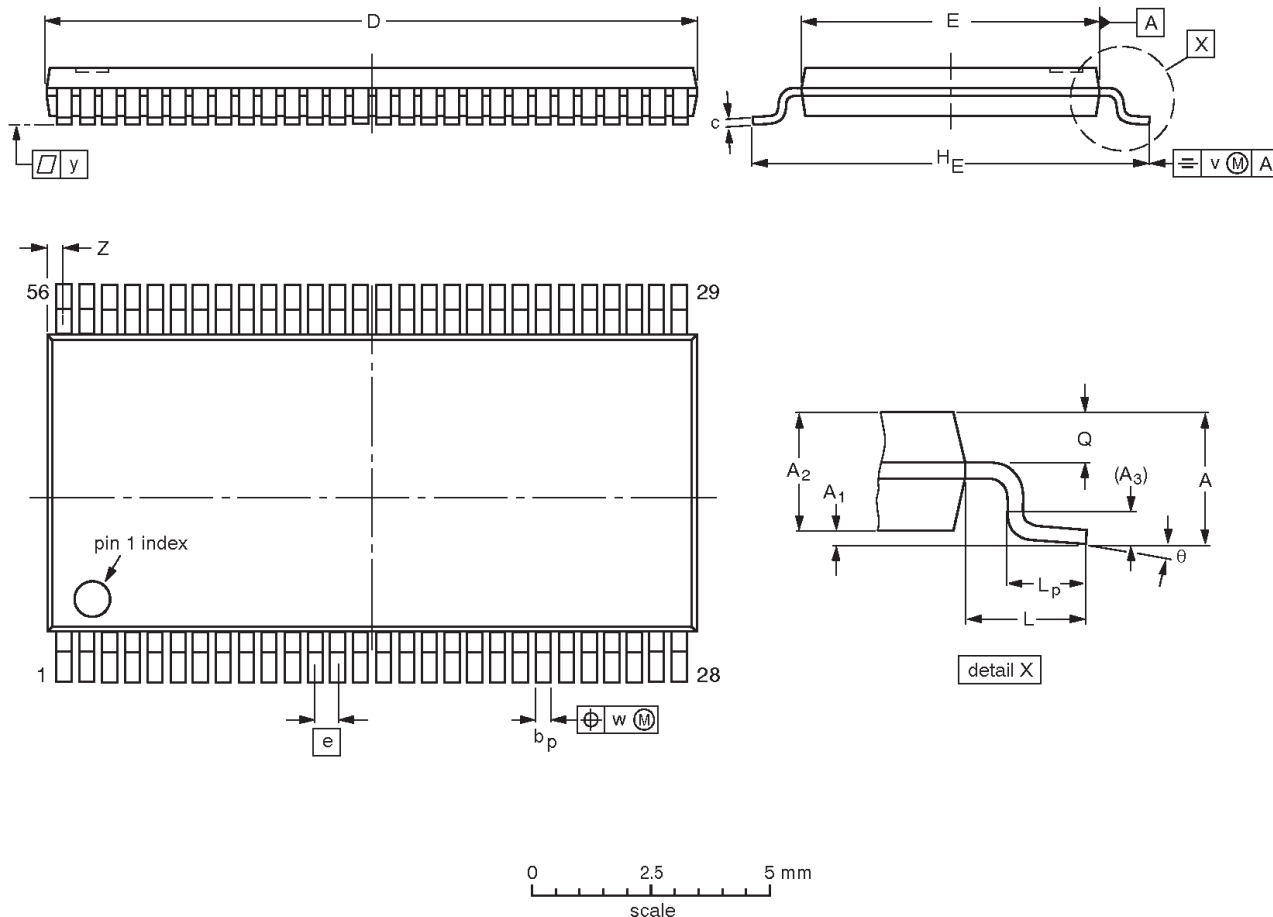


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TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1.0	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT364-1		MO-153EE				93-02-03 95-02-10

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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