DATA SHEET

74ALVT16899

2.5V/3.3V 18-bit latched transceiver with 16-bit parity generator/checker (3-State)

Product specification
IC23 Data Handbook

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Philips
Semiconductors

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2.5V/3.3V 18-bit latched transceiver with 16-bit parity generator/checker (3-State)

74ALVT16899

FEATURES

- Symmetrical (A and B bus functions are identical)
- Selectable generate parity or "feed-through" parity for A-to-B and B-to-A directions
- Independent transparent latches for A-to-B and B-to-A directions
- Selectable ODD/$\overline{\text{EVEN}}$ parity
- Continuously checks parity of both A bus and B bus latches as $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$
- Open-collector $\overline{\text{ERR}}$ output
- Ability to simultaneously generate and check parity
- Can simultaneously read/latch A and B bus data
- Output capability: +64 mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power up 3-State
- Power-up reset
- No bus current loading when output is tied to 5 V bus
- Live insertion/extraction permitted
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs

DESCRIPTION

The 74ALVT16899 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5V or 3.3V with I/O compatibility up to 5V.

The 74ALVT16899 is a 16-bit to 16-bit parity transceiver with separate transparent latches for the A bus and B bus. Either bus can generate or check parity. The parity bit can be fed-through with no change or the generated parity can be substituted with the $\overline{\text{SEL}}$ input.

The 74ALVT16899 features independent latch enables for the A and B bus latches, a select pin for ODD/$\overline{\text{EVEN}}$ parity, and separate error signal output pins for checking parity.

FUNCTIONAL DESCRIPTION:

The 74ALVT16899 has three principal modes of operation which are outlined below. All modes apply to both the A-to-B and B-to-A directions.

Transparent latch, Generate parity, Check A and B bus parity:
Bus A (B) communicates to Bus B (A), parity is generated and passed on to the B (A) Bus as BPAR (APAR). If LEA and LEB are High and the Mode Select ($\overline{\text{SEL}}$) is Low, the parity generated from A0-A7 and B0-B7 can be checked and monitored by $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$. (Fault detection on both input and output buses.)

Transparent latch, Feed-through parity, Check A and B bus parity:
Bus A (B) communicates to Bus B (A) in a feed-through mode if $\overline{\text{SEL}}$ is High. Parity is still generated and checked as $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$ and can be used as an interrupt to signal a data/parity bit error to the CPU.

Latched input, Generate/Feed-through parity, Check A (and B) bus parity:
Independent latch enables (LEA and LEB) allow other permutations of:

- Transparent latch / 1 bus latched / both buses latched
- Feed-through parity / generate parity
- Check in bus parity / check out bus parity / check in and out bus parity

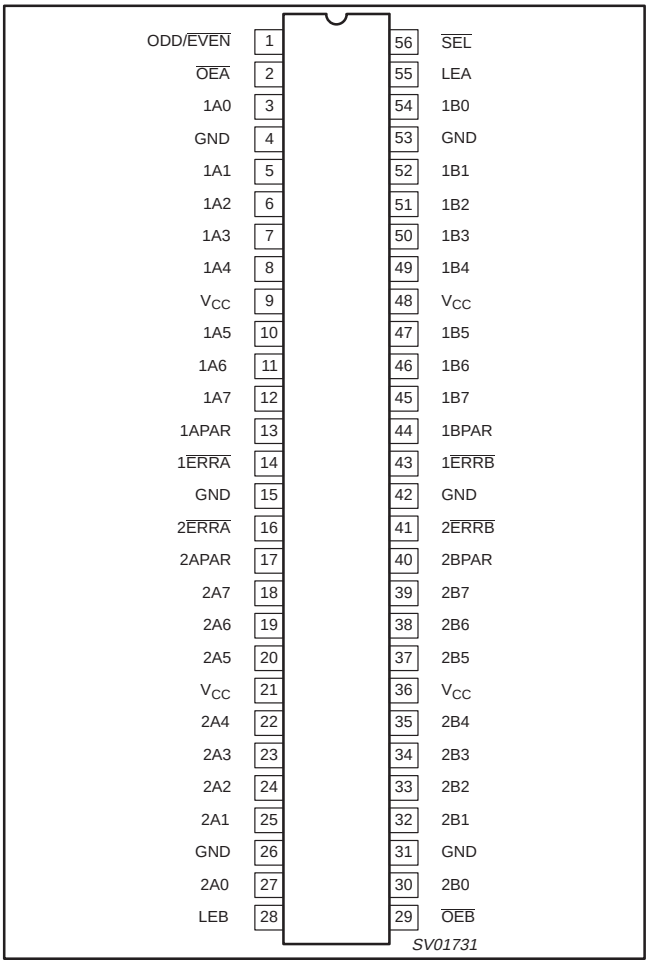
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL		UNIT
			2.5 V	3.3 V	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF	2.0 2.2	1.5 1.7	ns
t_{PLH} t_{PHL}	Propagation delay An to $\overline{\text{ERRA}}$	C_L = 50pF	9.8 7.0	7.8 5.1	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	3	pF
$C_{I/O}$	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	9	9	pF
I_{CCZ}	Quiescent supply current	Outputs disabled	40	70	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT16899	AV16899 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT16899 DGG	AV16899 DGG	SOT364-1

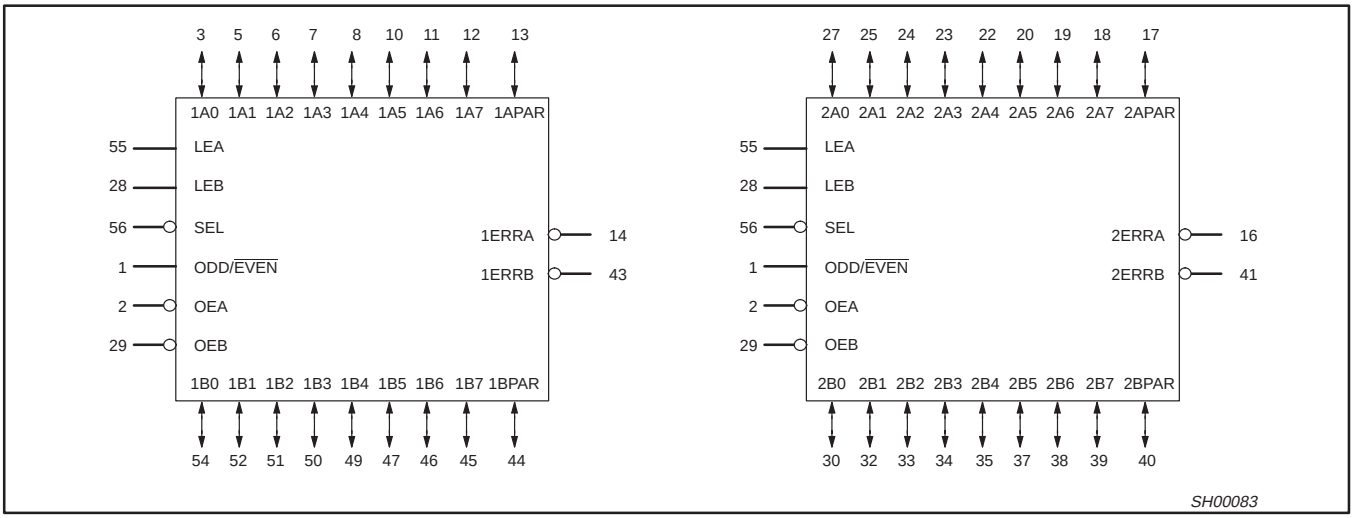
PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
1A0 - 1A7 2A0 - 2A7	3, 5, 6, 7, 8, 10, 11, 12 27, 25, 24, 23, 22, 20, 19, 18	Latched A bus 3-State inputs/outputs
1B0 - 1B7 2B0 - 2B7	54, 52, 51, 50, 49, 47, 46, 45 30, 32, 33, 34, 35, 37, 38, 39	Latched B bus 3-State inputs/outputs
1APAR 2APAR	13, 17	A bus parity 3-State input/output
1BPAR 2BPAR	44, 40	B bus parity 3-State input/output
ODD/$\overline{\text{EVEN}}$	1	Parity select input (Low for EVEN parity)
$\overline{\text{OEA}}$, $\overline{\text{OEB}}$	2, 29	Output enable inputs (gate A to B, B to A)
$\overline{\text{SEL}}$	56	Mode select input (Low for generate)
LEA, LEB	55, 28	Latch enable inputs (transparent High)
1$\overline{\text{ERRA}}$, 1$\overline{\text{ERRB}}$ 2$\overline{\text{ERRA}}$, 2$\overline{\text{ERRB}}$	14, 43, 16, 41	Error signal outputs (active-Low)
GND	4, 15, 26, 31, 42, 53	Ground (0V)
V_{CC}	9, 21, 36, 48	Positive supply voltage

LOGIC SYMBOL

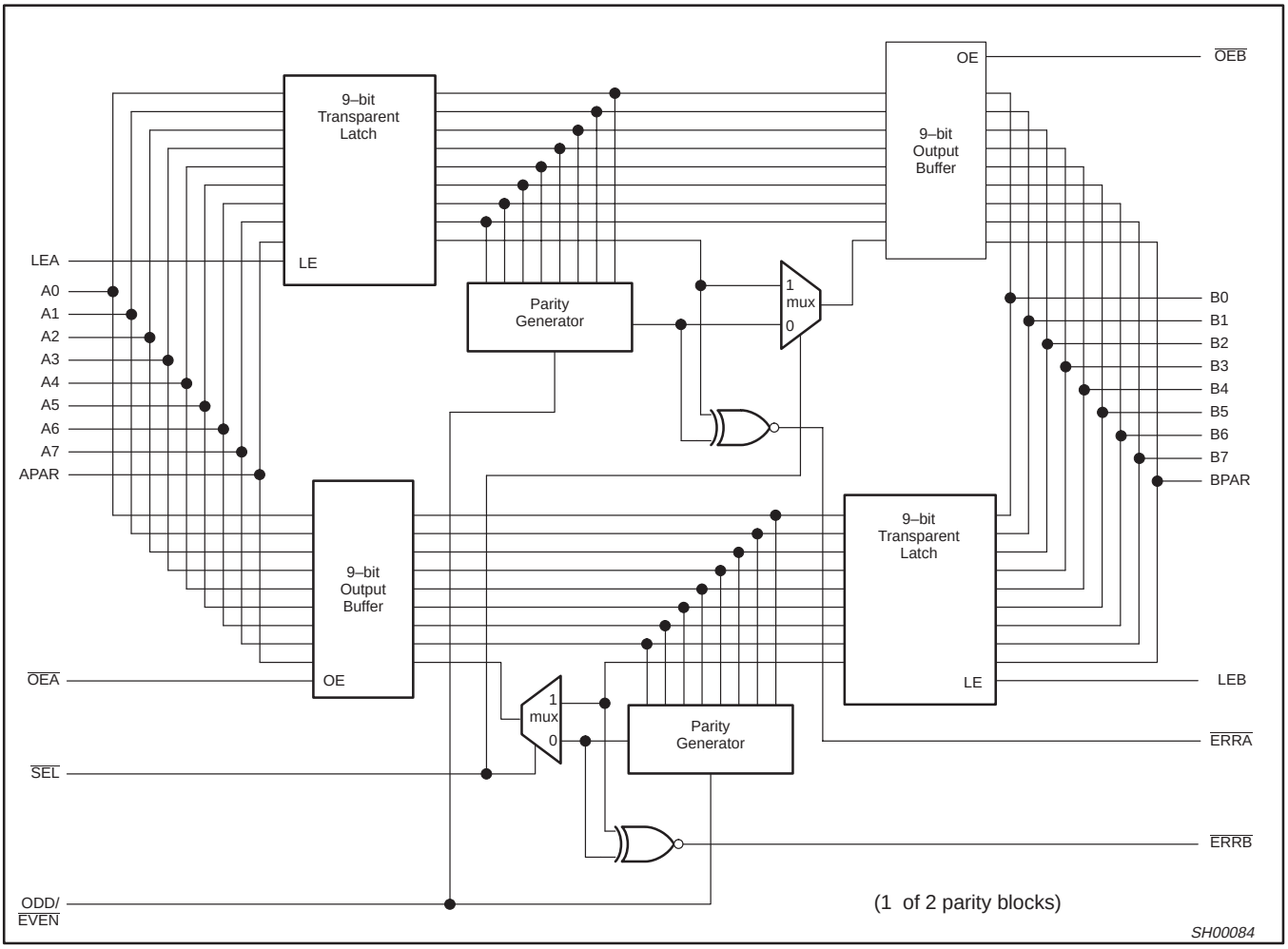


PARITY AND ERROR FUNCTION TABLE

INPUTS				OUTPUTS			PARITY MODES	
$\overline{SEL}$	ODD/$\overline{EVEN}$	xPAR (A or B)	Σ of High Inputs	xPAR (B or A)	$\overline{ERRt}$	$\overline{ERRr}$*		
H	H	H	Even Odd	H H	H L	H L	Odd Mode	Feed-through/check parity
H	H	L	Even Odd	L L	L H	L H		
H	L	H	Even Odd	H H	L H	L H	Even Mode	
H	L	L	Even Odd	L L	H L	H L		
L	H	H	Even Odd	H L	H L	H H	Odd Mode	Generate parity
L	H	L	Even Odd	H L	L H	H H		
L	L	H	Even Odd	L H	L H	H H	Even Mode	
L	L	L	Even Odd	L H	H L	H H		

H = High voltage level
L = Low voltage level
t = Transmit–if the data path is from A→B then $\overline{ERRt}$ is $\overline{ERRA}$
r = Receive–if the data path is from A→B then $\overline{ERRr}$ is $\overline{ERRB}$
* Blocked if latch is not transparent

BLOCK DIAGRAM



FUNCTION TABLE

INPUTS					OPERATING MODE
$\overline{OEB}$	$\overline{OEA}$	$\overline{SEL}$	LEA	LEB	
H	H	X	X	X	3-State A bus and B bus (input A & B simultaneously)
H	L	L	L	H	B → A, transparent B latch, generate parity from B0 - B7, check B bus parity
H	L	L	H	H	B → A, transparent A & B latch, generate parity from B0 - B7, check A & B bus parity
H	L	L	X	L	B → A, B bus latched, generate parity from latched B0 - B7 data, check B bus parity
H	L	H	X	H	B → A, transparent B latch, parity feed-through, check B bus parity
H	L	H	H	H	B → A, transparent A & B latch, parity feed-through, check A & B bus parity
L	H	L	H	X	A → B, transparent A latch, generate parity from A0 - A7, check A bus parity
L	H	L	H	H	A → B, transparent A & B latch, generate parity from A0 - A7, check A & B bus parity
L	H	L	L	X	A → B, A bus latched, generate parity from latched A0 - A7 data, check A bus parity
L	H	H	H	L	A → B, transparent A latch, parity feed-through, check A bus parity
L	H	H	H	H	A → B, transparent A & B latch, parity feed-through, check A & B bus parity
L	L	X	X	X	Output to A bus and B bus (NOT ALLOWED)

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage[3]		-0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	-0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–32	mA
I_{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		24		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[6]	V_{CC} = 3.6V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = 5.5V	Data pins[4]		0.1	20	
		V_{CC} = 3.6V; V_I = V_{CC}			0.5	1	
		V_{CC} = 3.6V; V_I = 0V			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		
		V_I = 0V to 3.6V; V_{CC} = 3.6V[7]		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} OE/$\overline{OE}$ = Don't care			33	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.05	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			4.6	7.0	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.06	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ±0.3V			
			MIN	TYP[1]	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	1	0.5 0.5	1.5 1.7	2.7 2.8	ns
t_{PLH} t_{PHL}	Propagation delay An to BPAR or Bn to APAR	4	2.5 2.0	5.0 4.6	8.0 7.3	ns
t_{PLH} t_{PHL}	Propagation delay An to $\overline{ERRA}$ or Bn to $\overline{ERRB}$	5	2.5 2.5	7.8 5.1	11.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay APAR to BPAR or BPAR to APAR	3	1.0 1.0	2.9 3.0	6.9 6.4	ns
t_{PLH} t_{PHL}	Propagation delay APAR to $\overline{ERRA}$ or BPAR to $\overline{ERRB}$	8	2.5 1.0	5.1 2.5	8.0 3.6	ns
t_{PLH} t_{PHL}	Propagation delay ODD/$\overline{EVEN}$ to APAR or BPAR	7	1.5 1.5	3.8 3.4	6.5 5.4	ns
t_{PLH} t_{PHL}	Propagation delay ODD/$\overline{EVEN}$ to $\overline{ERRA}$ or $\overline{ERRB}$	6	2.5 1.5	6.6 4.0	10.0 6.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SEL}$ to APAR or BPAR	10	1.0 1.0	2.6 2.4	4.0 3.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SEL}$ to $\overline{ERRA}$ or $\overline{ERRB}$	5	2.5 1.5	7.8 4.8	10.8 7.1	ns
t_{PLH} t_{PHL}	Propagation delay LEA to Bn or LEB to An	11	1.0 1.0	2.2 2.2	3.8 3.8	ns
t_{PLH} t_{PHL}	Propagation delay LEA to BPAR or LEB to APAR	11	2.5 2.0	5.3 4.9	8.5 7.6	ns
t_{PLH} t_{PHL}	Propagation delay LEA to $\overline{ERRA}$ or LEB to $\overline{ERRB}$	9	2.5 2.5	7.4 5.6	11.0 9.2	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEA}$ to An, APAR or $\overline{OEB}$ to Bn, BPAR	13, 14	1.0 0.5	2.4 1.8	5.8 3.3	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEA}$ to An, APAR or $\overline{OEB}$ to Bn, BPAR	13, 14	2.5 1.0	5.2 2.4	8.0 3.5	ns

NOTE:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V_{CC} = 3.3V ±0.3V		
			MIN	TYP	
t_s(H) t_s(L)	Setup time, High or Low An, APAR to LEA or Bn, BPAR to LEB	12	1.0 1.0	0.1 0.1	ns
t_h(H) t_h(L)	Hold time, High or Low An, APAR to LEA or Bn, BPAR to LEB	12	1.0 1.0	–0.1 0.1	ns
t_w(H)	Pulse width, High LEA or LEB	12	1.0	–	ns

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 2.3V; I_{OH} = –8mA		1.8	2.5		
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 2.3V; I_{OL} = 8mA				0.4	
V_{RST}	Power-up output low voltage[7]	V_{CC} = 2.7V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = 5.5V	Data pins[4]		0.1	20	
		V_{CC} = 2.7V; V_I = V_{CC}			0.1	10	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}[6]	Bus Hold current Data inputs	V_{CC} = 2.3V; V_I = 0.7V			115		µA
		V_{CC} = 2.3V; V_I = 1.7V			10		µA
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 2.3V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$ = Don't care			33	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.5	4.5	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.
7. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS (2.5V ±0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.5V ± 0.2V			
			MIN	TYP[1]	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	1	1.0 1.0	2.0 2.2	3.5 3.9	ns
t_{PLH} t_{PHL}	Propagation delay An to BPAR or Bn to APAR	4	3.0 3.0	7.0 6.5	10.5 10.2	ns
t_{PLH} t_{PHL}	Propagation delay An to $\overline{ERRA}$ or Bn to $\overline{ERRB}$	5	4.5 3.5	9.8 7.0	14.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay APAR to BPAR or BPAR to APAR	3	1.0 1.0	3.0 3.5	4.3 5.5	ns
t_{PLH} t_{PHL}	Propagation delay APAR to $\overline{ERRA}$ or BPAR to $\overline{ERRB}$	8	3.0 1.5	6.7 3.6	10.0 5.4	ns
t_{PLH} t_{PHL}	Propagation delay ODD/$\overline{EVEN}$ to APAR or BPAR	7	2.5 2.5	5.2 5.0	7.8 7.8	ns
t_{PLH} t_{PHL}	Propagation delay ODD/$\overline{EVEN}$ to $\overline{ERRA}$ or $\overline{ERRB}$	6	4.0 4.0	8.6 8.1	12.0 10.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SEL}$ to APAR or BPAR	10	1.5 1.5	3.7 3.2	5.5 5.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SEL}$ to $\overline{ERRA}$ or $\overline{ERRB}$	5	4.5 3.0	9.4 7.6	14.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay LEA to Bn or LEB to An	11	1.0 1.0	3.0 3.0	4.8 4.6	ns
t_{PLH} t_{PHL}	Propagation delay LEA to BPAR or LEB to APAR	11	2.5 2.5	7.5 7.4	12.2 11.2	ns
t_{PLH} t_{PHL}	Propagation delay LEA to $\overline{ERRA}$ or LEB to $\overline{ERRB}$	9	4.5 3.5	9.7 8.5	15.0 13.4	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEA}$ to An, APAR or $\overline{OEB}$ to Bn, BPAR	13, 14	1.5 1.0	4.0 2.6	6.0 4.6	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEA}$ to An, APAR or $\overline{OEB}$ to Bn, BPAR	13, 14	1.5 1.0	4.5 3.7	6.5 5.0	ns

NOTE:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

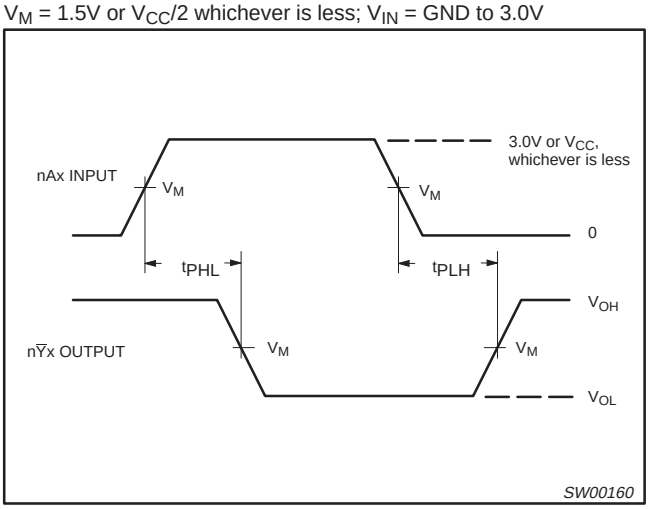
AC SETUP REQUIREMENTS (2.5V ±0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

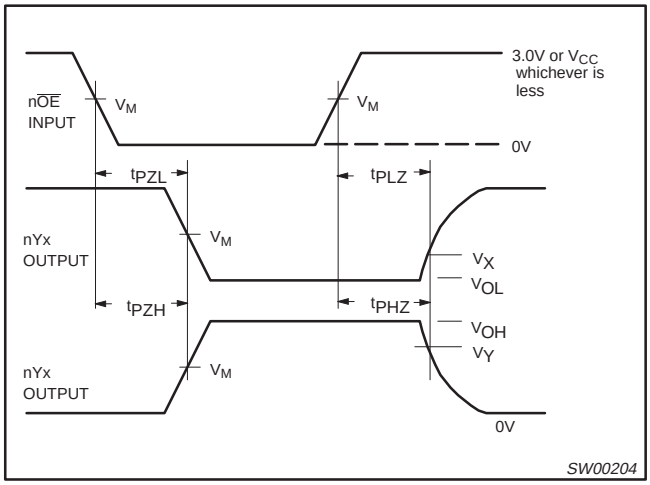
SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V_{CC} = 2.5V ±0.2V		
			MIN	TYP	
t_s(H) t_s(L)	Setup time, High or Low An, APAR to LEA or Bn, BPAR to LEB	12	–1.0 1.2	–0.4 0.4	ns
t_h(H) t_h(L)	Hold time, High or Low An, APAR to LEA or Bn, BPAR to LEB	12	–1.0 1.2	–0.4 0.5	ns
t_w(H)	Pulse width, High LEA or LEB	12	1.0	–	ns

AC WAVEFORMS

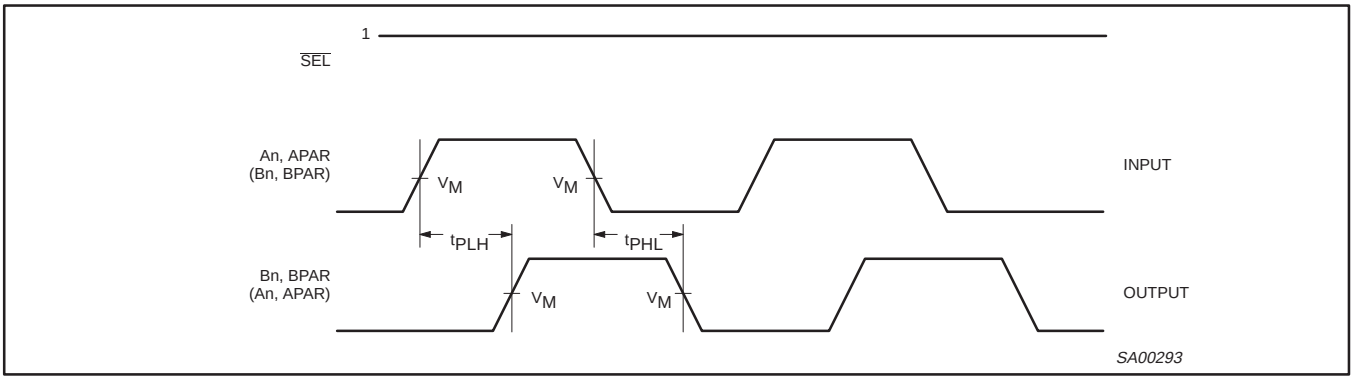
V_M = 1.5V or V_{CC}/2 whichever is less; V_{IN} = GND to 3.0V



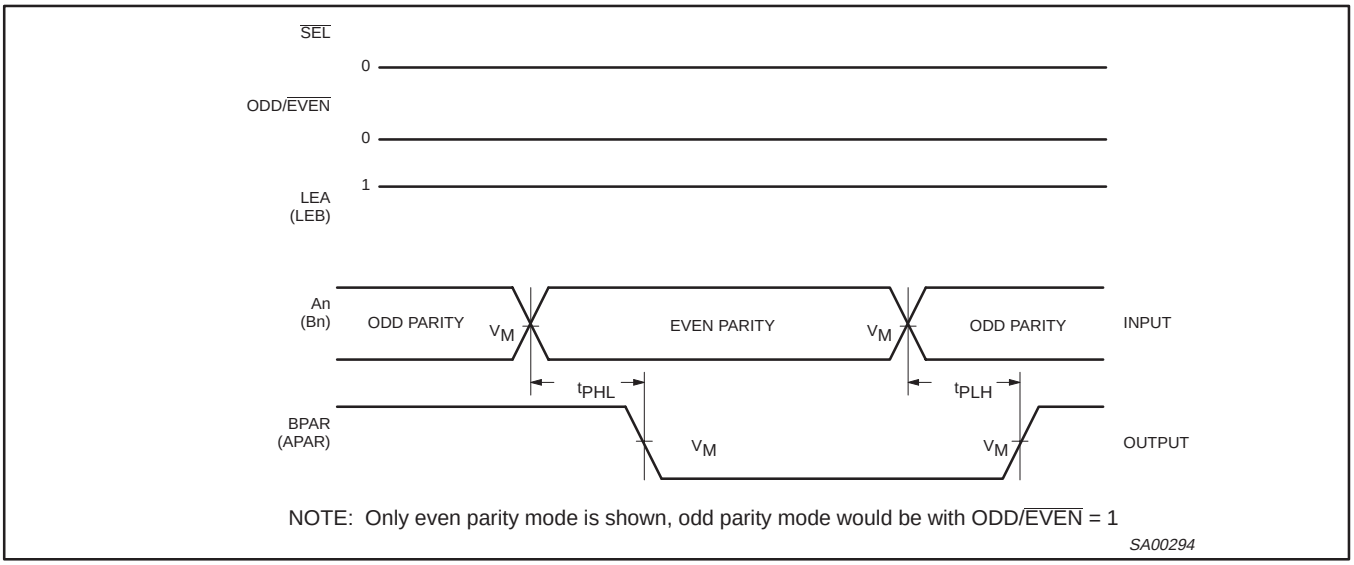
Waveform 1. Input (nAx) to Output (nYx) Propagation Delays



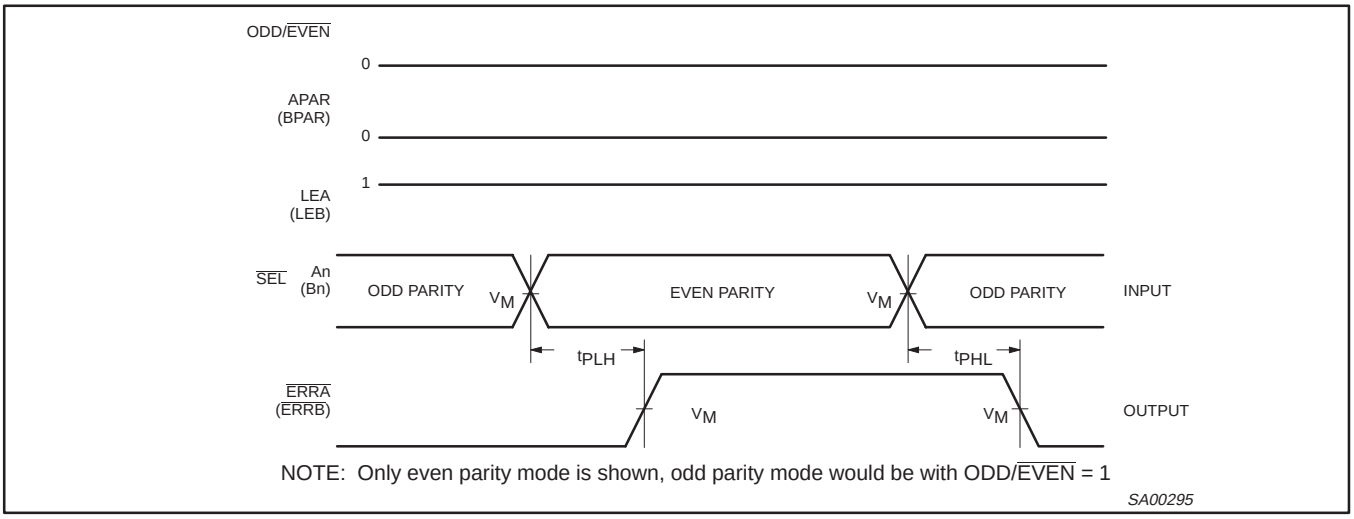
Waveform 2. 3-State Output Enable and Disable Times



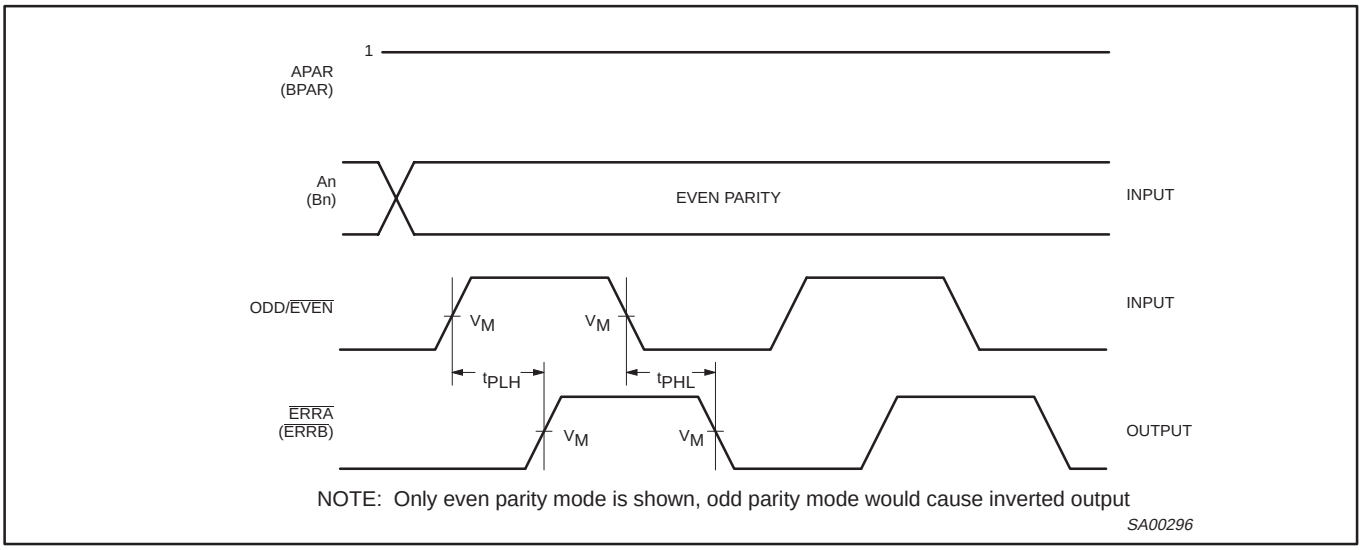
Waveform 3. Propagation Delay, An to Bn, Bn to An, APAR to BPAR, BPAR to APAR



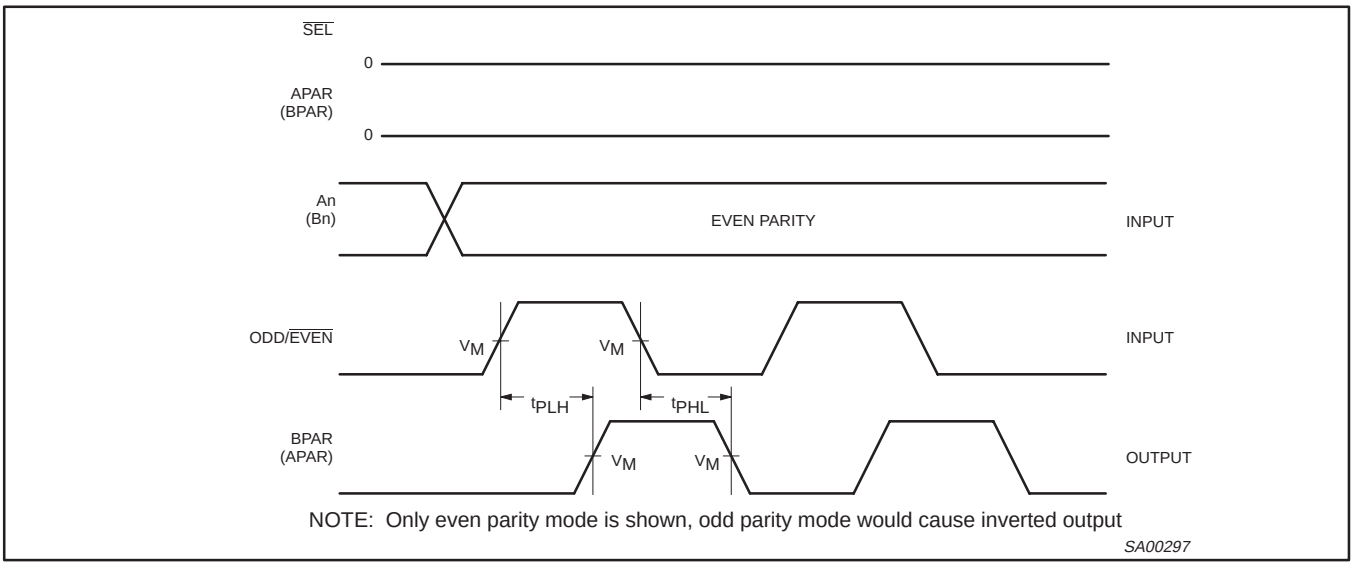
Waveform 4. Propagation Delay, An to BPAR or Bn to APAR



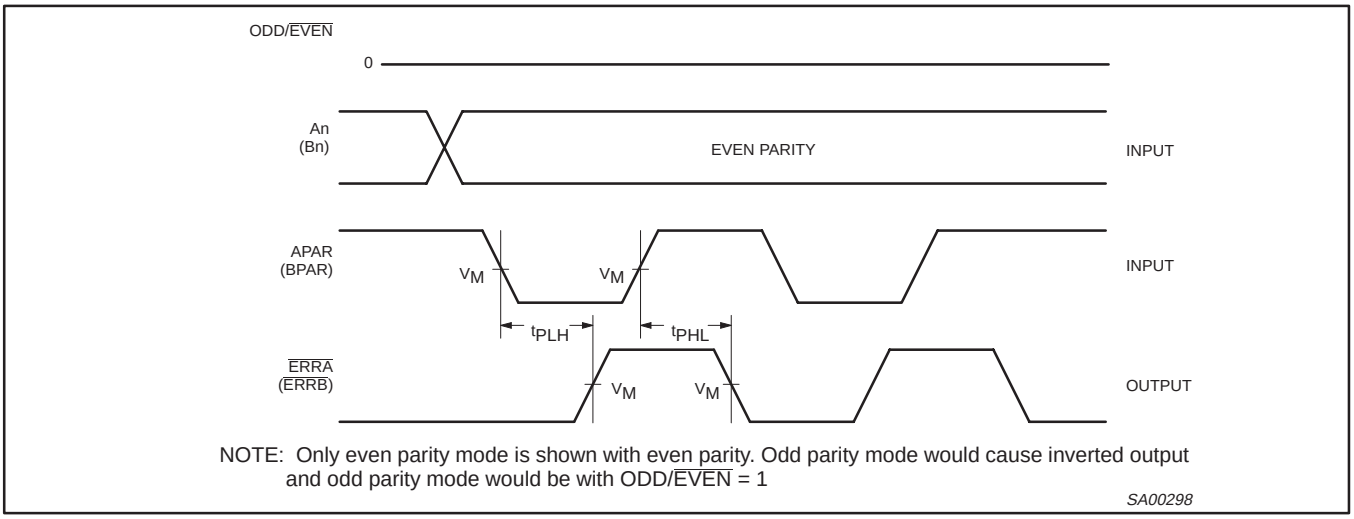
Waveform 5. Propagation Delay, An to $\overline{\text{ERRA}}$ or Bn to $\overline{\text{ERRB}}$



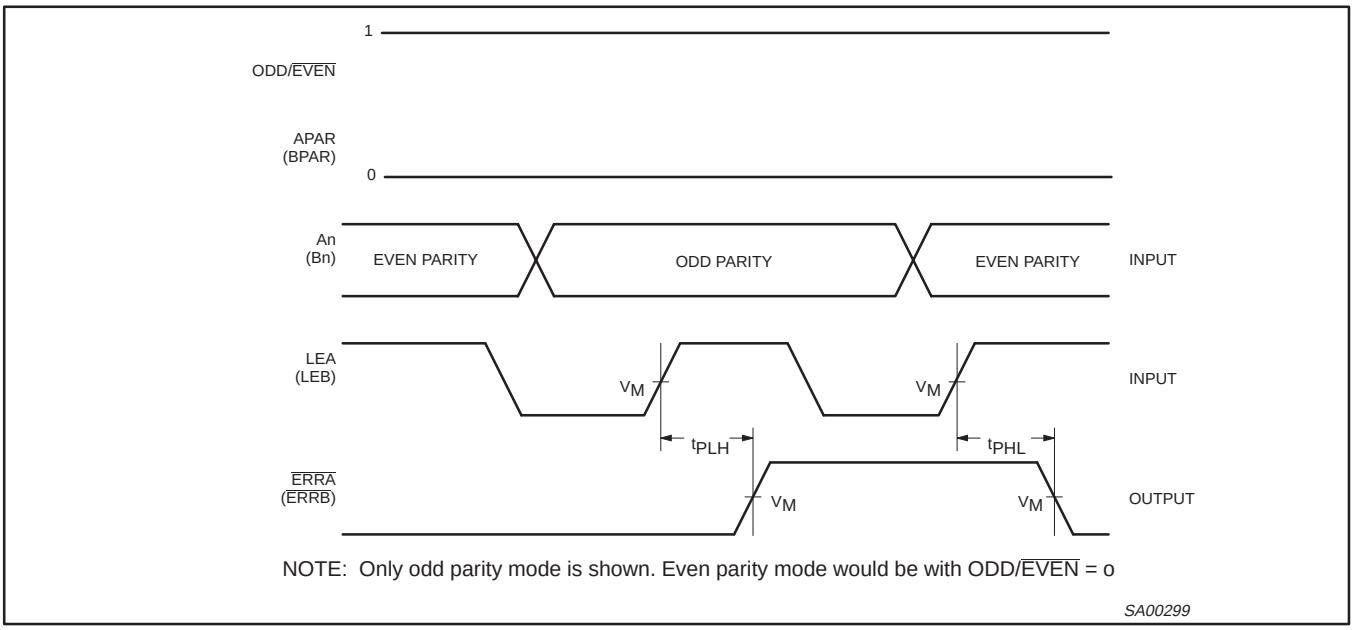
Waveform 6. Propagation Delay, ODD/$\overline{\text{EVEN}}$ to $\overline{\text{ERRA}}$ or ODD/$\overline{\text{EVEN}}$ to $\overline{\text{ERRB}}$



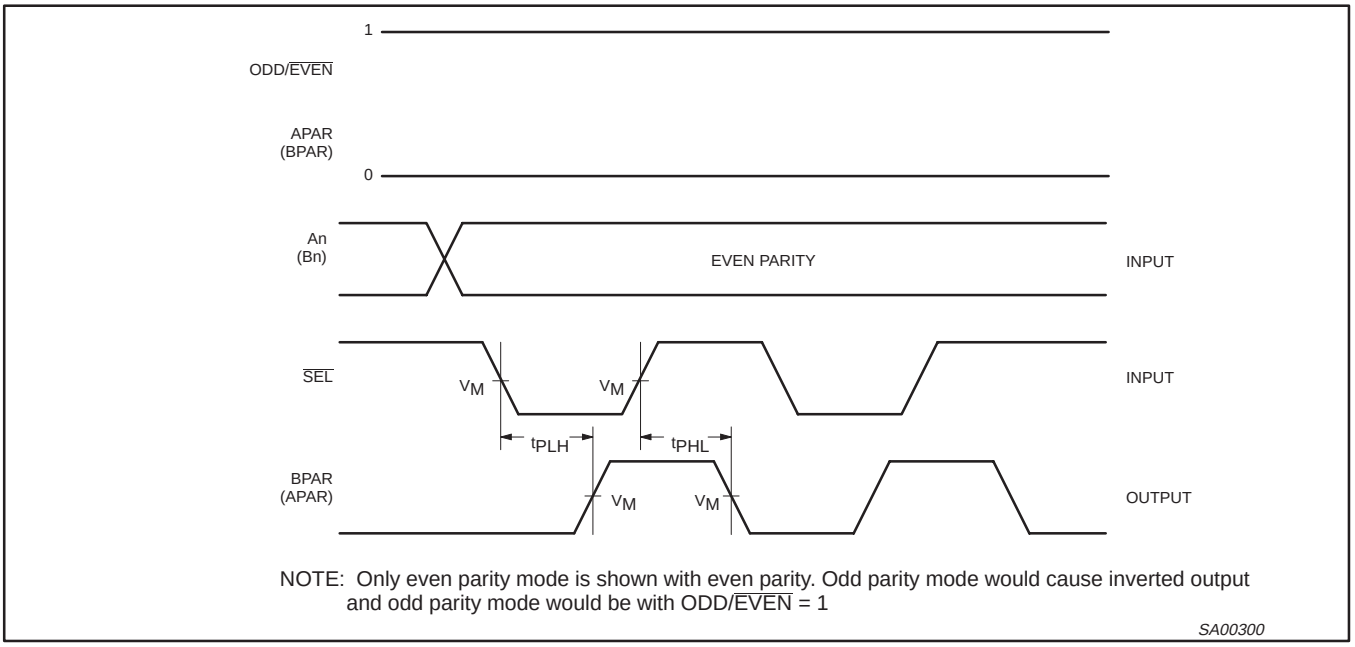
Waveform 7. Propagation Delay, ODD/$\overline{\text{EVEN}}$ to APAR or ODD/$\overline{\text{EVEN}}$ to BPAR



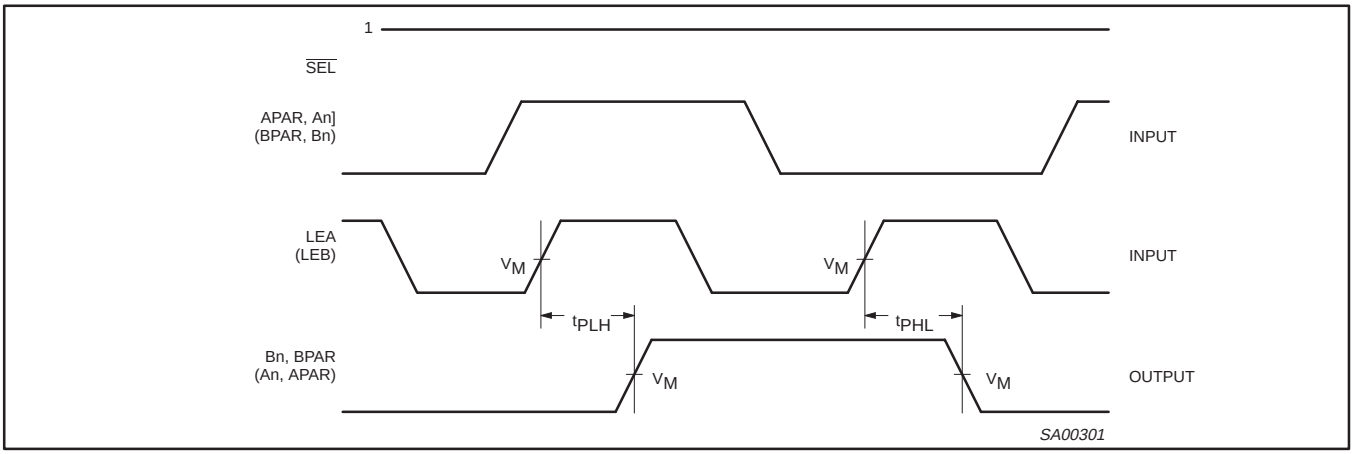
Waveform 8. Propagation Delay, APAR to $\overline{\text{ERRA}}$ or BPAR to $\overline{\text{ERRB}}$



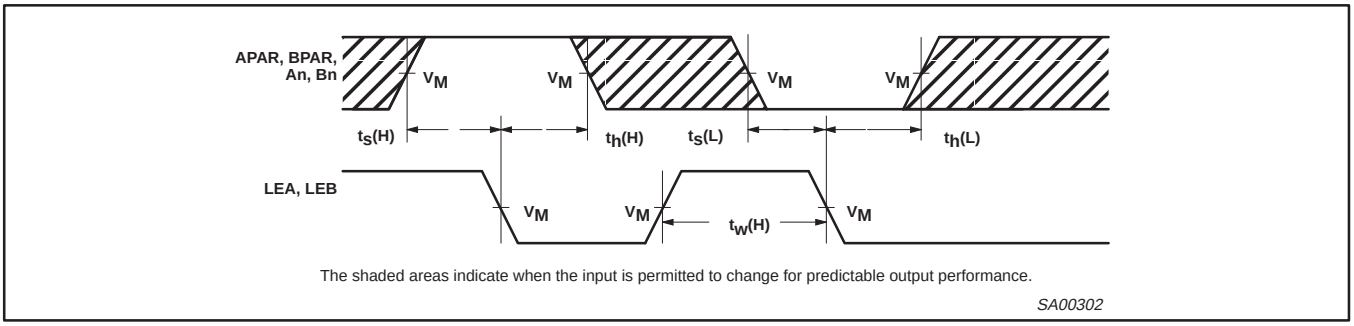
Waveform 9. Propagation Delay, LEA to $\overline{\text{ERRA}}$ or LEB to $\overline{\text{ERRB}}$



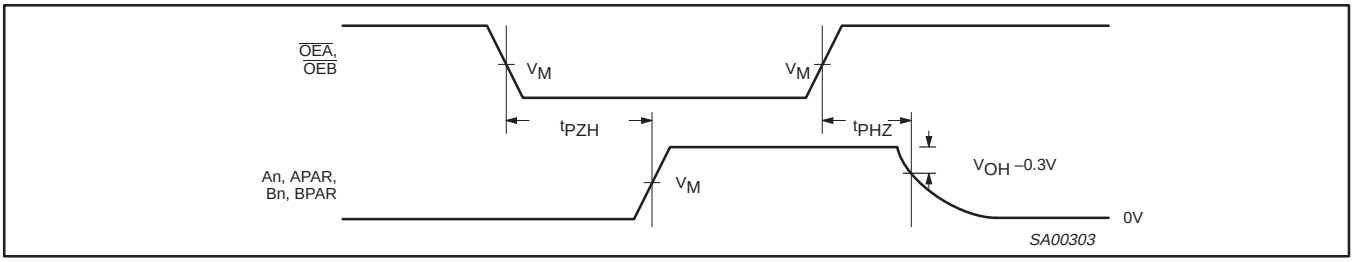
Waveform 10. Propagation Delay, $\overline{\text{SEL}}$ to BPAR or $\overline{\text{SEL}}$ to APAR



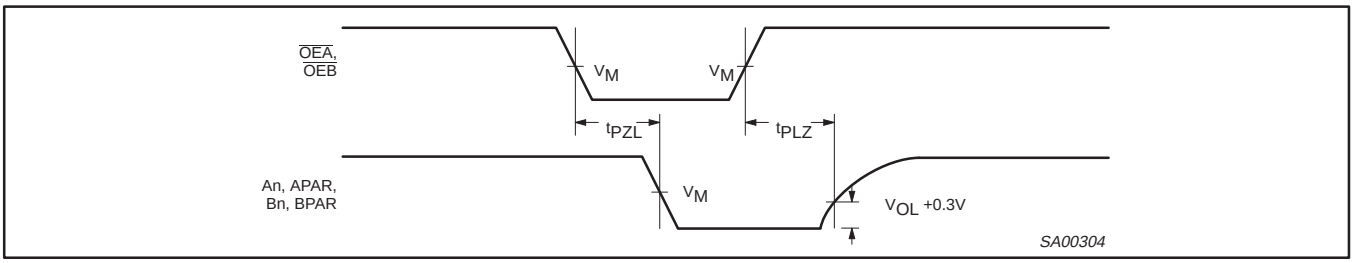
Waveform 11. Propagation Delay, LEA to BPAR or LEB to APAR, LEA to Bn or LEB to An



Waveform 12. Data Setup and Hold Times, Pulse Width High

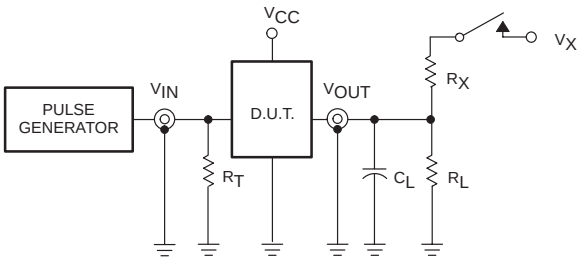


Waveform 13. 3-State Output Enable Time to High Level and Output Disable Time from High Level

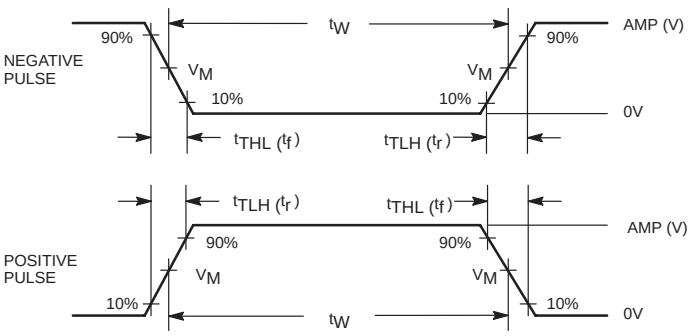


Waveform 14. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for Open Collector Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6 V or $V_{CC} \times 2$
t_{PLH}/t_{PHL}	open
t_{PHZ}/t_{PZH}	GND

LOAD VALUES

OUTPUT	R_X	V_X
$\overline{ERROR}$	100	V_{CC}
All other	500	switch

DEFINITIONS:

R_L = Load resistor; see AC CHARACTERISTICS for value.

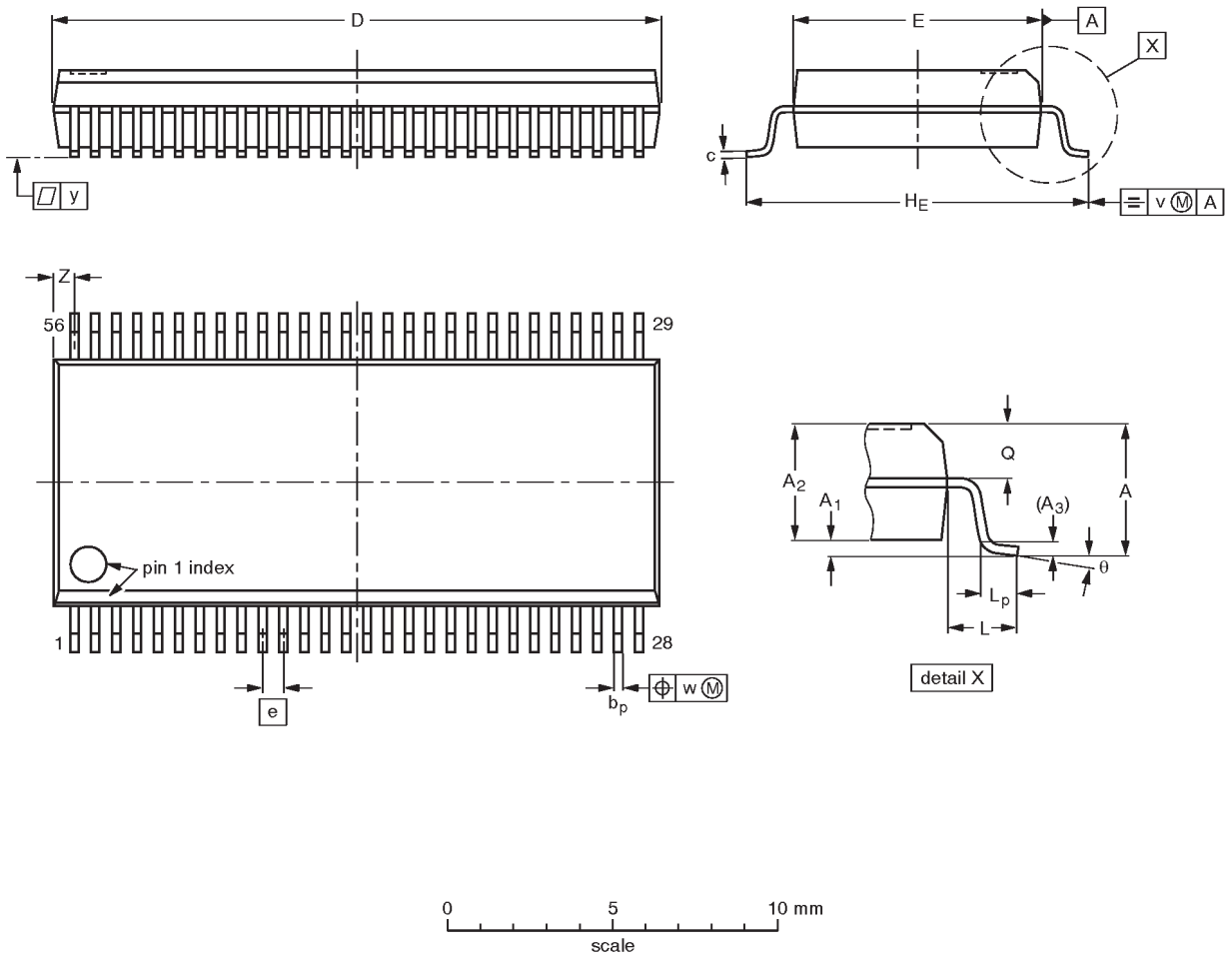
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_w	t_R	t_F
74ALVT16	3.0V or V_{CC}, which ever is less	≤ 10MHz	500ns	≤ 2.5ns	≤ 2.5ns

SV01732

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm **SOT371-1**



DIMENSIONS (mm are the original dimensions)

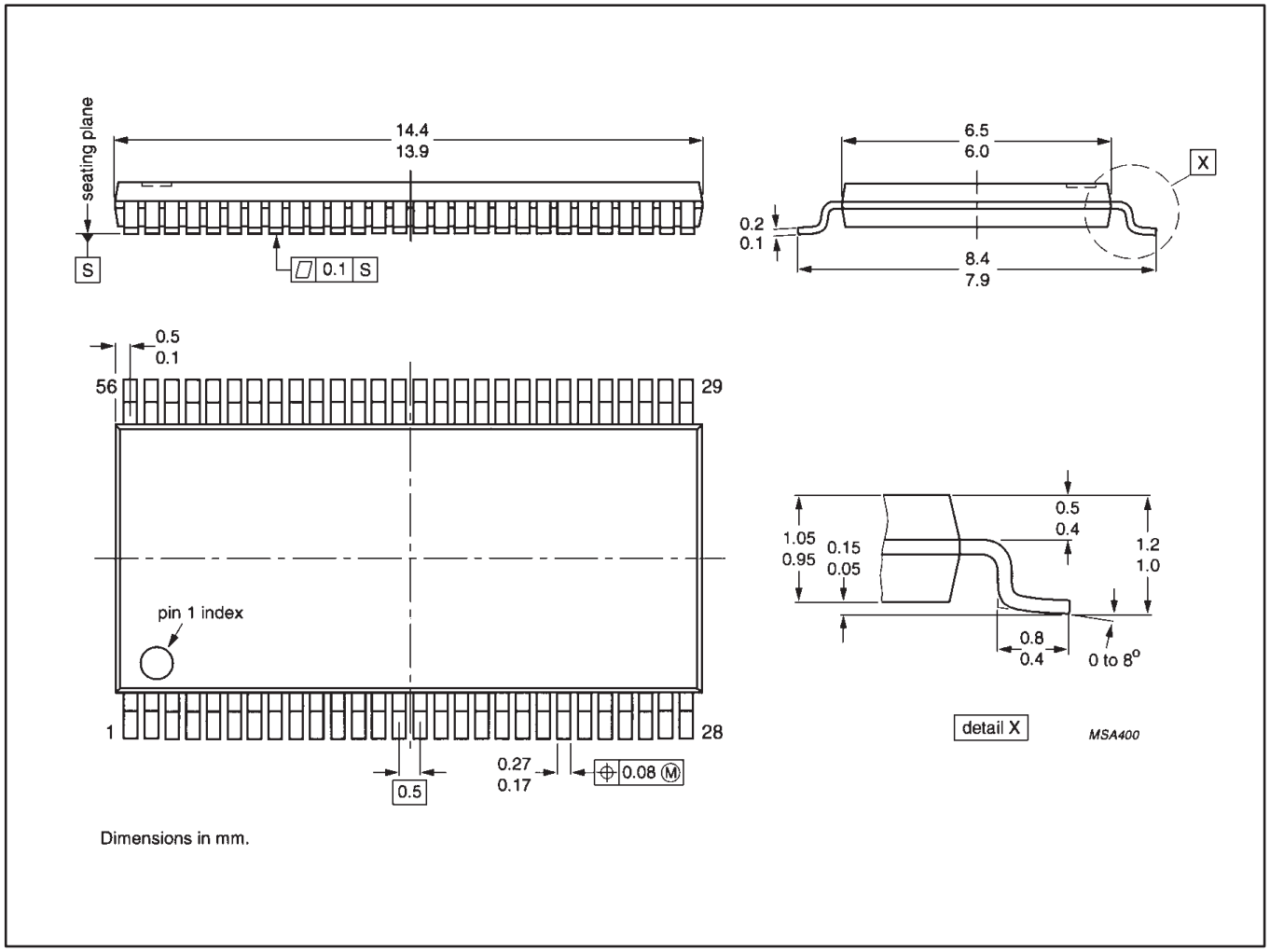
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118AB				~~93-11-02~~ 95-02-04

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm **SOT364-1**



Dimensions in mm.

NOTES

2.5V/3.3V 18-bit latched transceiver with 16-bit parity generator/checker (3-State)

74ALVT16899

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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