

## 74ALVCF162835

# Low Voltage 18-Bit Universal Bus Driver with 3.6V Tolerant Outputs and 26Ω Series Resistors in Outputs

### General Description

The 74ALVCF162835 low voltage 18-bit universal bus driver combines D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes.

Data flow is controlled by output-enable ( $\overline{OE}$ ), latch-enable (LE), and clock (CLK) inputs. The device operates in Transparent Mode when LE is held HIGH. The device operates in clocked mode when LE is LOW and CLK is toggled. Data transfers from the Inputs ( $I_n$ ) to Outputs ( $O_n$ ) on a Positive Edge Transition of the Clock. When  $\overline{OE}$  is LOW, the output data is enabled. When  $\overline{OE}$  is HIGH the output port is in a high impedance state.

The 74ALVCF162835 is designed with 26Ω series resistors in the outputs. This design reduces noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

The 74ALVCF162835 is designed for low voltage (1.65V to 3.6V)  $V_{CC}$  applications with I/O capability up to 3.6V.

The 74ALVCF162835 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

### Features

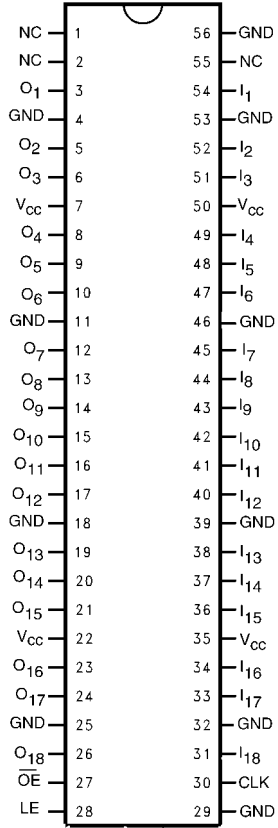
- Compatible with PC133 DIMM module specifications
- 1.65V-3.6V  $V_{CC}$  specifications provided
- 3.6V tolerant outputs
- 26Ω series resistors in outputs
- $t_{PD}$  (CLK to  $O_n$ )
  - 3.7 ns max for 3.0V to 3.6V  $V_{CC}$
  - 4.6 ns max for 2.3V to 2.7V  $V_{CC}$
  - 7.4 ns max for 1.65V to 1.95V  $V_{CC}$
- Power-down high impedance outputs
- Latchup conforms to JEDEC JED78
- ESD performance:
  - Human body model > 2000V
  - Machine model >200V

### Ordering Code:

Order Number	Package Number	Package Description
74ALVCF162835T	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Connection Diagram



### Pin Descriptions

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
LE	Latch Enable Input
CLK	Clock Input
$I_1 - I_{18}$	Data Inputs
$O_1 - O_{18}$	3-STATE Outputs

### Truth Table

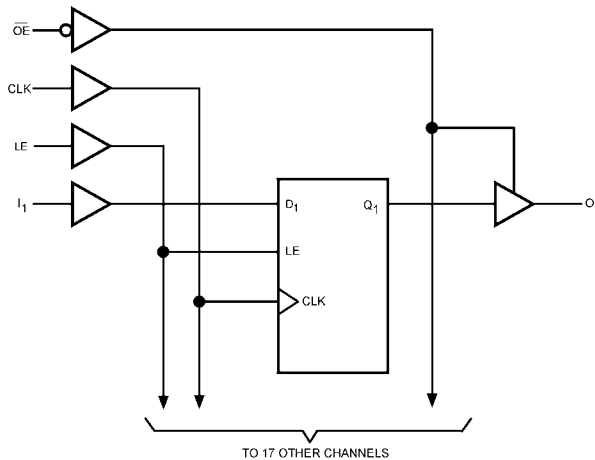
Inputs				Outputs
$\overline{OE}$	LE	CLK	$I_n$	$O_n$
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	H	X	$O_0$ (Note 1)
L	L	L	X	$O_0$ (Note 2)

H = Logic HIGH  
 L = Logic LOW  
 X = Don't Care, but not floating  
 Z = High Impedance  
 ↑ = LOW-to-HIGH Clock Transition

**Note 1:** Output level before the indicated steady-state input conditions were established provided that CLK was HIGH before LE went LOW.

**Note 2:** Output level before the indicated steady-state input conditions were established.

### Logic Diagram



**Absolute Maximum Ratings** (Note 3)

Supply Voltage ( $V_{CC}$ )	-0.5V to +4.6V
DC Input Voltage ( $V_I$ )	-0.5V to 4.6V
Output Voltage ( $V_O$ ) (Note 4)	-0.5V to $V_{CC} + 0.5V$
DC Input Diode Current ( $I_{IK}$ )	
$V_I < 0V$	-50 mA
DC Output Diode Current ( $I_{OK}$ )	
$V_O < 0V$	-50 mA
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ )	$\pm 50$ mA
DC $V_{CC}$ or GND Current per Supply Pin ( $I_{CC}$ or GND)	$\pm 100$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C

**Recommended Operating Conditions** (Note 5)

Power Supply	
Operating	1.65V to 3.6V
Input Voltage	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta t/\Delta V$ )	
$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V

**Note 3:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 4:**  $I_O$  Absolute Maximum Rating must be observed.

**Note 5:** Floating or unused control inputs must be held HIGH or LOW.

**DC Electrical Characteristics**

Symbol	Parameter	Conditions	$V_{CC}$ (V)	Min	Max	Units
$V_{IH}$	HIGH Level Input Voltage		1.65 - 1.95 2.3 - 2.7 2.7 - 3.6	$0.65 \times V_{CC}$ 1.7 2.0		V
$V_{IL}$	LOW Level Input Voltage		1.65 - 1.95 2.3 - 2.7 2.7 - 3.6		$0.35 \times V_{CC}$ 0.7 0.8	V
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	1.65 - 3.6	$V_{CC} - 0.2$		V
		$I_{OH} = -2$ mA	1.65	1.2		
		$I_{OH} = -4$ mA	2.3	1.9		
		$I_{OH} = -6$ mA	2.3	1.7		
		$I_{OH} = -8$ mA	3.0	2.4		
		$I_{OH} = -12$ mA	2.7	2		
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	1.65 - 3.6		0.2	V
		$I_{OL} = 2$ mA	1.65		0.45	
		$I_{OL} = 4$ mA	2.3		0.4	
		$I_{OL} = 6$ mA	2.3		0.55	
		$I_{OL} = 8$ mA	3.0		0.55	
		$I_{OL} = 12$ mA	2.7		0.6	
$I_{OH}$	High Level Output Current		1.65		-2	mA
			2.3		-6	
			2.7		-8	
			3.0		-12	
$I_{OL}$	Low Level Output Current		1.65		2	mA
			2.3		6	
			2.7		8	
			3.0		12	
$I_I$	Input Leakage Current	$0 \leq V_I \leq 3.6V$	1.65 - 3.6		$\pm 5.0$	$\mu A$
$I_{OZ}$	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V, V_I = V_{IH}$ or $V_{IL}$	1.65 - 3.6		$\pm 10$	$\mu A$
$I_{OFF}$	Power Off Leakage Current	$0V \leq (V_I, V_O) \leq 3.6V$	0		10	mA
$I_{CC}$	Quiescent Supply Current	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6		40	$\mu A$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	$V_{IH} = V_{CC} - 0.6V$	2.7 - 3.6		750	$\mu A$

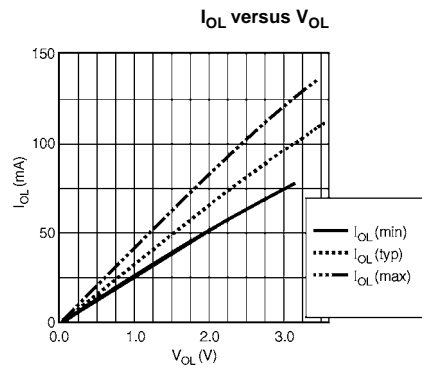
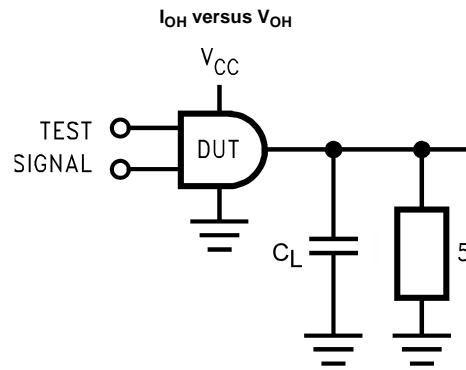
## AC Electrical Characteristics

Symbol	Parameter	$T_A = -40^\circ\text{C to } +85^\circ\text{C}, R_L = 500\Omega$								Units
		$C_L = 50\text{ pF}$				$C_L = 30\text{ pF}$				
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		$V_{CC} = 2.5 \pm 0.2V$		$V_{CC} = 1.8V \pm 0.15V$		
		Min	Max	Min	Max	Min	Max	Min	Max	
$f_{MAX}$	Maximum Clock Frequency	250		200		200		100		MHz
$t_{PHL}, t_{PLH}$	Propagation Delay Bus-to-Bus	1.1	3.6	1.3	4.5	0.8	4.0	1.5	7.2	ns
$t_{PHL}, t_{PLH}$	Propagation Delay Clock to Bus	1.5	3.7	2.0	4.6	1.5	4.1	2.0	7.4	ns
$t_{PHL}, t_{PLH}$	Propagation Delay LE to Bus	1.1	4.2	1.3	5.2	0.8	4.7	1.5	8.5	ns
$t_{PZL}, t_{PZH}$	Output Enable Time	1.1	4.8	1.3	6.4	0.8	5.9	1.5	9.8	ns
$t_{PLZ}, t_{PHZ}$	Output Disable Time	1.1	4.7	1.3	5.2	0.8	4.7	1.5	7.9	ns
$t_S$	Setup Time	1.5		1.5		1.5		2.5		ns
$t_H$	Hold Time	0.7		0.7		0.7		1.0		ns
$t_W$	Pulse Width	1.5		1.5		1.5		4.0		ns

## Capacitance

Symbol	Parameter	Conditions	$T_A = +25^\circ\text{C}$		Units
			$V_{CC}$	Typical	
$C_{IN}$	Input Capacitance	$V_I = 0V$ or $V_{CC}$	3.3	3.5	pF
$C_{OUT}$	Output Capacitance	$V_I = 0V$ or $V_{CC}$	3.3	5.5	pF
$C_{PD}$	Power Dissipation Capacitance	Outputs Enabled $f = 10\text{ MHz}, C_L = 0\text{ pF}$	3.3	13	pF
			2.5	13	

## $I_{OUT} - V_{OUT}$ Characteristics



## AC Loading and Waveforms

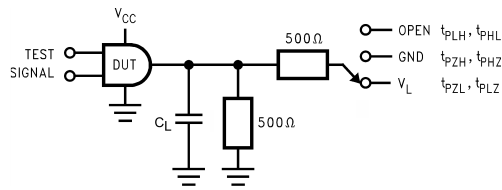


FIGURE 3. AC Test Circuit

Table 1: Values for Figure 1

TEST	SWITCH
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	$V_L$
$t_{PZH}$ , $t_{PHZ}$	GND

Table 2: Variable Matrix  
( Input Characteristics:  $f = 1\text{MHz}$ ;  $t_r=t_f=2\text{ns}$ ;  $Z_0 = 50\Omega$  )

Symbol	$V_{CC}$			
	$3.3\text{V} \pm 0.3\text{V}$	2.7V	$2.5\text{V} \pm 0.2\text{V}$	$1.8\text{V} \pm 0.15\text{V}$
$V_{mi}$	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_{mo}$	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_X$	$V_{OL} + 0.3\text{V}$	$V_{OL} + 0.3\text{V}$	$V_{OL} + 0.15\text{V}$	$V_{OL} + 0.15\text{V}$
$V_Y$	$V_{OH} - 0.3\text{V}$	$V_{OH} - 0.3\text{V}$	$V_{OH} - 0.15\text{V}$	$V_{OH} - 0.15\text{V}$
$V_L$	6V	6V	$V_{CC} * 2$	$V_{CC} * 2$

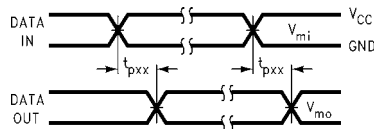


FIGURE 4. Waveform for Inverting and Non-inverting Functions

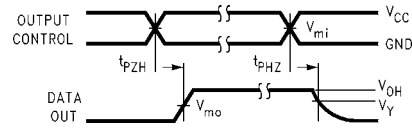


FIGURE 5. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

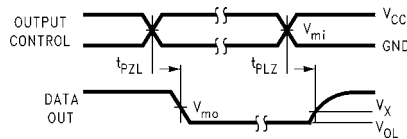
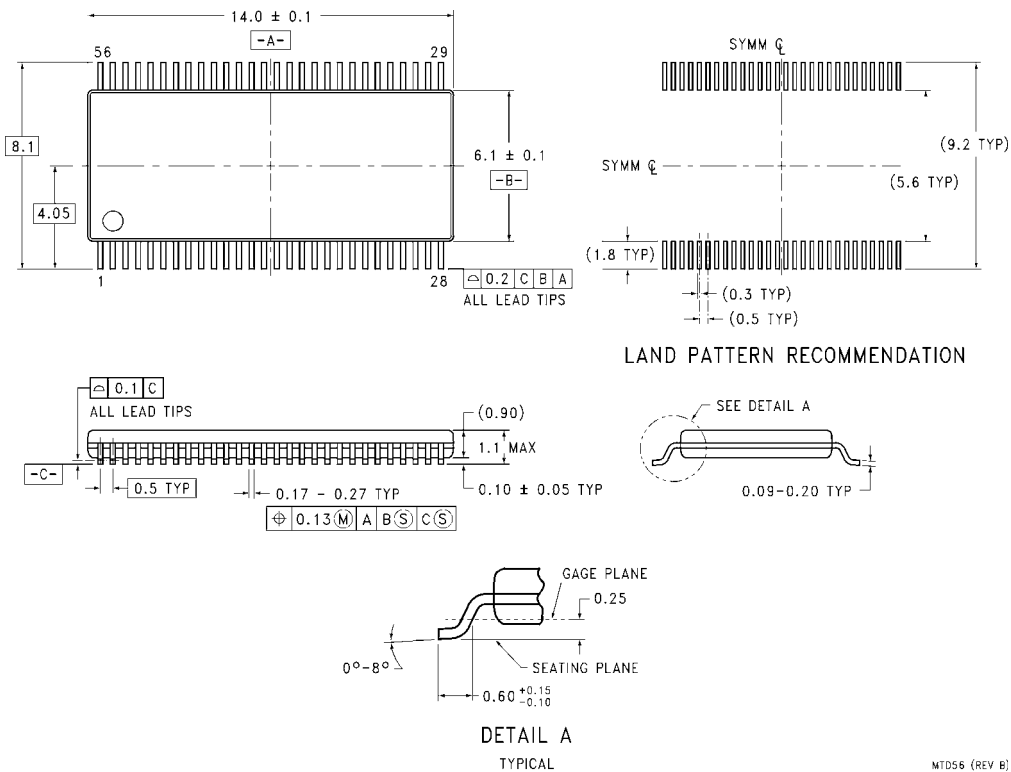


FIGURE 6. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

**Physical Dimensions** inches (millimeters) unless otherwise noted



**56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide  
Package Number MTD56**

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