## LME49990 Overture® **E-Series**

January 8, 2010

## **Ultra-low Distortion, Ultra-low Noise Operational Amplifier**

#### **General Description**

The LME49990 is part of the ultra-low distortion, low noise, high slew rate operational amplifier series optimized and fully specified for high performance, high fidelity applications. The LME49990 combines low voltage noise density (0.9nV/\(\sqrt{Hz}\)) with vanishing low THD+N (0.00001%). The LME49990 has a high slew rate of ±22V/µs and an output current capability of  $\pm 27$ mA. It drives  $600\Omega$  loads to within 2V of either power supply voltage.

The LME49990's outstanding Gain (135dB), CMRR (137dB), PSRR (144dB), and  $V_{OS} \, (130 \mu V)$  give the amplifier excellent operational amplifier DC performance. The LME49990 has a wide supply range of ±5V to ±18V. The LME49990 is unity gain stable and is available in an 8-lead narrow body SOIC.

### **Key Specifications**

Input Noise Density (f = 1kHz)	0.9nV/√ <del>Hz</del> (typ)
	1.3nV/√Hz (max)

■ THD+N  $(A_V = 1, V_{OUT} = 3V_{RMS}, f_{IN} = 1kHz)$ 

> $R_1 = 600\Omega$ 0.00001%

1/f Corner Frequency 43Hz (typ)

■ Slew Rate ±22V/µs (max)

■ Gain Bandwidth

 $(A_V = 10^4, R_I = 2k\Omega, f = 90kHz)$ 110MHz (typ)

PSRR 144dB (typ)

137dB (typ) ■ CMRR

±5V to ±18V ■ Power Supply Voltage Range

#### **Features**

- Easily drives 600Ω load
- Output short circuit protection

### **Applications**

- Ultra high quality audio signal processing
- Active Filters
- Preamplifiers
- Spectrum analyzers
- Ultrasound preamplifiers
- Sigma-Delta ADC/DAC buffers

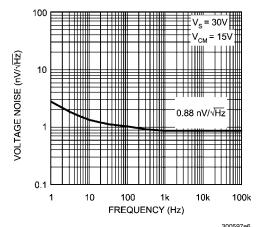


FIGURE 1. Voltage Noise Spectral Density

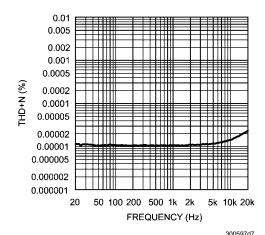
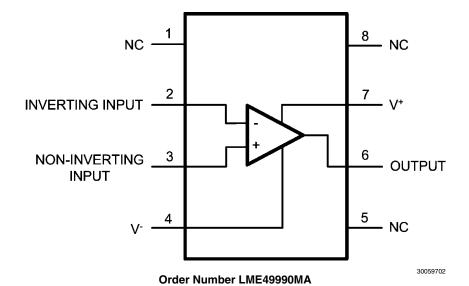


FIGURE 2. THD+N vs Frequency

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# **Connection Diagram**



# **Ordering Information**

Order Number	Package	Package DWG # Transport Media		MSL Level
LME49990MA	8 Ld SOIC	M08A	95 units in reel	1
LME49990MAX	8 Ld SOIC	DIC M08A 2500 units in tape and reel		1

See NS Package Number — M08A

#### **Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Supply Voltage

ESD Rating (*Note 4*) 2000V ESD Rating (*Note 5*) 200V ESD Rating (*Note 8*) 1000V Junction Temperature 150°C

Thermal Resistance  $\theta_{JA}$  (SO) 145°C/W

Soldering Information

Infrared or Convection (20 sec) 260°C

### **Operating Ratings** (Note 1)

Temperature Range

 $\begin{aligned} &\mathsf{T}_{\mathsf{MIN}} \leq \mathsf{T}_{\mathsf{A}} \leq \mathsf{T}_{\mathsf{MAX}} & -40^{\circ}\mathsf{C} \leq \mathsf{T}_{\mathsf{A}} \leq 85^{\circ}\mathsf{C} \\ &\mathsf{Supply Voltage Range} & \pm 5\mathsf{V} \leq \mathsf{V}_{\mathsf{S}} \leq \pm 18\mathsf{V} \end{aligned}$ 

#### **Electrical Characteristics** (Note 2)

The following specifications apply for  $V_S = \pm 15V$ ,  $R_L = 2k\Omega$ ,  $f_{IN} = 1kHz$ , and  $T_A = 25^{\circ}C$ , unless otherwise specified.

			LME49990		Units
Symbol	Parameter	Conditions	Typical	pical Limit	
			(Note 6)	(Note 7)	(Limits)
POWER SUF	PPLY				
V <sub>CC</sub>	Operating Supply Voltage			±5	V (min)
V CC	Operating Supply Voltage			±18	V (max)
		$V_{CM} = 0V, V_{O} = 0V, I_{O} = 0mA$			
lana	Quiescent Current	$V_{CC} = \pm 5V$	8	10	mA (max)
I <sub>CCQ</sub>	Quiescent Guirent	$V_{CC} = \pm 15V$	9	11	max)
		$V_{CC} = \pm 18V$	9	12	
PSRR	Power Supply Paination Patio	$V_{CC} = \pm 5V$ to $\pm 18V$	144	119	dB (min)
ronn	Power Supply Rejection Ratio	$T_{MIN}-T_{MAX}$	137	116	dB (min)
DYNAMIC PI	ERFORMANCE	•	•		
	Total Harmonic Distortion + Noise	$A_V = 1$ , $V_O = 3V_{BMS}$ , $R_L = 1k\Omega$			
THD+N		f = 1kHz	0.00001	0.00002	% (max)
		f = 20kHz	0.00003		%
IMD	Later and Latine Biotection	$A_V = 1$ , $V_O = 3V_{RMS}$			
טואוט	Intermodulation Distortion	Two-tone 60Hz & 7kHz 4:1	0.000017		%
GBWP	Gain Bandwith Product	$A_V = 10^4, R_L = 2k\Omega, f = 90kHz$	110		MHz
FPBW	Full Power Bandwidth	$A_V = -1, V_O = 20V_{PP}, R_L = 1k\Omega$	291		kHz
	Slew Rate	$A_{V} = -1, V_{O} = 20V_{PP}$			
SR		$R_{L} = 1k\Omega$	22	16.5	V/µs (min)
		$A_{V} = -1, V_{\Omega} = 10V_{PP}, R_{I} = 1k\Omega$			
t <sub>s</sub>	Settling time	0.01%	590		ns
		$V_O = \pm 10V$			
		$R_1 = 2k\Omega$	135	120	dB (min)
A <sub>VOL</sub>	Open-Loop Gain	T <sub>MIN</sub> – T <sub>MAX</sub>	124		dB
. 32		$R_1 = 600\Omega$	130	120	dB (min)
		T <sub>MIN</sub> – T <sub>MAX</sub>	122		ďΒ

	ol Parameter	Conditions	LME49990		
Symbol			Typical	Limit	Units
			(Note 6)	(Note 7)	(Limits)
NOISE					
	Input Noise Voltage Density	f = 10Hz	1.4		nV <b>/</b> √ <del>Hz</del>
•		f = 100Hz	1.0		nV <b>/</b> √ <del>Hz</del>
e <sub>N</sub>		f = 1kHz	0.88	1.3	nV/√Hz (max)
		f = 10kHz	0.88		nV/√ <del>Hz</del>
		BW = 0.1Hz to 10Hz ( <i>Note 4</i> )	30		nV <sub>PP</sub>
V_NOISE	SE RMS Voltage Noise	BW = 10Hz to 20kHz	0.12	0.2	μV (max)
		BW = 10Hz to 1MHz	1	1.2	μV (max)
i <sub>N</sub>	Input Current Noise Density	f = 1kHz	2.8		pA <b>/</b> √ <del>Hz</del>
INPUT CHA	RACTERISTICS	•			
V <sub>OS</sub>	Offset Voltage	$V_{CC} = \pm 18V, V_{CM} = 0v, V_{O} = 0V$	130	1000	μV (max)
V OS		$V_{CC} = \pm 18V, T_{MIN} - T_{MAX}$	300	2000	μV (max)
V <sub>OS</sub> Drift	Input Offset Voltage Drift vs	$V_{CC} = \pm 18V$ , $T_{MIN} - T_{MAX}$	2		μV/°C
VOS DIIIC	Temperature (ΔV <sub>OS</sub> /ΔTemp)	VCC - 110V, MIN MAX			μν/ Ο
1	Input Bias Current	$V_{CC} = \pm 18V, V_{CM} = 0v, V_{O} = 0V$	30	500	nA (max)
I <sub>BIAS</sub>		$V_{CC} = \pm 18V, T_{MIN} - T_{MAX}$	150	1000	nA (max)
1	Input Offset Current	$V_{CC} = \pm 18V, V_{CM} = 0v, V_{O} = 0V$	35	400	nA (max)
los		$V_{CC} = \pm 18V, T_{MIN} - T_{MAX}$	95	1000	nA (max)
V <sub>IN-CM</sub>	Common-Mode Input Voltage Range		12	11	V (min)
CMRR	Common-Mode Rejection	-10V <v<sub>CM&lt;10V</v<sub>	137	118	dB (min)
CIVIRR		T <sub>MIN</sub> – T <sub>MAX</sub>	132	110	dB (min)
OUTPUT CH	HARACTERISTICS				
	Output Voltage Swing	$V_{CC} = \pm 15V, R_L = 2k\Omega$	±13	12.5	V (min)
$V_{OUT}$		$V_{CC} = \pm 15V, R_{L} = 600\Omega$	±13	12	V (min)
		$V_{CC} = \pm 18V, R_L = 600\Omega$	±16	14.0	V (min)
I <sub>SHIRT</sub>	Output Short-Circuit Current	V <sub>CC</sub> = ±18V	+75/-70	+55/-50	mA (min)
I <sub>OUT</sub>	Output Current	$V_{CC} = \pm 18V, R_L = 600\Omega$	26	24	mA (min)

**Note 1:** "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

**Note 2:** The *Electrical Characteristics* tables list guaranteed specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not guaranteed.

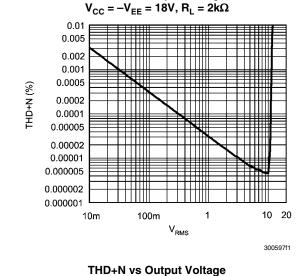
- Note 3: Amplifier output connected to GND, any number of amplifiers within a package.
- Note 4: Human body model, applicable std. JESD22-A114C.
- Note 5: Machine model, applicable std. JESD22-A115-A.
- Note 6: Typical values represent most likely parametric norms at  $T_A = +25$ °C, and at the *Recommended Operation Conditions* at the time of product characterization and are not guaranteed.
- Note 7: Datasheet min/max specification limits are guaranteed by test or statistical analysis.
- Note 8: Charge device model, applicable std JESD22-C101-A.

### **Typical Performance Characteristics**

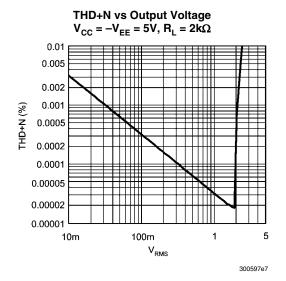
THD+N vs Output Voltage

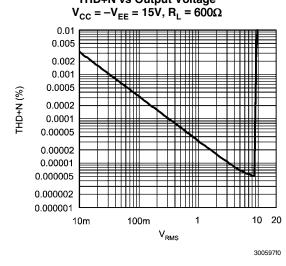
#### $V_{CC} = -V_{EE} = 15V$ , $R_L = 2k\Omega$ 0.01 0.005 0.002 Ш 0.001 0.0005 (%) N+QH1 0.0002 0.0001 0.00005 0.00002 0.00001 0.000005 0.000002 0.000001 10 20 10m 100m $V_{RMS}$

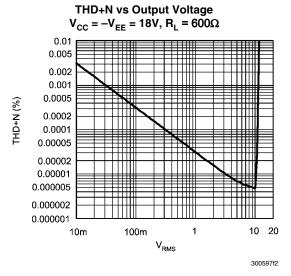
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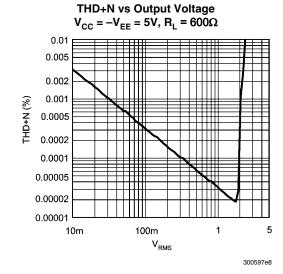


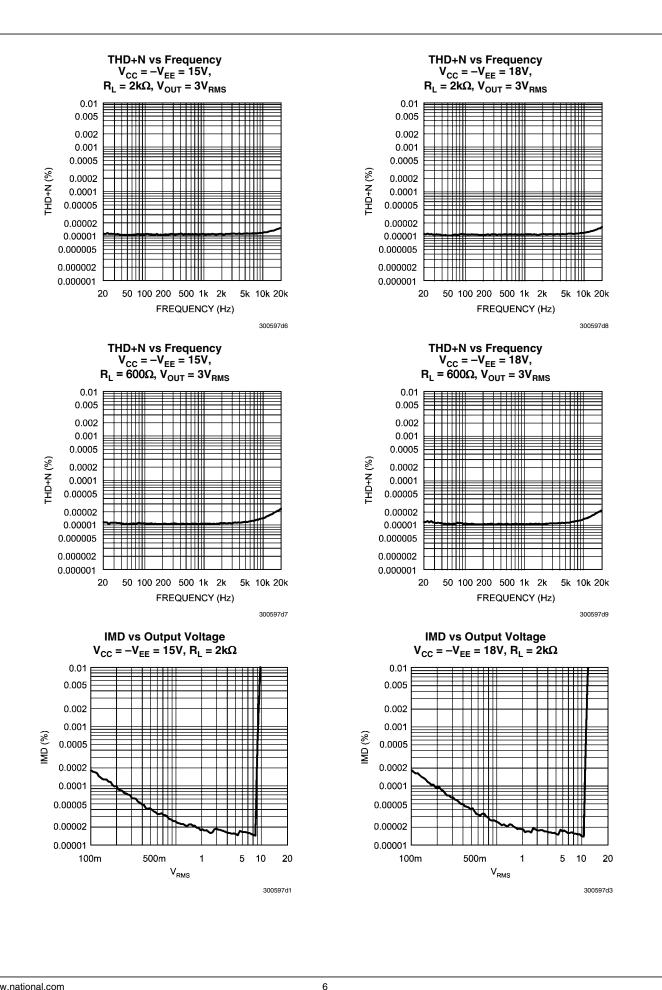
THD+N vs Output Voltage

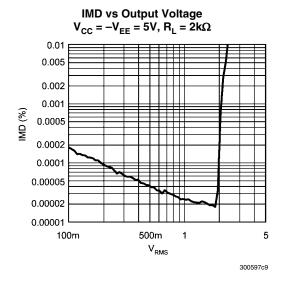


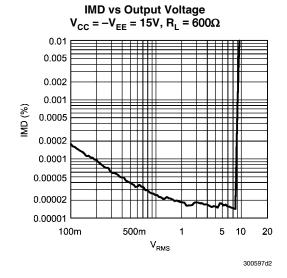


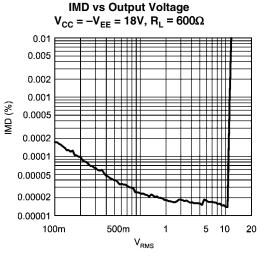


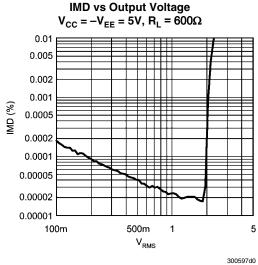


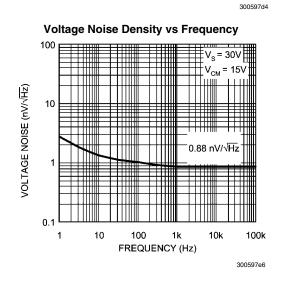


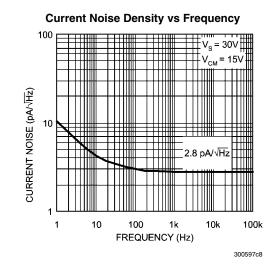


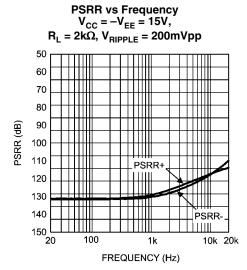




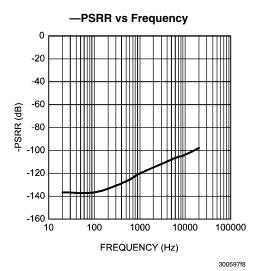




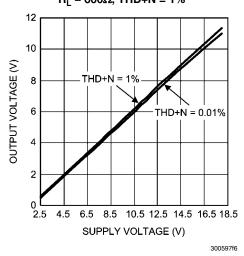




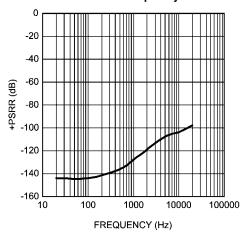
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Output Voltage vs Supply Voltage  $R_L = 600\Omega$ , THD+N = 1%

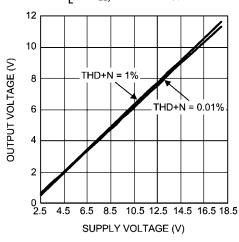


+PSRR vs Frequency

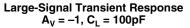


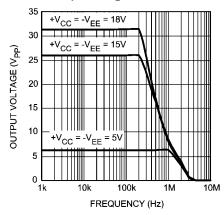
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# Output Voltage vs Supply Voltage $R_L = 2k\Omega$ , THD+N = 1%



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8

### **Application Hints**

#### **OUTPUT DRIVE AND STABILITY**

The LME49990 is unity gain stable from both input (both stable when gain = -1 or gain = 1). It able to drive resistive load  $600\Omega$  with output circuit with a typical 27mA. Capacitive loads up to 100pF will cause little change in the phase characteristics of the amplifiers and are therefore allowable.

Capacitive loads greater than 100pF must be isolated from the output. The most straight forward way to do this is to put a resistor in series with the output. This resistor will also prevent excess power dissipation if the output is accidentally shorted.

The effective load impedance (including feedback resistance) should be kept above  $600\Omega$  for fast settling. Load capacitance should also be minimized if good settling time is to be optimized. Large feedback resistors will make the circuit more susceptible to stray capacitance, so in high-speed applications keep the feedback resistors in the  $1k\Omega$  to  $2~k\Omega$  range whenever practical.

#### **OUTPUT COMPENSATION**

In most of the audio applications, the device will be operated in a room temperature and compensation networks are not necessary. However, the consideration of output network as shown in Figure 3 may be taken into account for some of the high performance audio applications such as high speed data conversion or when operating in a relatively low junction temperature. The compensation network will also provide a small improvement in settling time for the response time demanding applications.

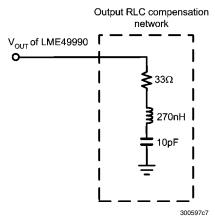


FIGURE 3. LME4990 Output Compensation Network

#### SUPPLY BYPASSING

To achieve a low noise and high-speed audio performance, power supply bypassing is extremely important. Applying multiple bypass capacitors is highly recommended. From experiment results, a  $10\mu F$  tantalum,  $2.2\mu F$  ceramic, and a  $0.47\mu F$  ceramic work well. All bypass capacitors leads should be very short. The ground leads of capacitors should also be separated to reduce the inductance to ground. To obtain the best result, a large ground plane layout technique is recommended and it was applied in the LME49990 evaluation board.

# **Typical Applications**

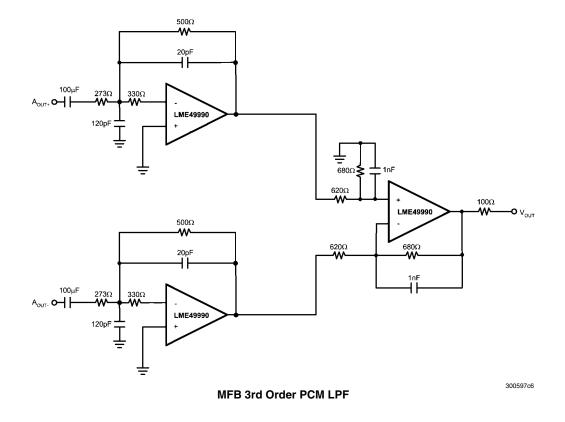
### **Balanced Input Mic Amp** R3 R4 10k 10k LME49990 R2 10k R1 200 R5 LME49990 10k R6 10k 10k LME49990

30059743

If R2 = R5, R3 = R6, R4 = R7  

$$V0 = \left(1 + \frac{2R2}{R1}\right) \frac{R4}{R3} (V2 - V1)$$

Illustration is: V0 = 101(V2 - V1)



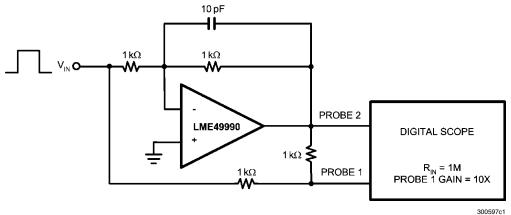
### **Application Information**

#### **SETTLING TIME AND SLEW RATE MEASUREMENTS**

The settling time of LME49990 may be verified using the test circuit in Figure 6. The LME49990 is connected for inverting operation, and the output voltage is summed with the input voltage step. When the LME49990's output voltage is equal to the input voltage, the voltage on the PROBE 1 will be zero. Any voltage appearing at this point will represent an error. And the settling time is equal to the time required for the error signal displayed on the oscilloscope to decay to less than one-half the necessary accuracy (See Settling Time — Output Swing photo). For a 10V input signal, settling time to 0.01% (1mV) will occur when the displayed error is less than 0.5mV. Since settling time is strongly dependent on slew rate, settling will be faster for smaller signal swings. The LME49990's inverting slew rate is faster than its non-inverting slew rate, so settling will be faster for inverting applications, as well.

It is important to note that the oscilloscope input amplifier may be overdriven during a settling time measurement, so the oscilloscope must be capable of recovering from overdrive very quickly. The signal generator used for this measurement must be able to drive  $50\Omega$  with a very clean  $\pm 10 V_{PP}$  square wave.

The Slew Rate of LME49990 tells how fast it responses to a transient or a step input. It may be measured by the test circuit in Figure 7. The Slew Rate of LME49990 is specified in closeloop gain = -1 when the output driving a  $1 k\Omega$  load at  $20 V_{PP}$ . The LME49990 behaves very stable in shape step response and have a minimal ringing in both small and large signal step response (See Typical Performance Characteristic). The slew rate typical value reach as high as  $\pm 18 V/\mu S$  was measured when the output reach -20V refer to the start point when input voltage equals to zero.



**FIGURE 6: Settling Time Test Circuit** 

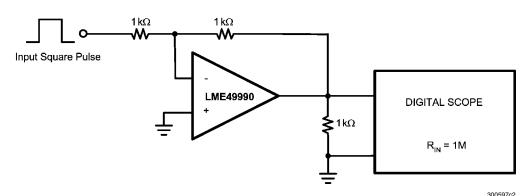


FIGURE 7: Slew Rate Test Circuit

#### **DISTORTION MEASUREMENTS**

The vanishingly low residual distortion produced by LME49990 is below the capabilities of all commercially available equipment. This makes distortion measurements just slightly more difficult than simply connecting a distortion meter to the amplifier's inputs and outputs. The solution, however, is quite simple: an additional resistor. Adding this resistor extends the resolution of the distortion measurement equipment.

The LME49990's low residual distortion is an input referred internal error. As shown in Figure 8, adding the  $10\Omega$  resistor connected between the amplifier's inverting and non-inverting inputs changes the amplifier's noise gain. The result is that

the error signal (distortion) is amplified by a factor of 101. Although the amplifier's closed-loop gain is unaltered, the feedback available to correct distortion errors is reduced by 101, which means that measurement resolution increases by 101. To ensure minimum effects on distortion measurements, keep the value of R1 low as shown in Figure 8.

This technique is verified by duplicating the measurements with high closed loop gain and/or making the measurements at high frequencies. Doing so produces distortion components that are within the measurement equipment's capabilities. This datasheet's THD+N and IMD values were generated using the above described circuit connected to an Audio Precision System Two Cascade.

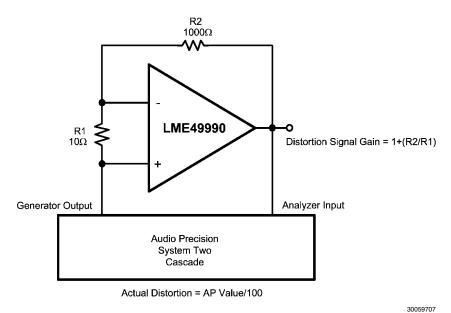


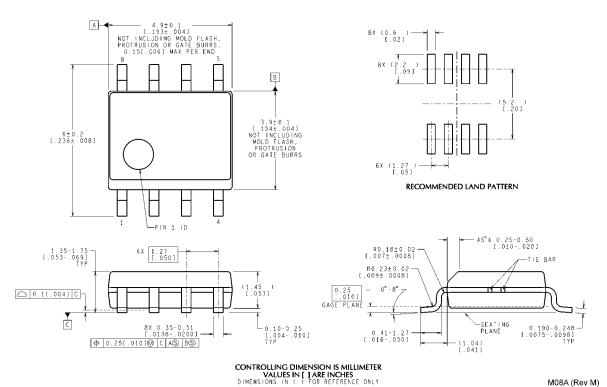
FIGURE 8: THD+N and IMD Distortion Test Circuit

12

# **Revision History**

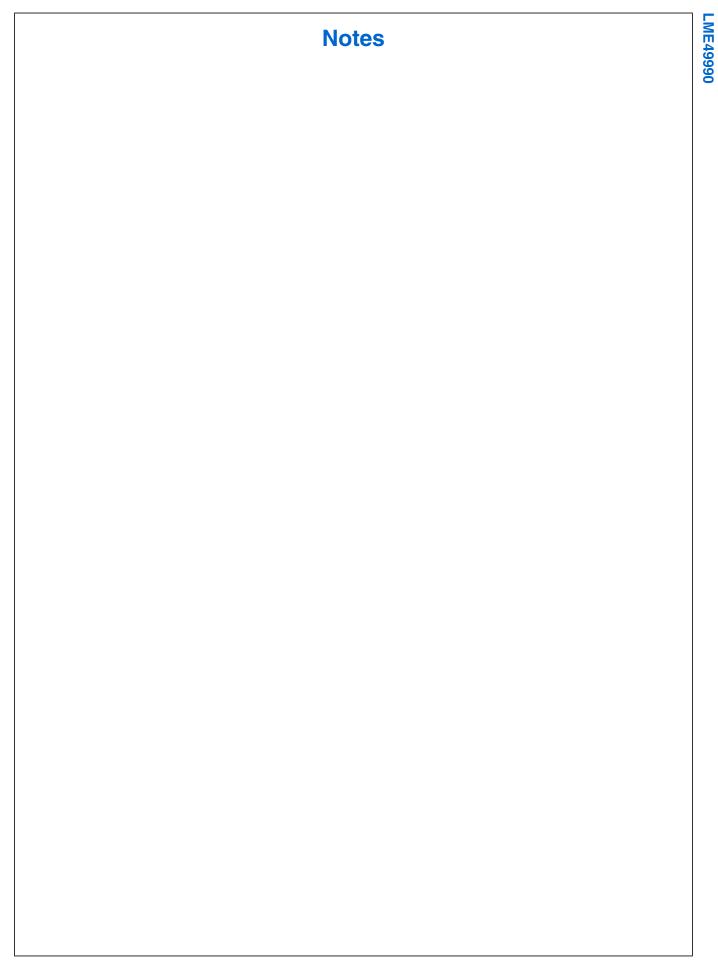
Rev	Date	Description
1.0	12/16/09	Initial released.
1.01	01/08/10	Input text edits.

### Physical Dimensions inches (millimeters) unless otherwise noted



Dual-In-Line Package Order Number LME49990MA NS Package Number M08A

14



#### **Notes**

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Voltage References	www.national.com/vref	Design Made Easy	www.national.com/easy	
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