74AUP1T97

Low-power configurable gate with voltage-level translator Rev. 01 — 25 October 2007 Product data s

Product data sheet

1. **General description**

The 74AUP1T97 provides low-power, low-voltage configurable logic gate functions. The output state is determined by eight patterns of 3-bit input. The user can choose the logic functions MUX, AND, OR, NAND, NOR, inverter and buffer. All inputs can be connected to V_{CC} or GND.

This device ensures a very low static and dynamic power consumption across the entire V_{CC} range from 2.3 V to 3.6 V.

The 74AUP1T97 is designed for logic-level translation applications with input switching levels that accept 1.8 V low-voltage CMOS signals, while operating from either a single 2.5 V or 3.3 V supply voltage.

The wide supply voltage range ensures normal operation as battery voltage drops from 3.6 V to 2.3 V.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

Schmitt trigger inputs make the circuit tolerant to slower input rise and fall times across the entire V_{CC} range.

Features 2.

- Wide supply voltage range from 2.3 V to 3.6 V
- High noise immunity
- ESD protection:
 - HBM JESD22-A114E Class 3A exceeds 5000 V
 - MM JESD22-A115-A exceeds 200 V
 - CDM JESD22-C101C exceeds 1000 V
- Low static power consumption; $I_{CC} = 1.5 \mu A$ (maximum)
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C



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3. Ordering information

Table 1. Ordering information

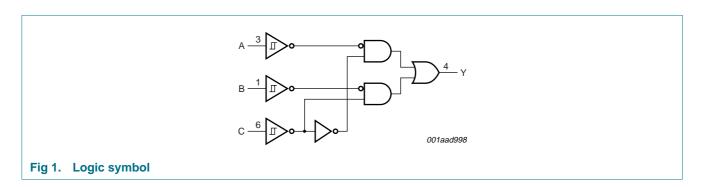
Type number	Package							
	Temperature range	Name	Description	Version				
74AUP1T97GW	–40 °C to +125 °C	SC-88	plastic surface-mounted package; 6 leads	SOT363				
74AUP1T97GM	–40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 \times 1.45 \times 0.5 mm	SOT886				
74AUP1T97GF	–40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 \times 1 \times 0.5 mm	SOT891				

4. Marking

Table 2. Marking

Type number	Marking code
74AUP1T97GW	59
74AUP1T97GM	59
74AUP1T97GF	59

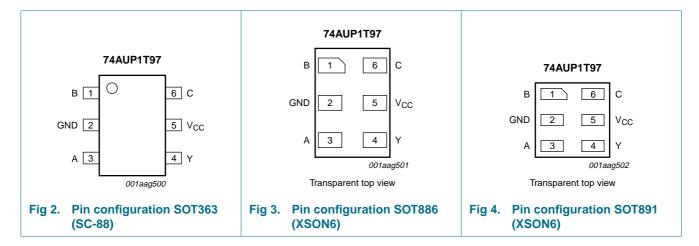
5. Functional diagram



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6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
В	1	data input
GND	2	ground (0 V)
A	3	data input
Υ	4	data output
V _{CC}	5	supply voltage
С	6	data input

7. Functional description

Table 4. Function table[1]

Input			Output
С	В	A	Υ
L	L	L	L
L	L	Н	L
L	Н	L	Н
L	Н	Н	Н
Н	L	L	L
Н	L	Н	Н
Н	Н	L	L
Н	Н	Н	Н

^[1] H = HIGH voltage level;

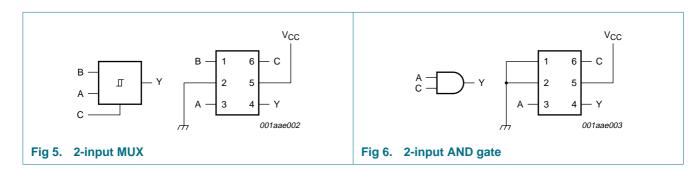
L = LOW voltage level.

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7.1 Logic configurations

Table 5. Function selection table

Logic function	Figure
2-input MUX	see Figure 5
2-input AND	see Figure 6
2-input OR with one input inverted	see Figure 7
2-input NAND with one input inverted	see Figure 7
2-input AND with one input inverted	see Figure 8
2-input NOR with one input inverted	see Figure 8
2-input OR	see Figure 9
Inverter	see Figure 10
Buffer	see Figure 11



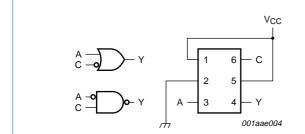


Fig 7. 2-input NAND gate with input A inverted or 2-input OR gate with input C inverted

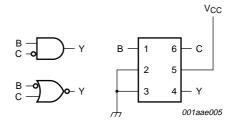
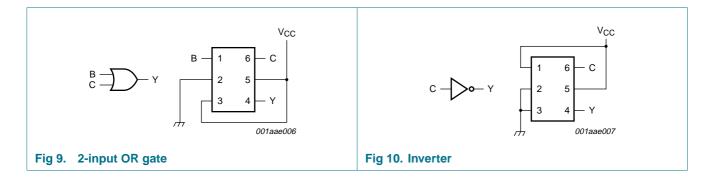
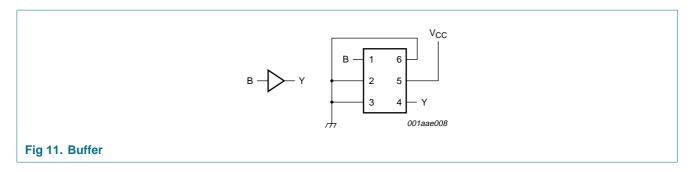


Fig 8. 2-input NOR gate with input B inverted or 2-input AND gate with input C inverted



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8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0 V$	-50	-	mA
V_{I}	input voltage		[<u>1</u>] –0.5	+4.6	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0 V$	-50	-	mA
V_{O}	output voltage	Active mode and Power-down mode	[<u>1</u>] –0.5	+4.6	V
I _O	output current	$V_O = 0 V \text{ to } V_{CC}$	-	±20	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$	[2] _	250	mW

^[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

9. Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		2.3	3.6	V
VI	input voltage		0	3.6	V
Vo	output voltage	Active mode	0	V_{CC}	V
		Power-down mode; V _{CC} = 0 V	0	3.6	V
T _{amb}	ambient temperature		-40	+125	°C

^[2] For SC-88 package: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K. For XSON6 packages: above 45 °C the value of P_{tot} derates linearly with 2.4 mW/K.

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10. Static characteristics

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$T_{amb} = 2$	5 °C					
V_{T+}	positive-going threshold	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0.60	-	1.10	V
	voltage	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	0.75	-	1.16	V
V_{T-}	negative-going threshold	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0.35	-	0.60	V
	voltage	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	0.50	-	0.85	V
V _H	hysteresis voltage	$(V_H = V_{T+} - V_{T-})$				
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0.23	-	0.60	V
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	0.25	-	0.56	V
V _{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -20 \mu A$; $V_{CC} = 2.3 \text{ V to } 3.6 \text{ V}$	V _{CC} - 0.1	-	-	V
		$I_{O} = -2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	2.05	-	-	V
		$I_{O} = -3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.9	-	-	V
		$I_{O} = -2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.72	-	-	V
		$I_{O} = -4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.6	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20 \mu A$; $V_{CC} = 2.3 \text{ V to } 3.6 \text{ V}$	-	-	0.10	V
		$I_O = 2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.31	V
		$I_O = 3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.44	V
		$I_O = 2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.31	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.44	V
l _l	input leakage current	$V_I = GND$ to 3.6 V; $V_{CC} = 0$ V to 3.6 V	-	-	±0.1	μΑ
I _{OFF}	power-off leakage current	V_I or $V_O = 0$ V to 3.6 V; $V_{CC} = 0$ V	-	-	±0.1	μΑ
ΔI_{OFF}	additional power-off leakage current	V_1 or $V_0 = 0$ V to 3.6 V; $V_{CC} = 0$ V to 0.2 V	-	-	±0.2	μΑ
I _{CC}	supply current	$V_I = GND \text{ or } V_{CC}; I_O = 0 \text{ A};$ $V_{CC} = 2.3 \text{ V to } 3.6 \text{ V}$	-	-	1.2	μΑ
Cı	input capacitance	V_{CC} = 0 V to 3.6 V; V_I = GND or V_{CC}	•	0.8	-	pF
Co	output capacitance	$V_O = GND$; $V_{CC} = 0 V$	-	1.7	-	pF
T _{amb} = -	40 °C to +85 °C					
V_{T+}	positive-going threshold	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0.60	-	1.10	V
	voltage	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	0.75	-	1.19	V
V_{T-}	negative-going threshold	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0.35	-	0.60	V
	voltage	V _{CC} = 3.0 V to 3.6 V	0.50	-	0.85	V
V_{H}	hysteresis voltage	$(V_H = V_{T+} - V_{T-})$				
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0.10	-	0.60	V
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	0.15	-	0.56	V

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Table 8. Static characteristics ...continued
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Uni
V _{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_{O} = -20 \mu A$; $V_{CC} = 2.3 \text{ V to } 3.6 \text{ V}$	V _{CC} - 0.1	-	-	V
		$I_{O} = -2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.97	-	-	V
		$I_{O} = -3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.85	-	-	V
		$I_{O} = -2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.67	-	-	V
		$I_{O} = -4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.55	-	-	V
V _{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20 \mu\text{A}; V_{CC} = 2.3 \text{V} \text{ to } 3.6 \text{V}$	-	-	0.1	V
		$I_O = 2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.33	V
		$I_O = 3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.45	V
		$I_O = 2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.33	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$		-	0.45	V
ı	input leakage current	$V_I = GND$ to 3.6 V; $V_{CC} = 0$ V to 3.6 V	-	-	±0.5	μΑ
OFF	power-off leakage current	V_I or $V_O = 0$ V to 3.6 V; $V_{CC} = 0$ V	-	-	±0.5	μΑ
ΔI_{OFF}	additional power-off leakage current	V_1 or $V_0 = 0$ V to 3.6 V; $V_{CC} = 0$ V to 0.2 V	-	-	±0.5	μΑ
cc	supply current	V_I = GND or V_{CC} ; I_O = 0 A; V_{CC} = 2.3 V to 3.6 V	-	-	1.5	μΑ
∆l _{CC}	additional supply current	V_{CC} = 2.3 V to 2.7 V; I_O = 0 A	<u>[1]</u> -	-	4	μΑ
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}; I_{O} = 0 \text{ A}$	[2] -	-	12	μΑ
Γ _{amb} = -	40 °C to +125 °C					
V _{T+}	positive-going threshold	V _{CC} = 2.3 V to 2.7 V	0.60	-	1.10	V
	voltage	V _{CC} = 3.0 V to 3.6 V	0.75	-	1.19	V
V_{T-}	negative-going threshold	V _{CC} = 2.3 V to 2.7 V	0.33	-	0.64	V
	voltage	V _{CC} = 3.0 V to 3.6 V	0.46	-	0.85	V
V_{OH}	hysteresis voltage	$(V_H = V_{T+} - V_{T-})$				
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0.10	-	0.60	V
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	0.15	-	0.56	V
V _{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_{O} = -20 \mu A$; $V_{CC} = 2.3 \text{ V to } 3.6 \text{ V}$	V _{CC} - 0.11	-	-	V
		$I_{O} = -2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.77	-	-	V
		$I_{O} = -3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.67	-	-	V
		$I_{O} = -2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.40	-	-	V
		$I_O = -4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.30	-	-	V
V _{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20 \mu\text{A}; V_{CC} = 2.3 \text{V} \text{ to } 3.6 \text{V}$	-	-	0.11	V
		$I_O = 2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.36	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.50	V
		$I_{O} = 2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.36	V
		$I_{O} = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.50	V
ı	input leakage current	$V_1 = GND \text{ to } 3.6 \text{ V}; V_{CC} = 0 \text{ V to } 3.6 \text{ V}$	-	-	±0.75	μΑ
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 Table 8.
 Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
I _{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.75	μΑ
ΔI_{OFF}	additional power-off leakage current	V_1 or $V_0 = 0$ V to 3.6 V; $V_{CC} = 0$ V to 0.2 V	-	-	±0.75	μΑ
I _{CC}	supply current	V_I = GND or V_{CC} ; I_O = 0 A; V_{CC} = 2.3 V to 3.6 V	-	-	3.5	μΑ
ΔI_{CC}	additional supply current	V_{CC} = 2.3 V to 2.7 V; I_O = 0 A	<u>[1]</u> -	-	7	μΑ
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V; } I_{O} = 0 \text{ A}$	[2] _	-	22	μΑ

^[1] One input at 0.3 V or 1.1 V, other input at V_{CC} or GND.

11. Dynamic characteristics

Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see <u>Figure 13</u>.

Symbol	Parameter	Conditions	25 °C			–40 °C to +125 °C			Unit	
				Min	Typ[1]	Max	Min	Max (85 °C)	Max (125 °C)	
$V_{CC} = 2.3$	3 V to 2.7 V; V _I = 1.6	55 V to 1.95 V					'		'	
t _{pd}	propagation delay	A, B, C to Y; see Figure 12	[2]							
		$C_L = 5 pF$		2.2	3.5	5.5	0.5	6.8	7.5	ns
		C _L = 10 pF		2.6	4.1	6.3	1.0	7.9	8.7	ns
		C _L = 15 pF		2.9	4.6	6.9	1.0	8.7	9.6	ns
		C _L = 30 pF		3.7	5.8	8.4	1.5	10.8	11.9	ns
V _{CC} = 2.3	3 V to 2.7 V; V _I = 2.3	3 V to 2.7 V								
t _{pd}	propagation delay	A, B, C to Y; see Figure 12	[2]							
		C _L = 5 pF		1.8	3.4	5.5	0.5	6.0	6.6	ns
		C _L = 10 pF		2.2	4.0	6.2	1.0	7.1	7.9	ns
		C _L = 15 pF		2.5	4.4	6.8	1.0	7.9	8.7	ns
		C _L = 30 pF		3.2	5.6	8.3	1.5	10.0	11.0	ns
V _{CC} = 2.3	3 V to 2.7 V; V _I = 3.0) V to 3.6 V								
t _{pd}	propagation delay	A, B, C to Y; see Figure 12	[2]							
		$C_L = 5 pF$		1.4	3.1	5.0	0.5	5.5	6.1	ns
		C _L = 10 pF		1.8	3.7	5.7	1.0	6.5	7.2	ns
		C _L = 15 pF		2.2	4.2	6.3	1.0	7.4	8.2	ns
		C _L = 30 pF		2.9	5.3	7.9	1.5	9.5	10.5	ns
$V_{CC} = 3.0$	0 V to 3.6 V; V _I = 1.6	65 V to 1.95 V								
t _{pd}	propagation delay	A, B, C to Y; see Figure 12	[2]							
		C _L = 5 pF		2.1	2.9	3.9	0.5	8.0	8.8	ns
		C _L = 10 pF		2.5	3.4	4.6	1.0	8.5	9.4	ns
		C _L = 15 pF		2.9	3.9	5.2	1.0	9.1	10.1	ns
		C _L = 30 pF		3.6	5.0	6.7	1.5	9.8	10.8	ns

^[2] One input at 0.45 V or 1.2 V, other input at V_{CC} or GND.

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 Table 9.
 Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 13.

Symbol	Parameter	Conditions		25 °C			–40 °C to +125 °C		
			Min	Typ[1]	Max	Min	Max (85 °C)	Max (125 °C)	
$V_{CC} = 3.0$	0 V to 3.6 V; V _I = 2.3	3 V to 2.7 V		'			'	•	
t _{pd}	propagation delay	A, B, C to Y; see Figure 12	1						
		C _L = 5 pF	1.7	2.8	4.2	0.5	5.3	5.9	ns
		C _L = 10 pF	2.1	3.4	5.0	1.0	6.1	6.8	ns
		C _L = 15 pF	2.4	3.8	5.6	1.0	6.8	7.5	ns
		$C_L = 30 \text{ pF}$	3.2	5.0	7.1	1.5	8.5	9.4	ns
$V_{CC} = 3.0$	0 V to 3.6 V; V _I = 3.0) V to 3.6 V							
t _{pd}	propagation delay	A, B, C to Y; see Figure 12	1						
		C _L = 5 pF	1.4	2.7	4.2	0.5	4.7	5.2	ns
		C _L = 10 pF	1.8	3.3	5.0	1.0	5.7	6.3	ns
		C _L = 15 pF	2.1	3.8	5.6	1.0	6.2	6.9	ns
		$C_L = 30 pF$	2.9	4.9	7.1	1.5	7.8	8.6	ns
$T_{amb} = 2$	5 °C								
C_{PD}	power dissipation	$f_i = 1 \text{ MHz}$; $V_I = \text{GND to } V_{CC}$	1						
	capacitance	V_{CC} = 2.3 V to 2.7 V	-	3.6	-	-	-	-	pF
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	-	4.3	-	-	-	-	pF

^[1] All typical values are measured at nominal V_{CC}.

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

 f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

 V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

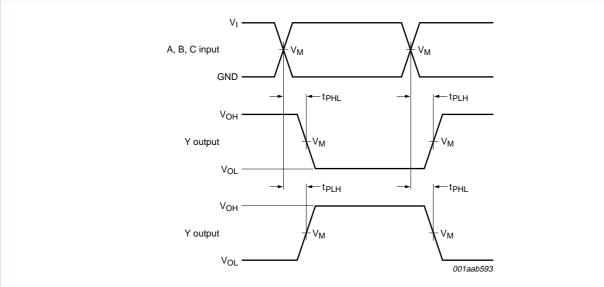
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^[2] t_{pd} is the same as t_{PLH} and t_{PHL}

^[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

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12. Waveforms



Measurement points are given in Table 10.

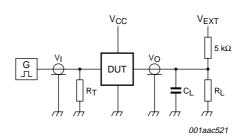
 $\ensuremath{V_{OL}}$ and $\ensuremath{V_{OH}}$ are typical output voltage drop that occur with the output load.

Fig 12. Input A, B and C to output Y propagation delay times.

Table 10. Measurement points

Supply voltage	Output	Input		
V _{CC}	V _M	V _M	V _I	$t_r = t_f$
2.3 V to 3.6 V	0.5V _{CC}	0.5V _I	1.65 V to 3.6 V	≤ 3.0 ns

Low-power configurable gate with voltage-level translator



Test data is given in Table 11.

Definitions for test circuit:

R_L = Load resistance.

 C_L = Load capacitance including jig and probe capacitance.

 R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

 V_{EXT} = External voltage for measuring switching times.

Fig 13. Load circuitry for switching times

Table 11. Test data

Supply voltage	Load		V _{EXT}		
V _{CC}	CL	R _L [1]	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}
2.3 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 k Ω or 1 M Ω	open	GND	$2 \times V_{CC}$

[1] For measuring enable and disable times R_L = 5 $k\Omega$, for measuring propagation delays, setup and hold times and pulse width R_L = 1 $M\Omega$.

Low-power configurable gate with voltage-level translator

13. Package outline

Plastic surface-mounted package; 6 leads

SOT363

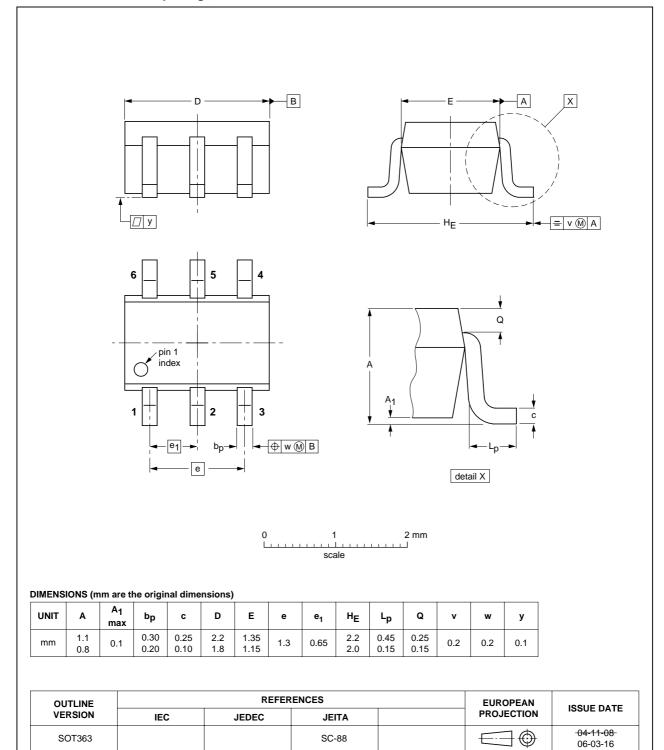


Fig 14. Package outline SOT363 (SC-88)

Low-power configurable gate with voltage-level translator

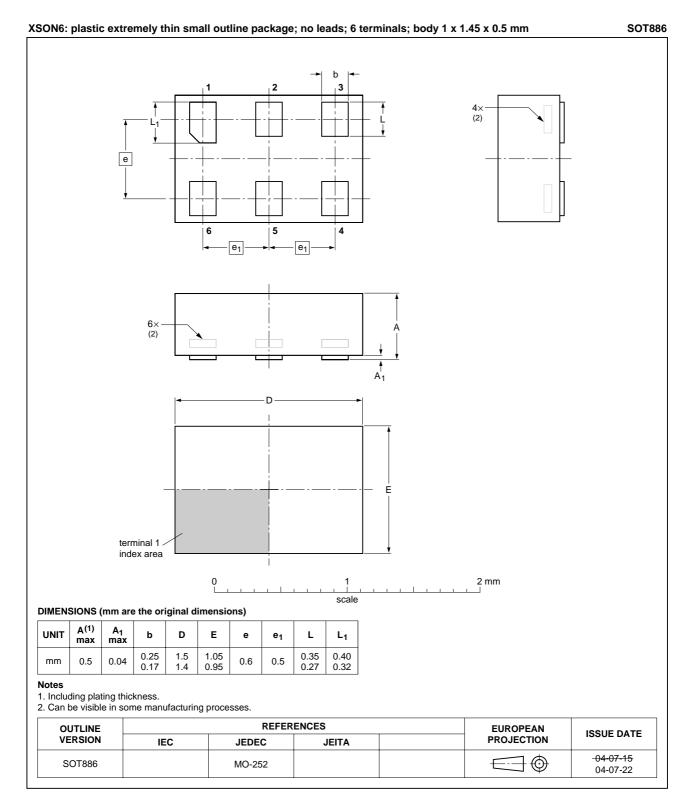


Fig 15. Package outline SOT886 (XSON6)

Low-power configurable gate with voltage-level translator

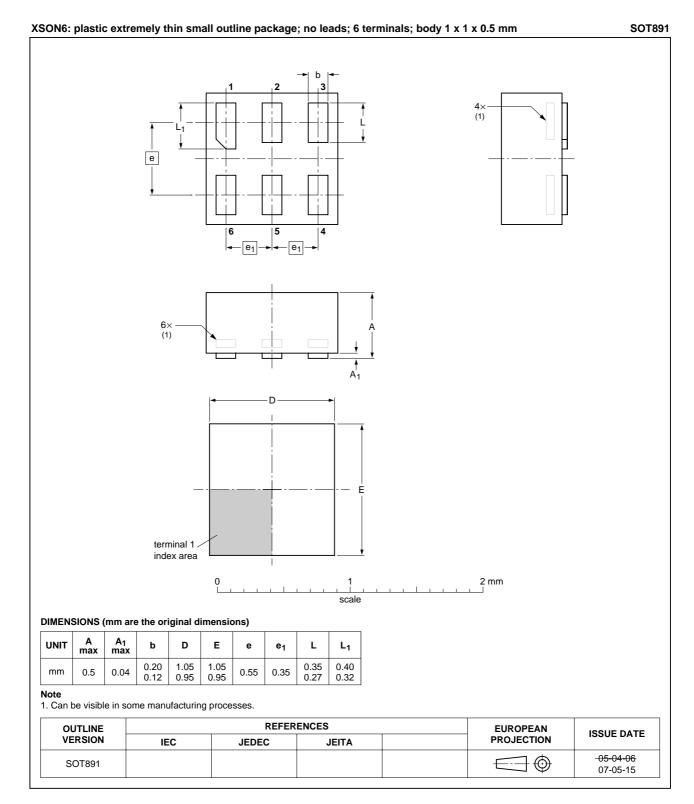


Fig 16. Package outline SOT891 (XSON6)

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14. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP1T97_1	20071025	Product data sheet	-	-

Low-power configurable gate with voltage-level translator

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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