

DM74LS395 4-Bit Shift Register with TRI-STATE® Outputs

General Description

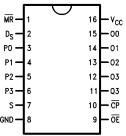
The LS395 is a 4-bit shift register with TRI-STATE outputs and can operate in either a synchronous parallel load or a serial shift-right mode, as determined by the Select input. An asynchronous active LOW Master Reset ($\overline{\text{MR}}$) input overrides the synchronous operations and clears the register. An active LOW Output Enable ($\overline{\text{OE}}$) input controls the TRI-STATE output buffers, but does not interfere with the other operations. The fourth stage also has a conventional output for linking purposes in multi-stage serial operations.

Features

- Shift right or parallel 4-bit register
- TRI-STATE outputs
- Input clamp diodes limit high speed termination effects
- Fully CMOS and TTL compatible

Connection Diagram

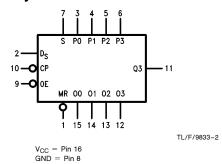
Dual-In-Line Package



TL/F/9833-1

Order Number DM74LS395WM or DM74LS395N See NS Package Number M16B or N16E

Logic Symbol



Mode Select Table

Operating Mode	Inputs @ t _n					Outputs @ t _{n+1}			
Operating mode	MR	СP	s	Ds	Pn	00	01	02	О3
Asynchronous Reset Shift, SET First Stage	L H	×	X L	X H	X X	L H	L O0 _n	L O1 _n	L 02 _n
Shift, RESET First Stage Parallel Load	тт	//	LH	L X	X Pn	L P0	O0 _n P1	O1 _n P2	02 _n P3

 $t_n, \, t_{n+1} = \text{Time before and after CP HIGH-to-LOW transition}$

H = HIGH Voltage Level
L = LOW Voltage Level

X = Immaterial

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Absolute Maximum Ratings (Note)

Supply Voltage 7V Input Voltage 7V 0°C to +70°C Operating Free Air Temperature Range Storage Temperature Range -65° C to $+150^{\circ}$ C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V _{CC}	Supply Voltage	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			V
V _{IL}	Low Level Input Voltage			0.8	V
ГОН	High Level Output Current			-0.4	mA
l _{OL}	Low Level Output Current			8	mA
T _A	Free Air Operating Temperature	0		70	°C
t _s (H) t _s (L)	Setup Time HIGH or LOW S, D _S or P _n to CP	20 20			ns
t _h (H) t _h (L)	Hold Time HIGH or LOW S, D _S or P _n to $\overline{\text{CP}}$	5 5			ns
t _w (L)	CP Pulse Width LOW	18			ns
t _w (L)	MR Pulse Width LOW	20			ns

Electrical Characteristics Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
VI	Input Clamp Voltage	$V_{CC} = Min, I_I = -18 \text{ mA}$			-1.5	V
V _{OH}	High Level Output Voltage	$V_{CC} = Min, I_{OH} = Max$ $V_{IL} = Max$	2.7			V
V _{OL}	Low Level Output Voltage	$V_{CC} = Min, I_{OL} = Max$ $V_{IH} = Min$		0.35	0.5	V
		I _{OL} = 4 mA, V _{CC} = Min		0.25	0.4	
II	Input Current @ Max Input Voltage	$V_{CC} = Max, V_I = 7V$			0.1	mA
I _{IH}	High Level Input Current	$V_{CC} = Max, V_I = 2.7V$			20	μΑ
I _{IL}	Low Level Input Current	$V_{CC} = Max, V_I = 0.4V$			-0.4	mA
los	Short Circuit Output Current	V _{CC} = Max (Note 2)	-20		-100	mA
Icc	Supply Current with Outputs OFF	$V_{CC} = Max, \overline{OE}, D_S, S = 4.5V$ $\overline{CP} = \searrow, P_n = GND$			29	mA
	Supply Current with Outputs ON	$V_{CC} = Max, D_S, S = 4.5V$ $\overline{OE}, \overline{CP}, P_n = GND$			25	mA
I _{OZH}	TRI-STATE Output Off Current HIGH	$V_{CC} = V_{CCH}$ $V_{OZH} = 2.7V$			20	μΑ
l _{OZL}	TRI-STATE Output Off Current LOW	$V_{CC} = V_{CCH}$ $V_{OZL} = 0.4V$			-20	μΑ

Note 1: All typicals are at $V_{CC} = 5V$, $T_A = 25^{\circ}C$. Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics $V_{CC} = +5.0V, T_A = +25^{\circ}C$

Symbol	Parameter	$R_L = 2 k\Omega$	Units		
	T all alliester	Min	Max		
f _{max}	Maximum Shift Frequency	30		MHz	
t _{PLH} t _{PHL}	Propagation Delay CP to O _n		35 25	ns	
t _{PHL}	Propagation Delay MR to O _n		35	ns	
t _{PZH} t _{PZL}	Output Enable Time		20 20	ns	
t _{PHZ} t _{PLZ}	Output Disable Time		17 23	ns	

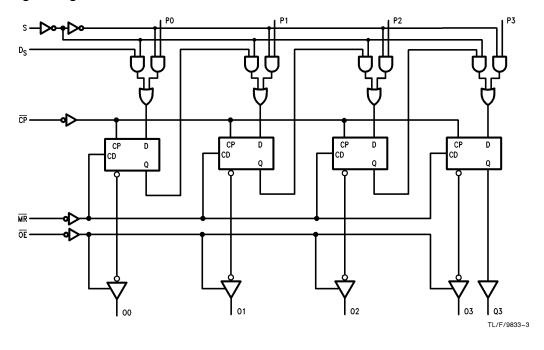
Functional Description

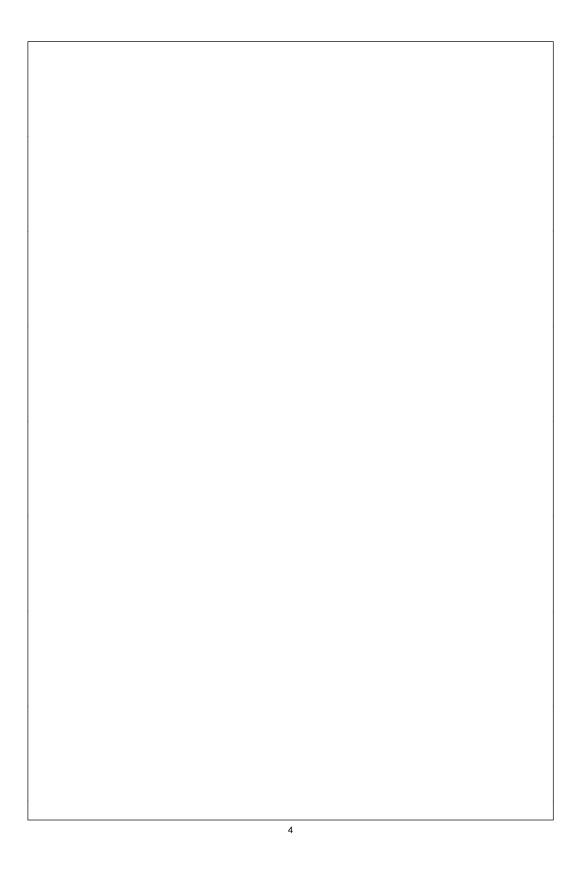
The 'LS395 contains four D-type edge-triggered flip-flops and auxiliary gating to select a D input either from a Parallel (P_n) input or from the preceding stage. When the Select input is HIGH, the P_n inputs are enabled. A LOW signal in the S input enables the serial inputs for shift-right operations, as indicated in the Truth Table.

State changes are initiated by HIGH-to-LOW transitions on the Clock Pulse (\overline{CP}) input. Signals on the P_n , D_S and Sinputs can change when the Clock is in either state, provided that the recommended setup and hold times are observed. When the S input is LOW, a $\overline{\mbox{CP}}$ HIGH-LOW trans sition transfers data in O0 to O1, O1 to O2, and O2 to O3. A left-shift is accomplished by connecting the outputs back to the P_n inputs, but offset one place to the left, i.e., O3 to P2, O2 to P1, and O1 to P0, with P3 acting as the linking input from another package.

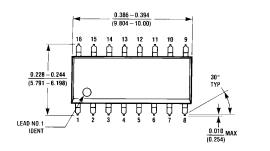
When the $\overline{\text{OE}}$ input is HIGH, the output buffers are disabled and the O0-O3 outputs are in a high impedance condition. The shifting, parallel loading or resetting operations can still be accomplished, however.

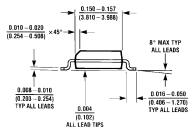
Logic Diagram

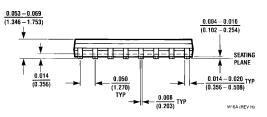






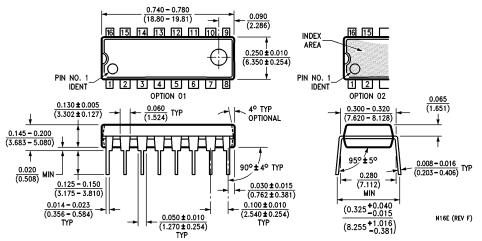






16-Lead Wide Small Outline Molded Package (M) Order Number DM74LS395WM NS Package Number M16B

Physical Dimensions inches (millimeters) (Continued)



16-Lead Molded Dual-In-Line Package (N) Order Number DM74LS395N NS Package Number N16E

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