**N**ational **S**emiconductor

May 1992

54LS192/DM74LS192 Up/Down Decade Counter with Separate Up/Down Clocks

General Description

The 'LS192 is an up/down BCD decade (8421) counter. Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs.

Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for a subsequent stage without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.
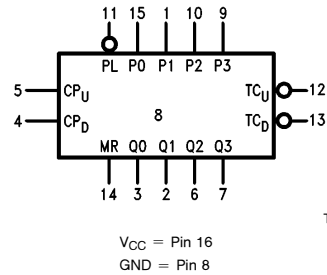
Connection Diagram

Dual-In-Line Package
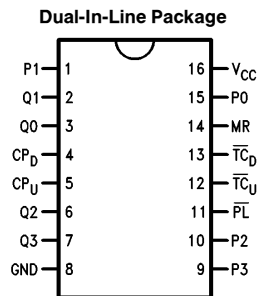
TL/F/10178–1

Order Number 54LS192DMQB, 54LS192FMQB, 54LS192LMQB, DM74LS192M or DM74LS192N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Logic Symbol

TL/F/10178–2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
CP_U	Count Up Clock Input (Active Rising Edge)
CP_D	Count Down Clock Input (Active Rising Edge)
MR	Asynchronous Master Reset Input (Active HIGH)
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
P0–P3	Parallel Data Inputs
Q0–Q3	Flip-Flop Outputs
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Active LOW)
$\overline{TC}_U$	Terminal Count Up (Carry) Output (Active LOW)

Mode Select Table

MR	$\overline{PL}$	CP_U	CP_D	Mode
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	╱	H	Count Up
L	H	H	╱	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	$-55°C$ to $+125°C$
DM74LS	$0°C$ to $+70°C$
Storage Temperature Range	$-65°C$ to $+150°C$

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS192			DM74LS192			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Voltage			-0.4			-0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	-55		125	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW Pn to $\overline{PL}$	20 20			20 10			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW Pn to $\overline{PL}$	3 3			3 3			ns
t_w (L)	CP Pulse Width LOW	17			17			ns
t_w (L)	$\overline{PL}$ Pulse Width LOW	20			20			ns
t_w (H)	MR Pulse Width HIGH	15			15			ns
t_{rec}	Recovery Time, MR to CP	3			3			ns
t_{rec}	Recovery Time, $\overline{PL}$ to CP	10			10			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} =$ Min, $I_I = -18$ mA				-1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} =$ Min, $I_{OH} =$ Max, $V_{IL} =$ Max	54LS	2.5			V
			DM74	2.7			
V_{OL}	Low Level Output Voltage	$V_{CC} =$ Min, $I_{OL} =$ Max,	54LS			0.4	V
		$V_{IH} =$ Min	DM74			0.5	
		$I_{OL} = 4$ mA, $V_{CC} =$ Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	$V_{CC} =$ Max, $V_I = 10$V $V_I = 7$V	DM54			0.1	mA
			DM74				
I_{IH}	High Level Input Current	$V_{CC} =$ Max, $V_I = 2.7$V				20	μA
I_{IL}	Low Level Input Current	$V_{CC} =$ Max, $V_I = 0.4$V				-0.4	mA
I_{OS}	Short Circuit Output Current	$V_{CC} =$ Max (Note 2)	54LS	-20		-100	mA
			DM74	-20		-100	
I_{CC}	Supply Current	$V_{CC} =$ Max, MR, $\overline{PL} =$ GND Other Inputs $= 4.5$V				31	mA

Note 1: All typicals are at $V_{CC} = 5$V, $T_A = 25°C$.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

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Switching Characterisitcs

$V_{CC} = +0.5V$, $T_A = +25°C$ (See Section 1 for waveforms and load configurations)

Symbol	Parameter	$R_L = 2k$ $C_L = 15$ pF		Units
		Min	Max	
f_{max}	Maximum Count Frequency	30		MHz
t_{PLH} t_{PHL}	Propagation Delay CP_U or CP_D to Q_n		31 28	ns
t_{PLH} t_{PHL}	Propagation Delay CP_U to $\overline{TC}_U$		16 21	ns
t_{PLH} t_{PHL}	Propagation Delay CP_D to $\overline{TC}_D$		16 24	
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n		20 30	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n		32 30	ns
t_{PHL}	Propagation Delay, MR to Q_n		25	

Functional Description

The '192 is an asynchronously presettable decade and 4-bit binary synchronous up/down (reversible) counter. The operating modes of the '192 decade counter and the '193 binary counter are identical, with the only difference being the count sequences as noted in the State Diagram. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up, and count down operations.

Each flip-flop contains JK feedback from slave to master such that a LOW-to-HIGH transition on its T input causes the slave, and thus the Q output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is LOW.
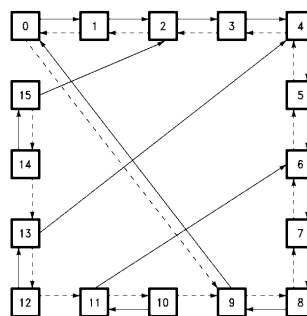
The Terminal Count Up ($\overline{TC}_U$) and Terminal Count Down ($\overline{TC}_D$) outputs are normally HIGH. When a circuit has reached the maximum count state (9 for the '192, 15 for the '193), the next HIGH-to-LOW transition of the Count Up Clock will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the $\overline{TC}$ outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

$$\overline{TC}_U = Q0 \bullet Q3 \bullet \overline{CP}_U$$
$$\overline{TC}_D = \overline{Q0} \bullet \overline{Q1} \bullet \overline{Q2} \bullet \overline{Q3} \bullet \overline{CP}_D$$
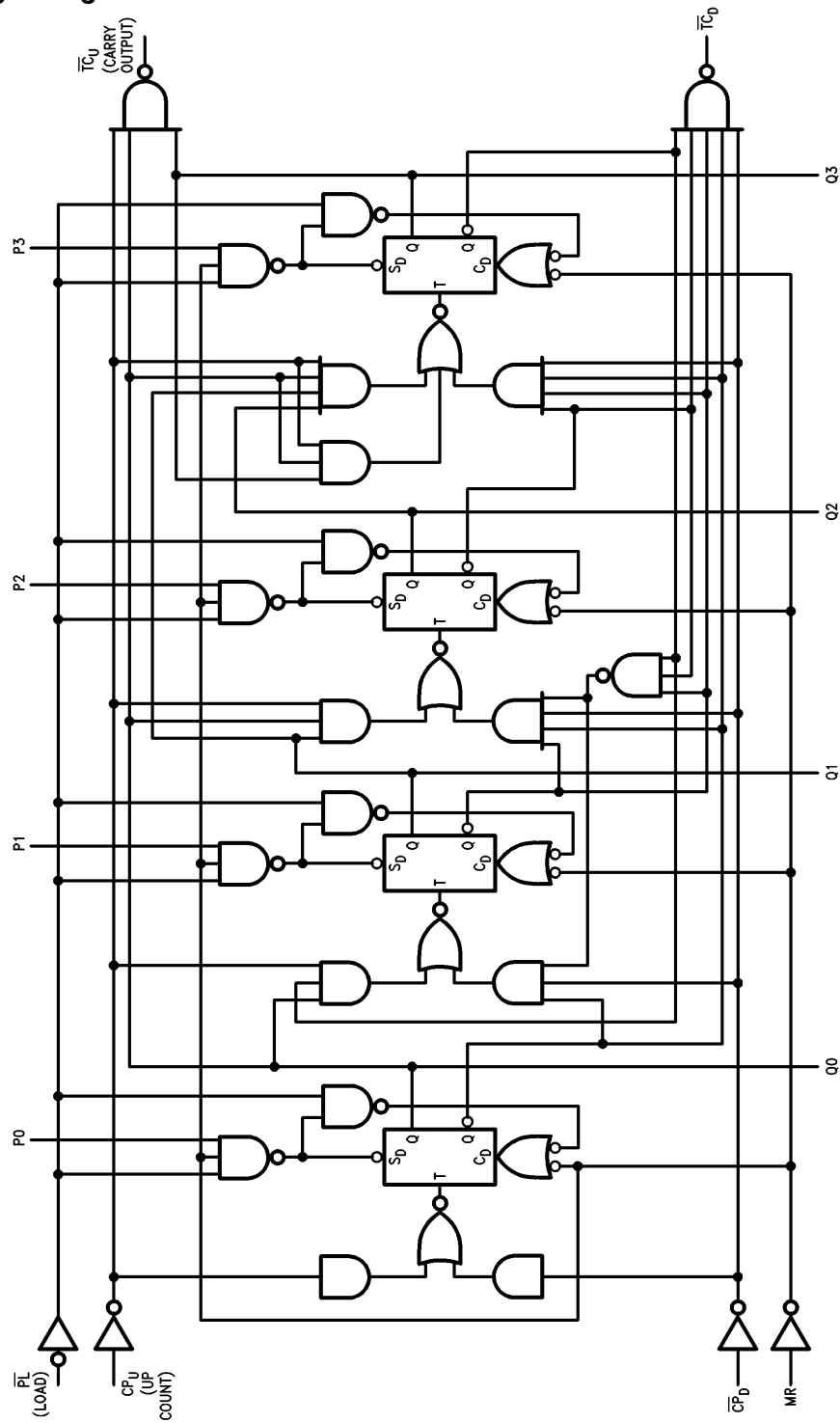
Each circuit has an asynchronous parallel load capability permitting the counter to be reset. When the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data inputs (P0–P3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both Clock inputs, and latch each Q output in the LOW state. If one of the Clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that Clock will be interpreted as a legitimate signal and will be counted.
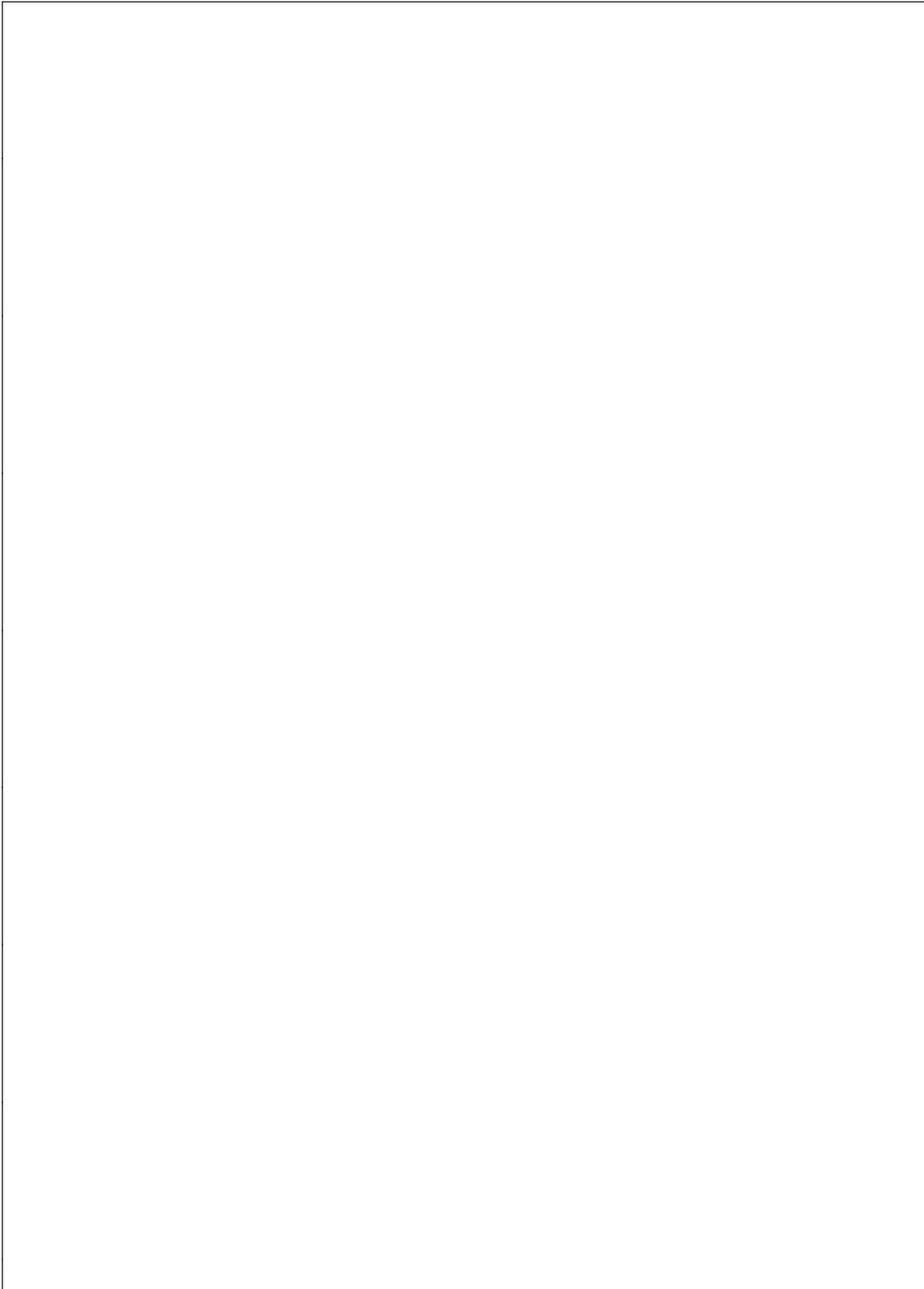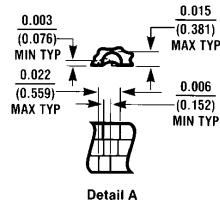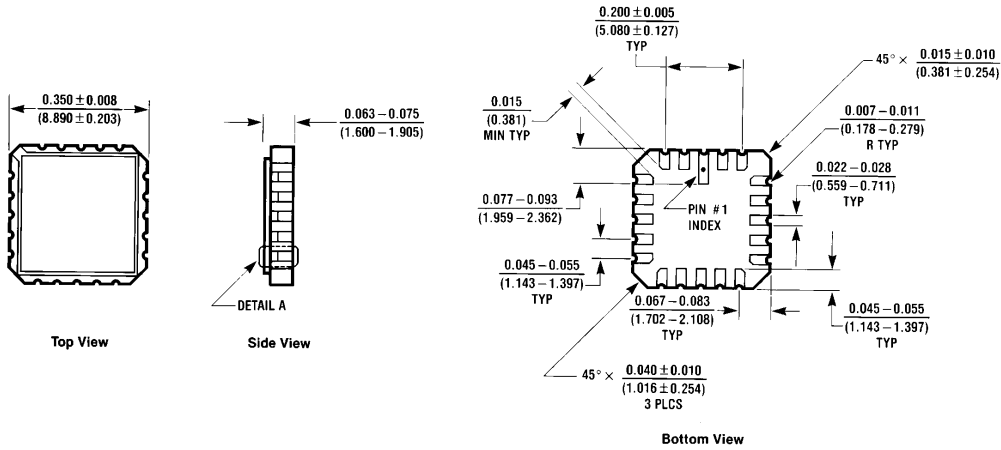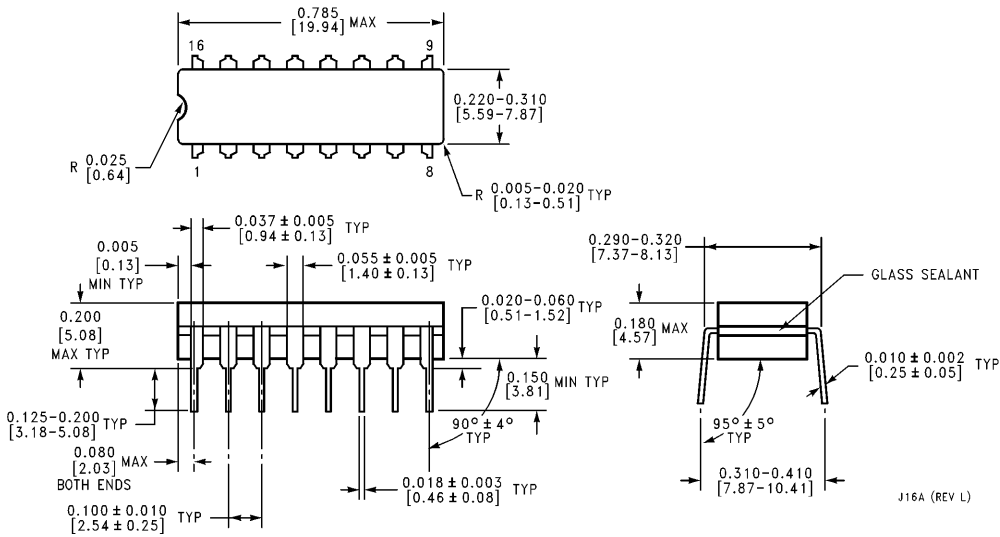
State Diagram

TL/F/10178–4

3

Logic Diagram

TL/F/10178–3

4

5

Physical Dimensions inches (millimeters)

Top View

Side View

DETAIL A

0.350 ± 0.008
(8.890 ± 0.203)

0.063 − 0.075
(1.600 − 1.905)

0.200 ± 0.005
(5.080 ± 0.127)
TYP

45° × 0.015 ± 0.010
(0.381 ± 0.254)

0.015
(0.381)
MIN TYP

0.007 − 0.011
(0.178 − 0.279)
R TYP

0.022 − 0.028
(0.559 − 0.711)
TYP

0.077 − 0.093
(1.959 − 2.362)

PIN #1
INDEX

0.045 − 0.055
(1.143 − 1.397)
TYP

0.067 − 0.083
(1.702 − 2.108)
TYP

0.045 − 0.055
(1.143 − 1.397)
TYP

45° × 0.040 ± 0.010
(1.016 ± 0.254)
3 PLCS

Bottom View

0.003
(0.076)
MIN TYP

0.015
(0.381)
MAX TYP

0.022
(0.559)
MAX TYP

0.006
(0.152)
MIN TYP

Detail A

E20A (REV D)

Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS192LMQB
NS Package Number E20A

0.785
[19.94] MAX

16   9

R 0.025
[0.64]

1   8

0.220−0.310
[5.59−7.87]

R 0.005−0.020
[0.13−0.51] TYP

0.037 ± 0.005
[0.94 ± 0.13] TYP

0.005
[0.13]
MIN TYP

0.055 ± 0.005
[1.40 ± 0.13] TYP

0.200
[5.08]
MAX TYP

0.020−0.060
[0.51−1.52] TYP

0.150 MIN TYP
[3.81]

0.125−0.200
[3.18−5.08] TYP

90° ± 4°
TYP

0.080
[2.03] MAX
BOTH ENDS

0.018 ± 0.003
[0.46 ± 0.08] TYP

0.100 ± 0.010
[2.54 ± 0.25] TYP

0.290−0.320
[7.37−8.13]

GLASS SEALANT

0.180 MAX
[4.57]

0.010 ± 0.002
[0.25 ± 0.05] TYP

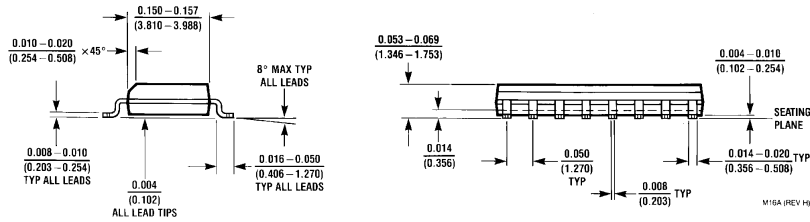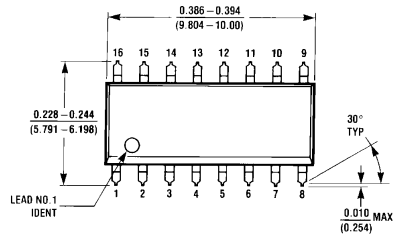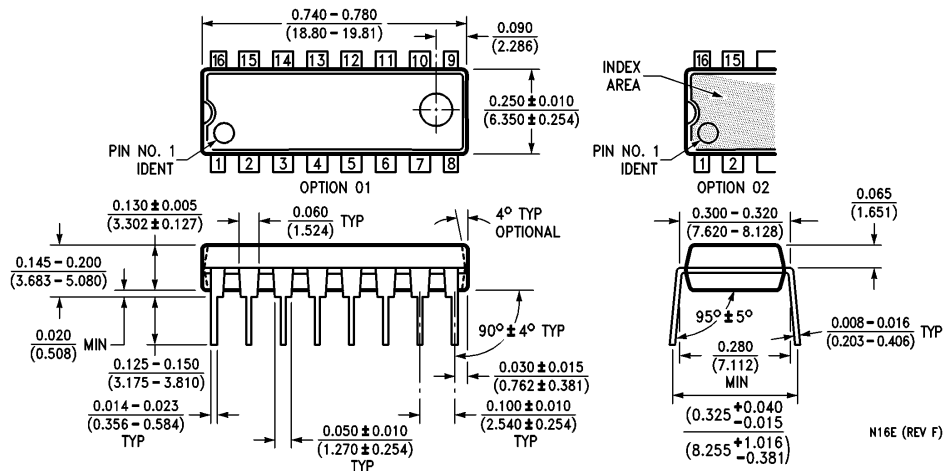95° ± 5°
TYP

0.310−0.410
[7.87−10.41]

J16A (REV L)

16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS192DMQB
NS Package Number J16A

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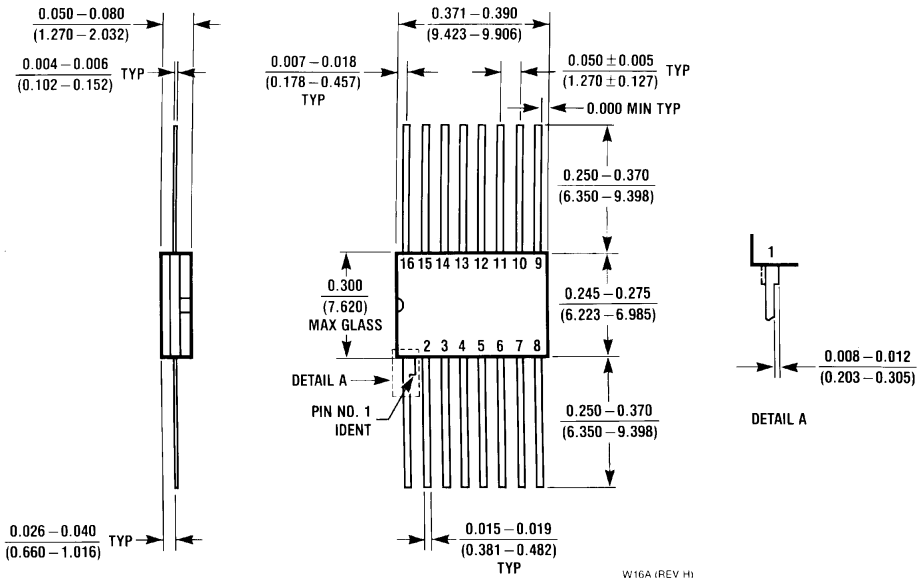**Physical Dimensions** inches (millimeters) (Continued)

0.386 − 0.394
(9.804 − 10.00)

16 15 14 13 12 11 10 9

0.228 − 0.244
(5.791 − 6.198)

30°
TYP

LEAD NO. 1
IDENT

1 2 3 4 5 6 7 8

0.010
(0.254) MAX

0.150 − 0.157
(3.810 − 3.988)

0.010 − 0.020
(0.254 − 0.508) × 45°

8° MAX TYP
ALL LEADS

0.008 − 0.010
(0.203 − 0.254)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.053 − 0.069
(1.346 − 1.753)

0.004 − 0.010
(0.102 − 0.254)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008
(0.203) TYP

0.014 − 0.020
(0.356 − 0.508) TYP

M16A (REV H)

16-Lead Small Outline Molded Package (M)
Order Number DM74LS192M
NS Package Number M16A

0.740 − 0.780
(18.80 − 19.81)

0.090
(2.286)

16 15 14 13 12 11 10 9

0.250 ± 0.010
(6.350 ± 0.254)

PIN NO. 1
IDENT

1 2 3 4 5 6 7 8

OPTION 01

INDEX
AREA

16 15

PIN NO. 1
IDENT

1 2

OPTION 02

0.130 ± 0.005
(3.302 ± 0.127)

0.060
(1.524) TYP

4° TYP
OPTIONAL

0.145 − 0.200
(3.683 − 5.080)

0.020
(0.508) MIN

0.125 − 0.150
(3.175 − 3.810)

0.014 − 0.023
(0.356 − 0.584)
TYP

0.050 ± 0.010
(1.270 ± 0.254)
TYP

90° ± 4° TYP

0.030 ± 0.015
(0.762 ± 0.381)

0.100 ± 0.010
(2.540 ± 0.254)
TYP

0.065
(1.651)

0.300 − 0.320
(7.620 − 8.128)

95° ± 5°

0.280
(7.112)
MIN

0.008 − 0.016
(0.203 − 0.406) TYP

$(0.325 ^{+0.040}_{-0.015})$

$(8.255 ^{+1.016}_{-0.381})$

N16E (REV F)

16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS192N
NS Package Number N16E

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Physical Dimensions inches (millimeters) (Continued)

$$\frac{0.050 - 0.080}{(1.270 - 2.032)}$$

$$\frac{0.004 - 0.006}{(0.102 - 0.152)} \text{ TYP}$$

$$\frac{0.371 - 0.390}{(9.423 - 9.906)}$$

$$\frac{0.007 - 0.018}{(0.178 - 0.457)} \text{ TYP}$$

$$\frac{0.050 \pm 0.005}{(1.270 \pm 0.127)} \text{ TYP}$$

0.000 MIN TYP

$$\frac{0.250 - 0.370}{(6.350 - 9.398)}$$

$$\frac{0.300}{(7.620)} \text{ MAX GLASS}$$

16 15 14 13 12 11 10 9

$$\frac{0.245 - 0.275}{(6.223 - 6.985)}$$

DETAIL A

1 2 3 4 5 6 7 8

PIN NO. 1 IDENT

$$\frac{0.250 - 0.370}{(6.350 - 9.398)}$$

$$\frac{0.026 - 0.040}{(0.660 - 1.016)} \text{ TYP}$$

$$\frac{0.015 - 0.019}{(0.381 - 0.482)} \text{ TYP}$$

W16A (REV H)

$$\frac{0.008 - 0.012}{(0.203 - 0.305)}$$

DETAIL A

16-Lead Ceramic Flat Package (W)
Order Number 54LS192FMQB
NS Package Number W16A

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