

## DM74LS194A

### 4-Bit Bidirectional Universal Shift Register

#### General Description

This bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register; they feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

- Parallel (broadside) load
- Shift right (in the direction  $Q_A$  toward  $Q_D$ )
- Shift left (in the direction  $Q_D$  toward  $Q_A$ )
- Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs,  $S_0$  and  $S_1$ , HIGH. The data is loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when  $S_0$  is HIGH and  $S_1$  is LOW. Serial data for this mode is entered at the shift-right data input. When  $S_0$  is LOW and  $S_1$  is HIGH, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are LOW.

#### Features

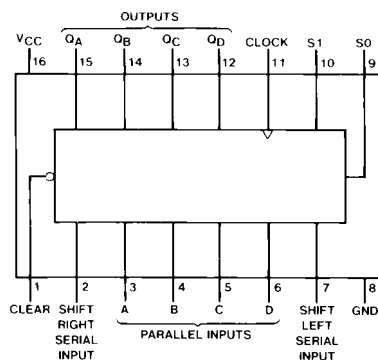
- Parallel inputs and outputs
- Four operating modes:
  - Synchronous parallel load
  - Right shift
  - Left shift
  - Do nothing
- Positive edge-triggered clocking
- Direct overriding clear

#### Ordering Code:

Order Number	Package Number	Package Description
DM74LS194AM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS194AN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Connection Diagram



## Function Table

Inputs									Outputs				
Clear	Mode		Clock	Serial		Parallel				Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>
	S1	S0		Left	Right	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>
H	L	H	↑	X	L	X	X	X	X	L	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>
H	H	L	↑	H	X	X	X	X	X	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	H
H	H	L	↑	L	X	X	X	X	X	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	L
H	L	L	X	X	X	X	X	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>

H = HIGH Level (steady state)

L = LOW Level (steady state)

X = Don't Care (any input, including transitions)

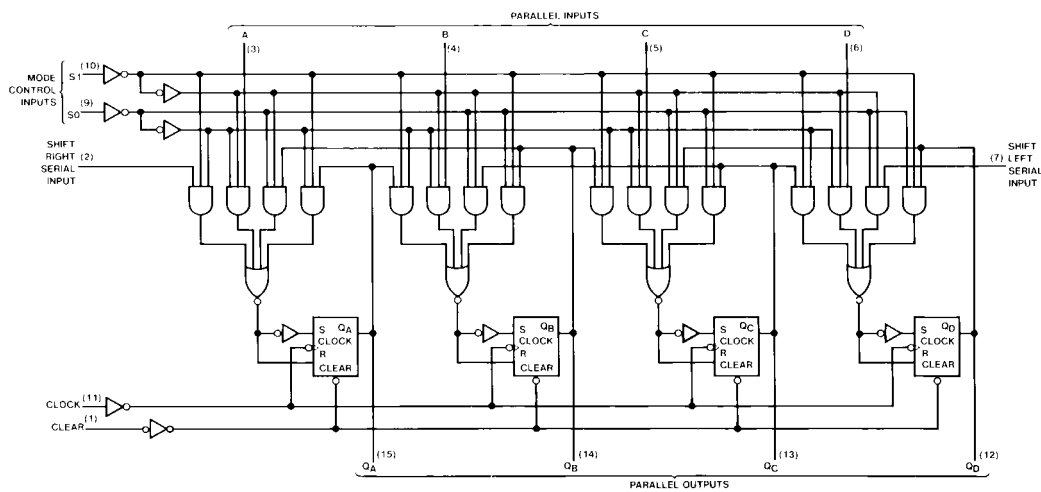
↑ = Transition from LOW-to-HIGH level

a, b, c, d = The level of steady state input at inputs A, B, C or D, respectively.

$Q_{A0}$ ,  $Q_{B0}$ ,  $Q_{C0}$ ,  $Q_{D0}$  = The level of  $Q_A$ ,  $Q_B$ ,  $Q_C$ , or  $Q_D$ , respectively, before the indicated steady state input conditions were established.

$Q_{An}$ ,  $Q_{Bn}$ ,  $Q_{Cn}$ ,  $Q_{Dn}$  = The level of  $Q_A$ ,  $Q_B$ ,  $Q_C$ , respectively, before the most-recent ↑ transition of the clock.

## Logic Diagram



**Absolute Maximum Ratings**(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Symbol	Parameter	Min	Nom	Max	Units
$V_{CC}$	Supply Voltage	4.75	5	5.25	V
$V_{IH}$	HIGH Level Input Voltage	2			V
$V_{IL}$	LOW Level Input Voltage			0.8	V
$I_{OH}$	HIGH Level Output Current			−0.4	mA
$I_{OL}$	LOW Level Output Current			8	mA
$f_{CLK}$	Clock Frequency (Note 2)	0		25	MHz
	Clock Frequency (Note 3)	0		20	
$t_W$	Pulse Width (Note 4)	Clock	20		ns
		Clear	20		
$t_{SU}$	Setup Time (Note 4)	Mode	30		ns
		Data	20		
$t_H$	Hold Time (Note 4)	0			ns
$t_{REL}$	Clear Release Time (Note 4)	25			ns
$T_A$	Free Air Operating Temperature	0		70	°C

**Note 2:**  $C_L = 15$  pF,  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5\text{V}$ .

**Note 3:**  $C_L = 50$  pF,  $R_L = 2$  k $\Omega$ ,  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5\text{V}$ .

**Note 4:**  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5\text{V}$ .

**Electrical Characteristics**

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 5)	Max	Units
$V_I$	Input Clamp Voltage	$V_{CC} = \text{Min}$ , $I_I = -18$ mA			−1.5	V
$V_{OH}$	HIGH Level Output Voltage	$V_{CC} = \text{Min}$ , $I_{OH} = \text{Max}$ $V_{IL} = \text{Max}$ , $V_{IH} = \text{Min}$	2.7	3.4		V
$V_{OL}$	LOW Level Output Voltage	$V_{CC} = \text{Min}$ , $I_{OL} = \text{Max}$ $V_{IL} = \text{Max}$ , $V_{IH} = \text{Min}$		0.35	0.5	V
		$I_{OL} = 4$ mA, $V_{CC} = \text{Min}$			0.4	
$I_I$	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}$ , $V_I = 7\text{V}$			0.1	mA
$I_{IH}$	HIGH Level Input Current	$V_{CC} = \text{Max}$ , $V_I = 2.7\text{V}$			20	$\mu\text{A}$
$I_{IL}$	LOW Level Input Current	$V_{CC} = \text{Max}$ , $V_I = 0.4\text{V}$			−0.4	mA
$I_{OS}$	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 6)	−20		−100	mA
$I_{CC}$	Supply Current	$V_{CC} = \text{Max}$ (Note 7)		15	23	mA

**Note 5:** All typicals are at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ .

**Note 6:** Not more than one output should be shorted at a time, and the duration should not exceed one second.

**Note 7:** With all outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, CLEAR, and the serial inputs,  $I_{CC}$  is tested with momentary ground, then 4.5V applied to CLOCK.

## Switching Characteristics

at  $V_{CC} = 5V$  and  $T_A = 25^\circ C$

Symbol	Parameter	From (Input) To (Output)	$C_L = 50 \text{ pF}, R_L = 2 \text{ k}\Omega$		Units
			Min	Max	
$f_{MAX}$	Maximum Clock Frequency		20		MHz
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Any Q		26	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Any Q		35	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Output	Clear to Any Q		38	ns

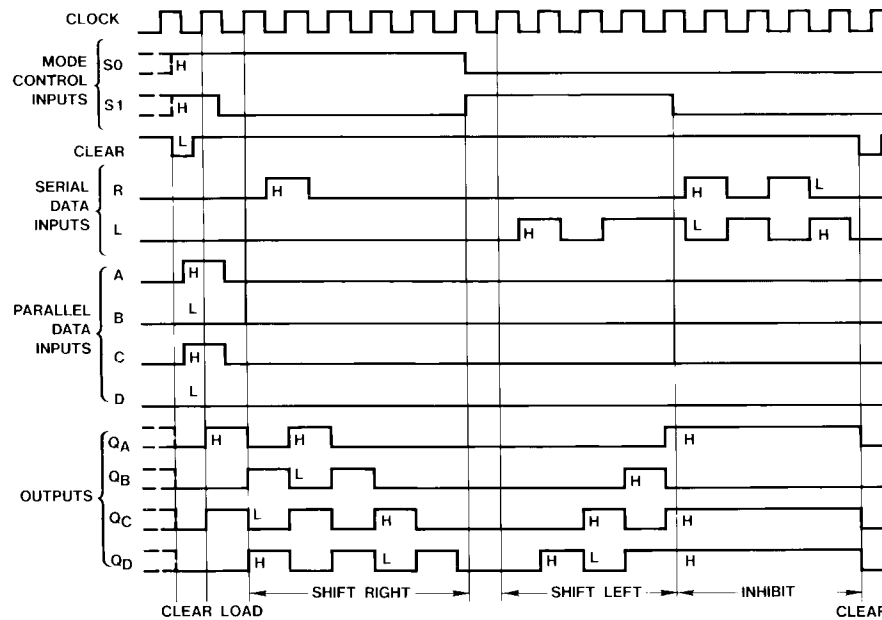
**Note 8:** All typicals are at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ .

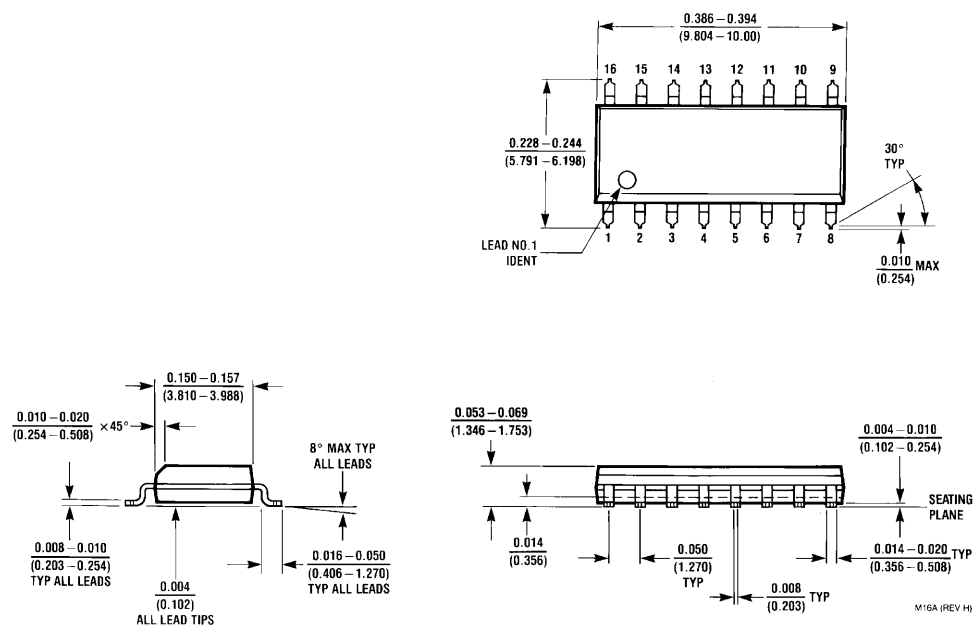
**Note 9:** Not more than one output should be shorted at a time, and the duration should not exceed one second.

**Note 10:** With all outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, CLEAR, and the serial inputs,  $I_{CC}$  is tested with momentary ground, then 4.5V applied to CLOCK.

## Timing Diagram

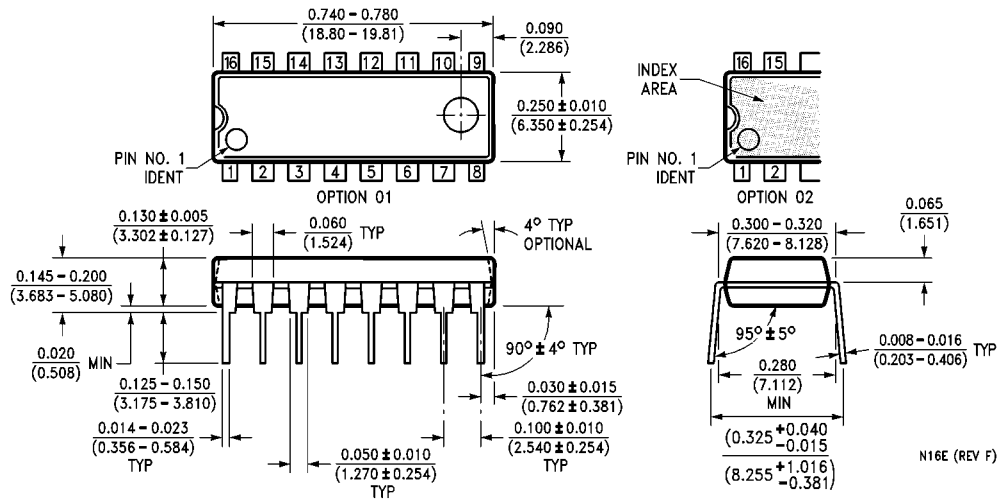
Typical Clear, Load, Right-Shift, Left-Shift, Inhibit, and Clear Sequences



**Physical Dimensions** inches (millimeters) unless otherwise noted


**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow  
Package Number M16A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide  
Package Number N16E

N16E (REV F)

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