FAIRCHILD SEMICONDUCTOR™

October 1986
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DM74AS573
Octal D-Type Transparent Latch with 3-STATE Outputs

General Description

These 8-bit registers feature totem-pole 3-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased HIGH-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the DM74AS573 are transparent D-type latches, meaning that while the enable (G) is HIGH the Q outputs will follow the data (D) inputs. When the enable is taken LOW the output will be latched at the level of the data that was set UP.

A buffered output control input can be used to place the eight outputs in either a normal logic state (HIGH or LOW logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are OFF.

The pin-out is arranged to ease printed circuit board layout. All data inputs are on one side of the package while all the outputs are on the other side.

Features

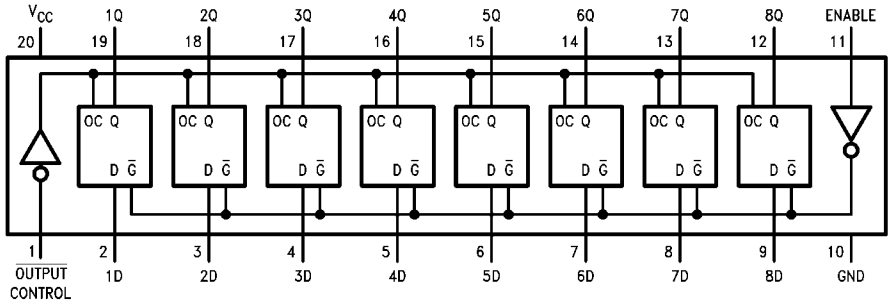
- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally equivalent with DM74S373
- Improved AC performance over DM74S373 at approximately half the power
- 3-STATE buffer-type outputs drive bus lines directly
- Bus structured pinout

Ordering Code:

Order Number	Package Number	Package Description
DM74AS573WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
DM74AS573N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

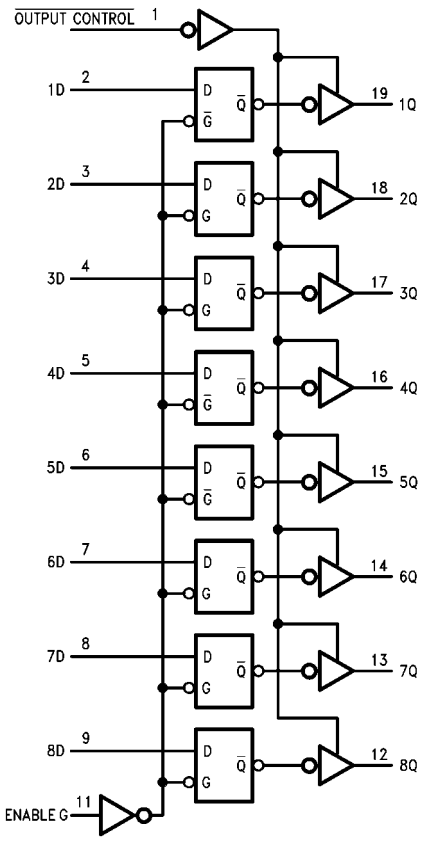


Function Table

$\overline{\text{Output}}$ Control	Enable G	D	Output Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

L = LOW State
H = HIGH State
X = Don't Care
Z = High Impedance State
Q_0 = Previous Condition of Q

Logic Diagram



Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	–65°C to +150°C
Typical θ_{JA}	
N Package	52.0°C/W
M Package	70.0°C/W

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	HIGH Level Input Voltage		2			V
V_{IL}	LOW Level Input Voltage				0.8	V
I_{OH}	HIGH Level Output Current				–15	mA
I_{OL}	LOW Level Output Current				48	mA
t_W	Width of Enable Pulse	HIGH	4.5			ns
		LOW	5.5			
t_{SU}	Data Setup Time (Note 2)		2↑			ns
t_H	Data Hold Time (Note 2)		3↑			ns
T_A	Free Air Operating Temperature		0		70	°C

Note 2: The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = –18 mA				–1.2	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = 4.5V, V_{IL} = Max, I_{OH} = Max		2.4	3.3		V
		V_{CC} = 4.5V to 5.5V, I_{OH} = –2 mA		V_{CC} – 2			
V_{OL}	LOW Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	µA
I_{IL}	LOW Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				–0.5	mA
I_O (Note 3)	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		–30		–112	mA
I_{OZH}	OFF-State Output Current, HIGH Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 2.7V				50	µA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 0.4V				–50	µA
I_{CC}	Supply Current	V_{CC} = 5.5V, Outputs Open	Outputs HIGH		56	93	mA
			Outputs LOW		55	90	
			Outputs Disabled		65	106	

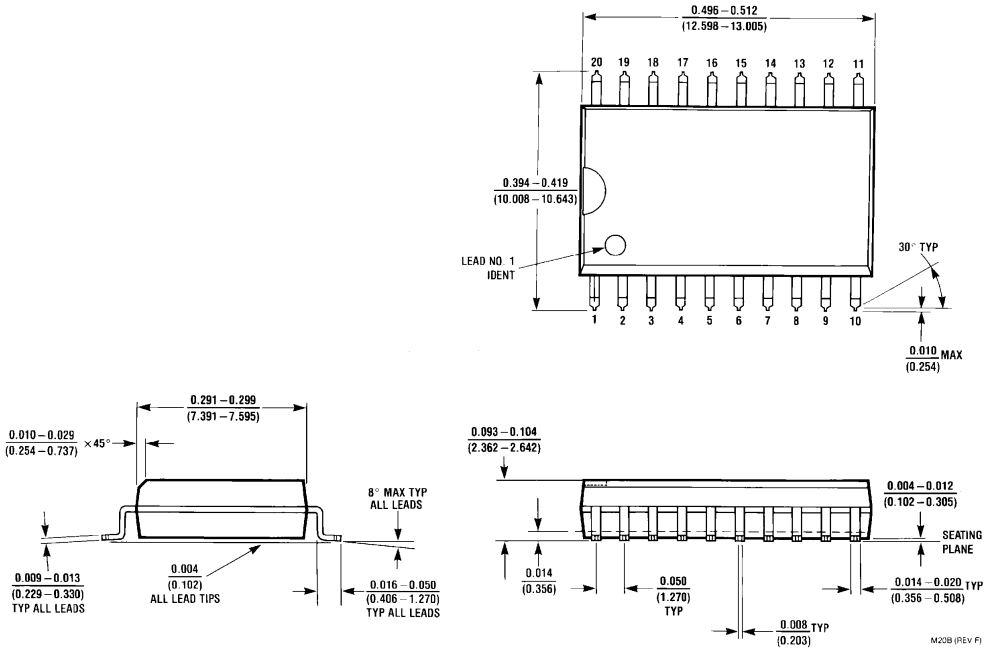
Note 3: The output conditions have been chosen to produce a current that approximates one half of the true short-circuit output current, I_{OS}.

Switching Characteristics

over recommended operating free air temperature range

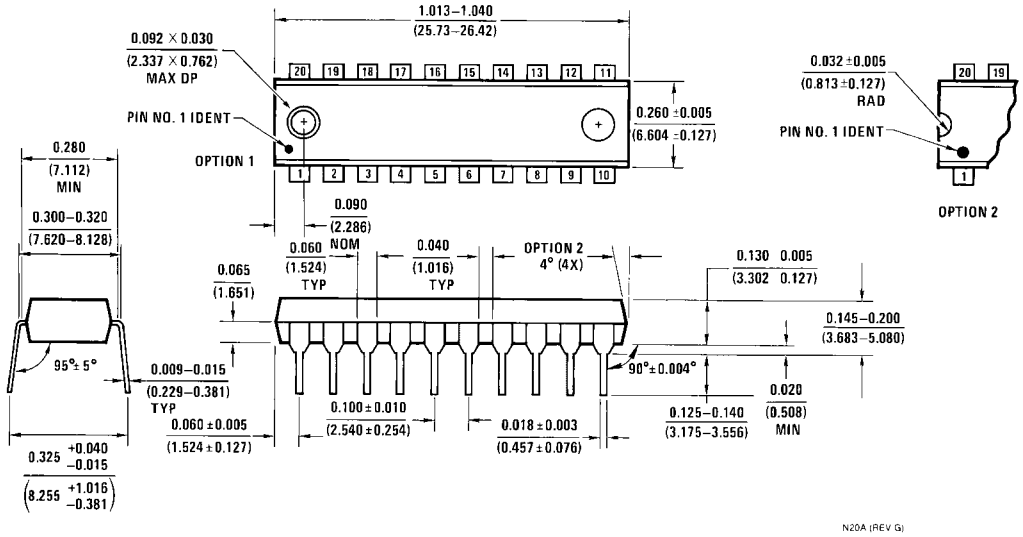
Symbol	Parameter	Conditions	From	To	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	Data	Any Q	3	6	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output		Data	Any Q	3	6	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output		Enable	Any Q	6	11.5	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output		Enable	Any Q	4	7.5	ns
t_{PZH}	Output Enable Time to HIGH Level Output		$\overline{\text{Output}}$ Control	Any Q	2	6.5	ns
t_{PZL}	Output Enable Time to LOW Level Output		$\overline{\text{Output}}$ Control	Any Q	4	9.5	ns
t_{PHZ}	Output Disable Time from HIGH Level Output		$\overline{\text{Output}}$ Control	Any Q	2	6.5	ns
t_{PLZ}	Output Disable Time from LOW Level Output		$\overline{\text{Output}}$ Control	Any Q	2	7	ns

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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