

## 74ABT126 Quad Buffer with 3-STATE Outputs

### General Description

The ABT126 contains four independent non-inverting buffers with 3-STATE outputs.

### Features

- Non-inverting buffers
- Output sink capability of 64 mA, source capability of 32 mA
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Disable time less than enable time to avoid bus contention

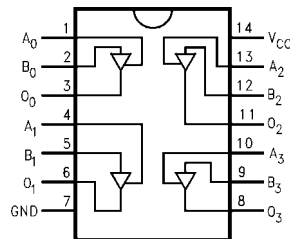
### Ordering Code:

| Order Number                 | Package Number | Package Description   |
|------------------------------|----------------|---|
| 74ABT126CSC                  | M14A           | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow        |
| 74ABT126CSJ                  | M14D           | Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide               |
| 74ABT126CMTC                 | MTC14          | 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide         |
| 74ABT126CMTCX_NL<br>(Note 1) | MTC14          | Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.  
Pb-Free package per JEDEC J-STD-020B.

**Note 1:** "\_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.

### Connection Diagram



### Pin Descriptions

| Pin Names  | Descriptions |
|------------|--------------|
| $A_n, B_n$ | Inputs       |
| $O_n$      | Outputs      |

### Function Table

| Inputs |       | Output |
|--------|-------|--------|
| $A_n$  | $B_n$ | $O_n$  |
| H      | L     | L      |
| H      | H     | H      |
| L      | X     | Z      |

H = HIGH Voltage Level  
L = LOW Voltage Level  
Z = HIGH Impedance  
X = Immaterial

**Absolute Maximum Ratings** (Note 2)

|  |                                      |
|--|--------------------------------------|
| Storage Temperature  | -65°C to +150°C                      |
| Ambient Temperature under Bias   | -55°C to +125°C                      |
| Junction Temperature under Bias  | -55°C to +150°C                      |
| V <sub>CC</sub> Pin Potential to Ground Pin                            | -0.5V to +7.0V                       |
| Input Voltage (Note 3)   | -0.5V to +7.0V                       |
| Input Current (Note 3)   | -30 mA to +5.0 mA                    |
| Voltage Applied to Any Output<br>in the Disabled or<br>Power-Off State | -0.5V to 5.5V                        |
| in the HIGH State  | -0.5V to V <sub>CC</sub>             |
| Current Applied to Output<br>in LOW State (Max)                        | twice the rated I <sub>OL</sub> (mA) |
| DC Latchup Source Current<br>(Across Comm Operating Range)             | -300 mA                              |
| Over Voltage Latchup (I/O)   | 10V                                  |

**Recommended Operating Conditions**

|   |                |
|---|----------------|
| Free Air Ambient Temperature                    | -40°C to +85°C |
| Supply Voltage                                  | +4.5V to +5.5V |
| Minimum Input Edge Rate ( $\Delta V/\Delta t$ ) |                |
| Data Input                                      | 50 mV/ns       |
| Enable Input                                    | 100 mV/ns      |

**Note 2:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 3:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

| Symbol           | Parameter                         | Min     | Typ  | Max  | Units      | V <sub>CC</sub> | Conditions  |
|------------------|-----------------------------------|---------|------|------|------------|-----------------|---|
| V <sub>IH</sub>  | Input HIGH Voltage                | 2.0     |      |      | V          |                 | Recognized HIGH Signal  |
| V <sub>IL</sub>  | Input LOW Voltage                 |         |      | 0.8  | V          |                 | Recognized LOW Signal   |
| V <sub>CD</sub>  | Input Clamp Diode Voltage         |         |      | -1.2 | V          | Min             | I <sub>IN</sub> = -18 mA  |
| V <sub>OH</sub>  | Output HIGH Voltage               | 2.5     |      |      | V          | Min             | I <sub>OH</sub> = -3 mA   |
|                  |                                   | 2.0     |      |      | V          | Min             | I <sub>OH</sub> = -32 mA  |
| V <sub>OL</sub>  | Output LOW Voltage                |         | 0.55 |      | V          | Min             | I <sub>OL</sub> = 64 mA   |
| I <sub>IH</sub>  | Input HIGH Current                |         | 1    |      | μA         | Max             | V <sub>IN</sub> = 2.7V (Note 4)   |
|                  |                                   |         | 1    |      | μA         | Max             | V <sub>IN</sub> = V <sub>CC</sub>   |
| I <sub>BVI</sub> | Input HIGH Current Breakdown Test |         |      | 7    | μA         | Max             | V <sub>IN</sub> = 7.0V  |
| I <sub>IL</sub>  | Input LOW Current                 |         |      | -1   | μA         | Max             | V <sub>IN</sub> = 0.5V (Note 4)   |
|                  |                                   |         |      | -1   | μA         | Max             | V <sub>IN</sub> = 0.0V  |
| V <sub>ID</sub>  | Input Leakage Test                | 4.75    |      |      | V          | 0.0             | I <sub>ID</sub> = 1.9 μA, All Other Pin Grounded  |
| I <sub>OZH</sub> | Output Leakage Current            |         |      | 10   | μA         | 0 - 5.5V        | V <sub>OUT</sub> = 2.7V; $\overline{OE}_n = 2.0V$   |
| I <sub>OZL</sub> | Output Leakage Current            |         |      | -10  | μA         | 0 - 5.5V        | V <sub>OUT</sub> = 0.5V; $\overline{OE}_n = 2.0V$   |
| I <sub>OS</sub>  | Output Short-Circuit Current      | -100    |      | -275 | mA         | Max             | V <sub>OUT</sub> = 0.0V   |
| I <sub>CEX</sub> | Output HIGH Leakage Current       |         |      | 50   | μA         | Max             | V <sub>OUT</sub> = V <sub>CC</sub>  |
| I <sub>ZZ</sub>  | Bus Drainage Test                 |         |      | 100  | μA         | 0.0             | V <sub>OUT</sub> = 5.5V; All Others GND   |
| I <sub>CCH</sub> | Power Supply Current              |         |      | 50   | μA         | Max             | All Outputs HIGH  |
| I <sub>CCL</sub> | Power Supply Current              |         |      | 15   | mA         | Max             | All Outputs LOW   |
| I <sub>CCZ</sub> | Power Supply Current              |         |      | 50   | μA         | Max             | $\overline{OE}_n = V_{CC}$ ;<br>All Others at V <sub>CC</sub> or Ground   |
|                  |                                   |         |      | 1.5  | mA         | Max             | V <sub>I</sub> = V <sub>CC</sub> - 2.1V   |
|                  |                                   |         |      | 50   | μA         |                 | Enable Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V<br>Data Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V<br>All Others at V <sub>CC</sub> or Ground |
| I <sub>CCD</sub> | Dynamic I <sub>CC</sub> (Note 4)  | No Load |      | 0.1  | mA/<br>MHz | Max             | Outputs Open<br>$\overline{OE}_n = \text{GND}$ , (Note 5)<br>One Bit Toggling, 50% Duty Cycle   |

**Note 4:** Guaranteed, but not tested.

**Note 5:** For 8 bits toggling, I<sub>CCD</sub> < 0.8 mA/MHz.

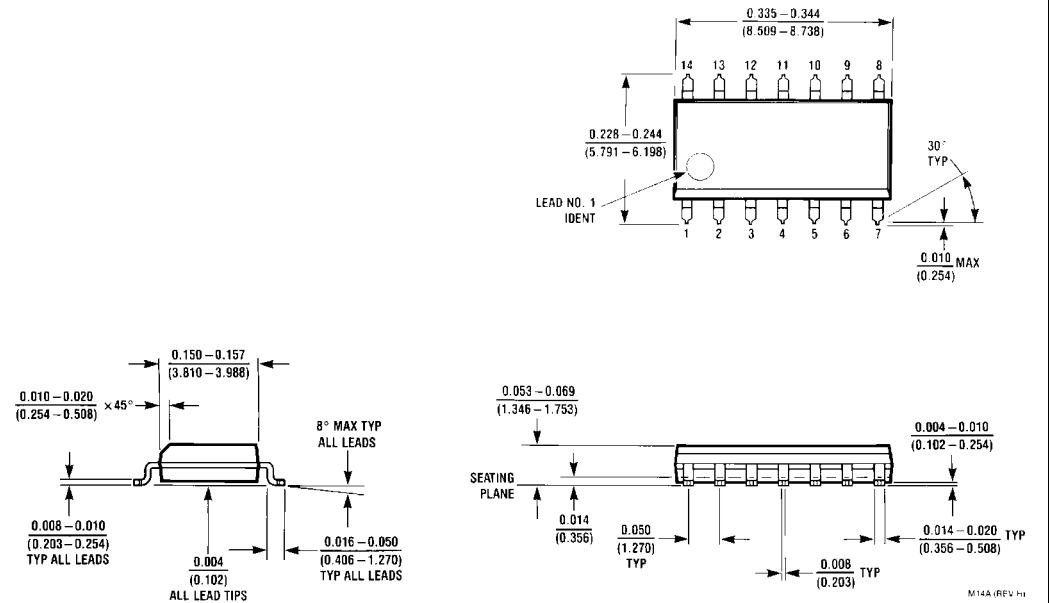
| AC Electrical Characteristics |                   |  |     |     |   |     |       |
|-------------------------------|-------------------|--|-----|-----|---|-----|-------|
| Symbol                        | Parameter         | $T_A = +25^\circ\text{C}$<br>$V_{CC} = +5\text{V}$<br>$C_L = 50\text{ pF}$ |     |     | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$<br>$V_{CC} = 4.5\text{V} - 5.5\text{V}$<br>$C_L = 50\text{ pF}$ |     | Units |
|                               |                   | Min  | Typ | Max | Min   | Max |       |
| $t_{PLH}$                     | Propagation Delay | 1.0  |     | 4.4 | 1.0   | 4.4 | ns    |
| $t_{PHL}$                     | Data to Outputs   | 1.0  |     | 4.6 | 1.0   | 4.6 |       |
| $t_{PZH}$                     | Output Enable     | 1.0  |     | 6.5 | 1.0   | 6.5 | ns    |
| $t_{PZL}$                     | Time              | 1.0  |     | 6.5 | 1.0   | 6.5 |       |
| $t_{PHZ}$                     | Output Disable    | 1.0  |     | 5.8 | 1.0   | 5.8 | ns    |
| $t_{PLZ}$                     | Time              | 1.0  |     | 5.5 | 1.0   | 5.5 |       |

| Capacitance        |                    |     |       |  |
|--------------------|--------------------|-----|-------|--|
| Symbol             | Parameter          | Typ | Units | Conditions<br>$T_A = 25^\circ\text{C}$ |
| $C_{IN}$           | Input Capacitance  | 5.0 | pF    | $V_{CC} = 0\text{V}$                   |
| $C_{OUT}$ (Note 6) | Output Capacitance | 9.0 | pF    | $V_{CC} = 5.0\text{V}$                 |

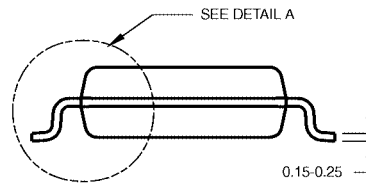
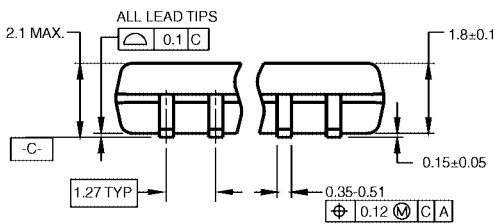
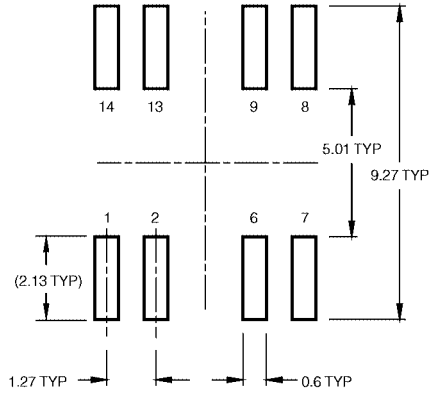
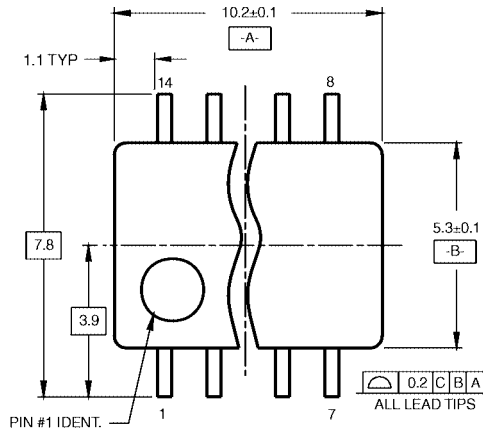
**Note 6:**  $C_{OUT}$  is measured at frequency  $f = 1\text{ MHz}$ , per MIL-STD-883, Method 3012.

**Physical Dimensions** inches (millimeters) unless otherwise noted



**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow  
Package Number M14A**

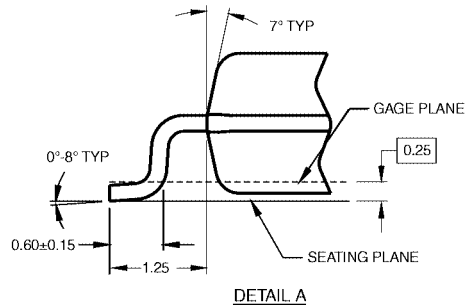
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

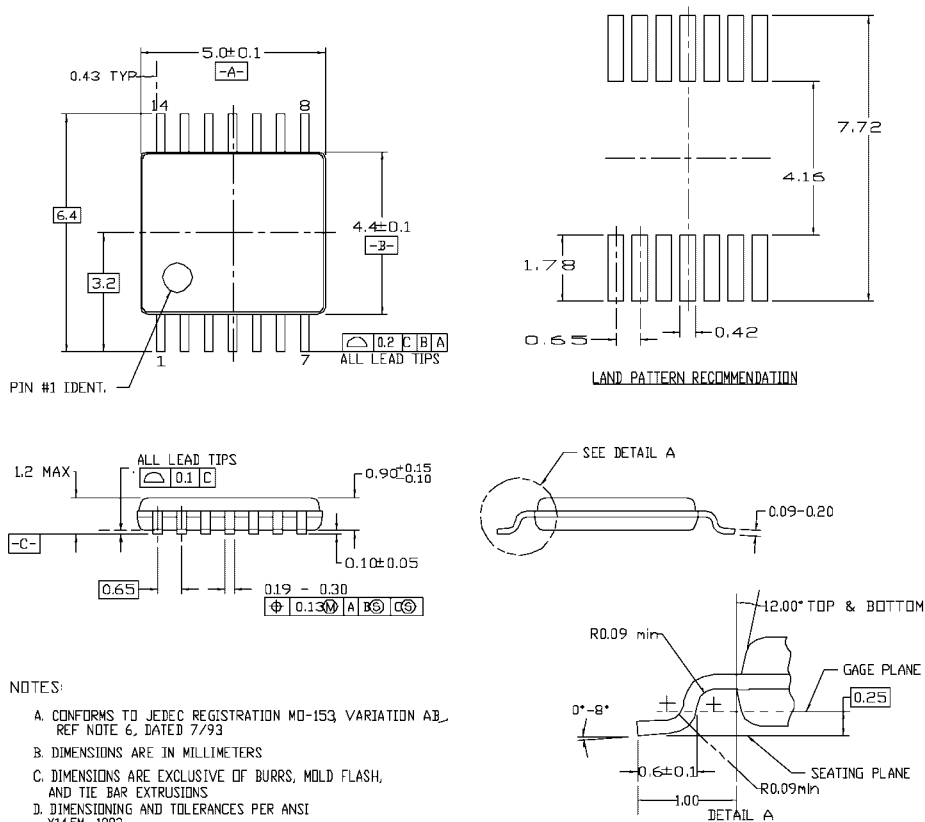
- NOTES:  
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.  
 B. DIMENSIONS ARE IN MILLIMETERS.  
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1



**Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M14D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



- NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO-153 VARIATION AB, REF NOTE 6, DATED 7/93
  - B. DIMENSIONS ARE IN MILLIMETERS
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
  - D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

MTC14revD

**14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14**

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