

DATA SHEET

74ABT16952

16-bit registered transceiver (3-State)

Product specification

Replaces 74ABT16952/74ABTH16952 dated 1998 Feb 25

2002 Apr 03

16-bit registered transceiver (3-State)

74ABT16952

FEATURES

- Two 8-bit registered transceivers
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- Multiple V_{CC} and GND pins minimize switching noise
- Independent registers for A and B buses
- Output capability: +64 mA/-32 mA
- Latch-up protection exceeds 500 mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs

DESCRIPTION

The 74ABT16952 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16952 is a dual octal registered transceiver. Two 8-bit registers store data flowing in both directions between two bidirectional buses. Data applied to the inputs is entered and stored on the rising edge of the Clock ($nCPXX$) provided that the Clock Enable ($nCEXX$) is LOW. The data is then present at the 3-State output buffers, but is only accessible when the Output Enable ($nOEXX$) is LOW. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25\text{ }^{\circ}\text{C}; \text{GND} = 0\text{ V}$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay $nCPBA$ to nAx or $nCPAB$ to nBx	$C_L = 50\text{ pF}; V_{CC} = 5\text{ V}$	2.8 2.3	ns
C_{IN}	Input capacitance	$V_I = 0\text{ V}$ or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	$V_O = 0\text{ V}$ or V_{CC} ; 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; $V_{CC} = 5.5\text{ V}$	500	μA
I_{CCL}		Outputs LOW; $V_{CC} = 5.5\text{ V}$	8	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
56-Pin Plastic SSOP Type III	-40 °C to +85 °C	74ABT16952DL	SOT371-1
56-Pin Plastic TSSOP Type II	-40 °C to +85 °C	74ABT16952DGG	SOT364-1

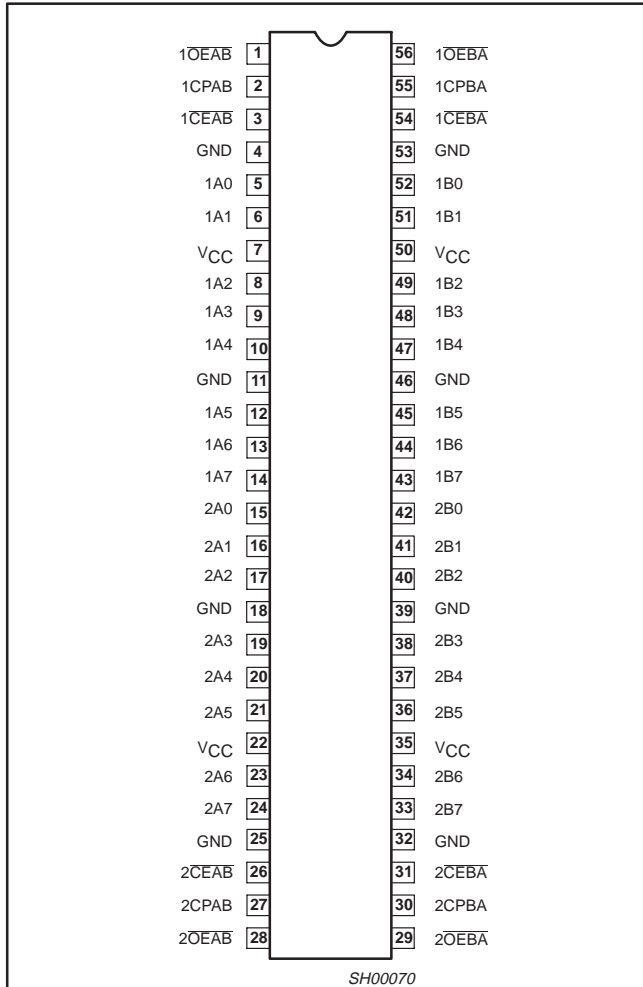
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 55 18, 22	1CPAB / 1CPBA 2CPAB / 2CPBA	Clock input A-to-B / Clock input B-to-A
3, 54, 26, 31	1CEAB / 1CEBA 2CEAB / 2CEBA	Clock enable input A-to-B / Clock enable input B-to-A
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33	1A0 – 1A7 2A0 – 2A7	Data inputs/outputs (A side)
1, 56 8, 29	1B0 – 1B7 2B0 – 2B7	Data inputs/outputs (B side)
4, 11, 18, 25, 32, 39, 45, 53	1OEAB / 1OEBA 2OEAB / 2OEBA	Output enable inputs
4, 17, 30, 43	GND	Ground (0 V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

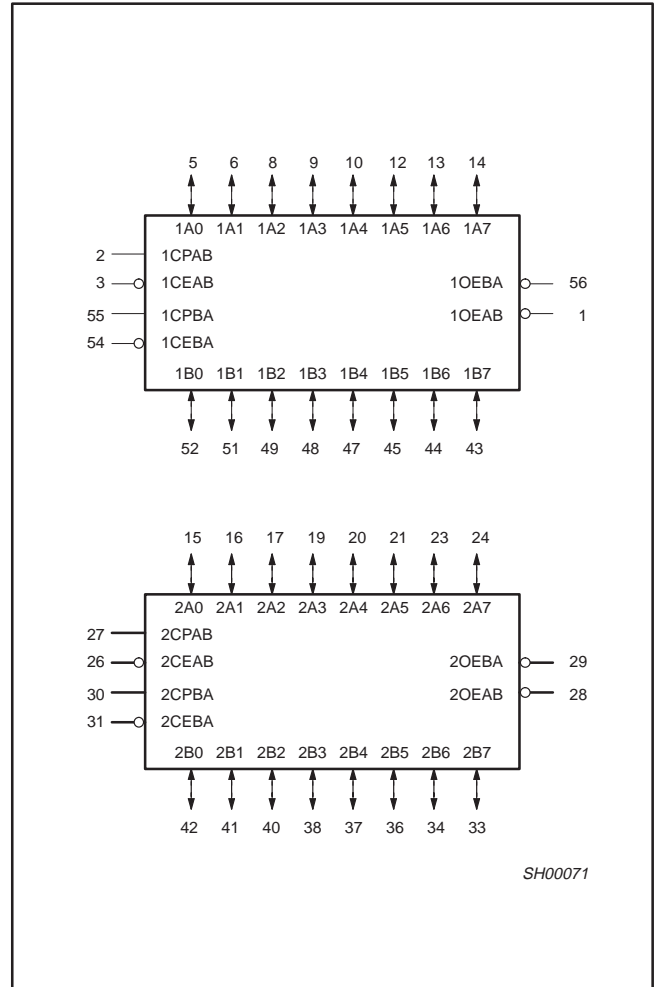
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PIN CONFIGURATION



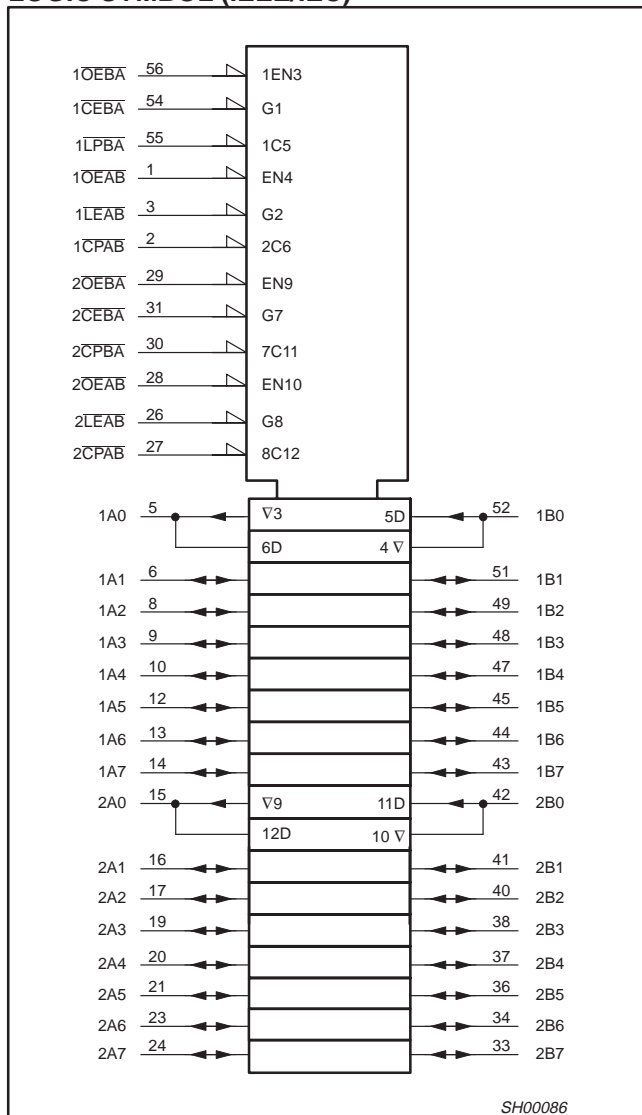
LOGIC SYMBOL



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LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE for Register nAx or nBx

INPUTS			INTERNAL Q	OPERATING MODE
nAx or nBx	nCPXX	nCEXX		
X	X	H	NC	Hold data
L H	↑ ↑	L L	L H	Load data

H = HIGH voltage level
 L = LOW voltage level
 ↑ = LOW-to-HIGH transition
 X = Don't care
 XX = AB or BA
 NC = No change

FUNCTION TABLE for Output Enable

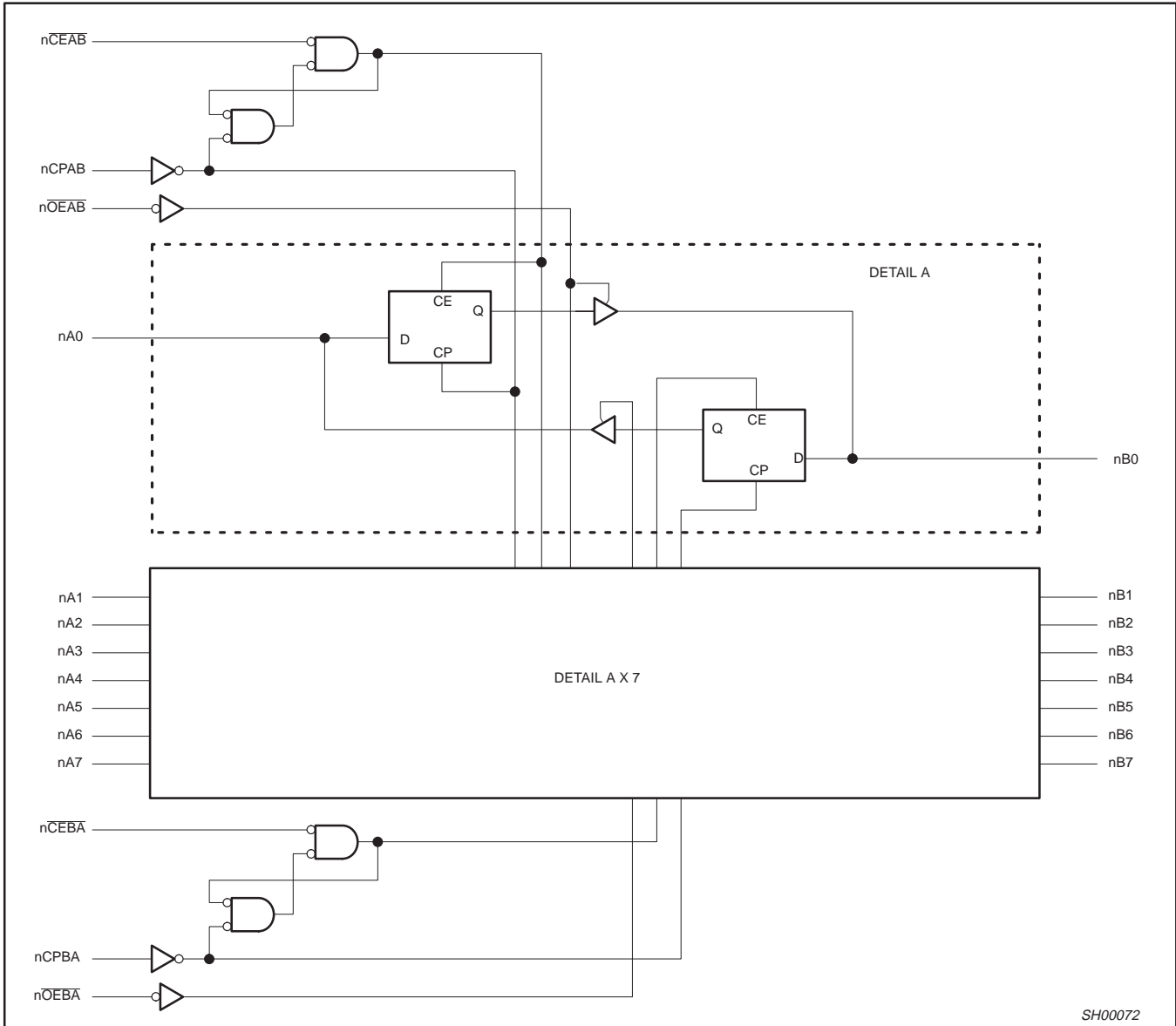
INPUTS		INTERNAL Q	nAx or nBx OUTPUTS	OPERATING MODE
nOEXX				
H		X	Z	Disable outputs
L L		L H	L H	Enable outputs

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 XX = AB or BA
 Z = High impedance "off" state

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LOGIC DIAGRAM



SH00072

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ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0	-18	mA
V _I	DC input voltage ³		-1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	-50	mA
V _{OUT}	DC output voltage ³	Output in Off or HIGH state	-0.5 to +5.5	V
I _{OUT}	DC output current	Output in LOW state	128	mA
		Output in HIGH state	-64	
T _{stg}	Storage temperature range		-65 to +150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V _{CC}	DC supply voltage	4.5	5.5	V
V _I	Input voltage	0	V _{CC}	V
V _{IH}	HIGH-level input voltage	2.0	-	V
V _{IL}	LOW-level Input voltage	-	0.8	V
I _{OH}	HIGH-level output current	-	-32	mA
I _{OL}	LOW-level output current	-	64	mA
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T _{amb}	Operating free-air temperature range	-40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _{amb} = +25 °C			T _{amb} = -40 °C to +85 °C		
			MIN	TYP	MAX	MIN	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 4.5 V; I _{IK} = -18 mA		-0.9	-1.2		-1.2	V
V _{OH}	HIGH-level output voltage	V _{CC} = 4.5 V; I _{OH} = -3 mA; V _I = V _{IL} or V _{IH}	2.5	2.9		2.5		V
		V _{CC} = 5.0 V; I _{OH} = -3 mA; V _I = V _{IL} or V _{IH}	3.0	3.4		3.0		V
		V _{CC} = 4.5 V; I _{OH} = -32 mA; V _I = V _{IL} or V _{IH}	2.0	2.4		2.0		V
V _{OL}	LOW-level output voltage	V _{CC} = 4.5 V; I _{OL} = 64 mA; V _I = V _{IL} or V _{IH}		0.42	0.55		0.55	V
V _{RST}	Power-up output low voltage ³	V _{CC} = 5.5 V; I _{OL} = 1 mA; V _I = GND or V _{CC}		0.13	0.55		0.55	V
I _I	Input leakage current	Control pins V _{CC} = 5.5 V; V _I = GND or 5.5 V		±0.01	±1.0		±1.0	µA
I _{OFF}	Power-off leakage current	V _{CC} = 0 V; V _O or V _I ≤ 4.5 V		±5.0	±100		±100	µA
I _{PU/PD}	Power-up/down 3-State output current ⁴	V _{CC} = 2.1 V; V _O = 0.0 V; V _I = GND or V _{CC} ; V _{OE} = Don't care		±5.0	±50		±50	µA
I _{IH} + I _{OZH}	3-State output HIGH current	V _{CC} = 5.5 V; V _O = 5.5 V; V _I = V _{IL} or V _{IH}		5.0	50		50	µA
I _{IL} + I _{OZL}	3-State output LOW current	V _{CC} = 5.5 V; V _O = 0.0 V; V _I = V _{IL} or V _{IH}		-5.0	-50		-50	µA
I _{CEX}	Output HIGH leakage current	V _{CC} = 5.5 V; V _O = 5.5 V; V _I = GND or V _{CC}		5.0	50		50	µA
I _O	Output current ¹	V _{CC} = 5.5 V; V _O = 2.5 V	-50	-70	-180	-50	-180	mA
I _{CCH}	Quiescent supply current	V _{CC} = 5.5 V; Outputs HIGH, V _I = GND or V _{CC}		0.5	1.5		1.5	mA
I _{CCL}		V _{CC} = 5.5 V; Outputs LOW, V _I = GND or V _{CC}		8	19		19	mA
I _{CCZ}		V _{CC} = 5.5 V; Outputs 3-State; V _I = GND or V _{CC}		0.5	1.5		1.5	mA
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 5.5 V; one input at 3.4 V, other inputs at V _{CC} or GND		5	100		100	µA

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4 V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- This parameter is valid for any V_{CC} between 0 V and 2.1 V with a transition time of up to 10 msec. From V_{CC} = 2.1 V to V_{CC} = 5 V ± 10% a transition time of up to 100 µsec is permitted.
- Unused pins at V_{CC} or GND.

AC CHARACTERISTICS

GND = 0 V; t_R = t_F = 2.5 ns; C_L = 50 pF, R_L = 500 Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25 °C V _{CC} = +5.0 V			T _{amb} = -40 °C to +85 °C V _{CC} = +5.0 V ± 0.5 V		
			MIN	TYP	MAX	MIN	MAX	
f _{MAX}	Maximum clock frequency	1	150			150		MHz
t _{PLH} t _{PHL}	Propagation delay nCPBA to nAx, nCPAB to nBx	1	1.0	2.8	3.9	1.0	4.3	ns
			1.0	2.3	3.9	1.0	4.3	
t _{PZH} t _{PZL}	Output enable time nOEBA to nAx, nOEAB to nBx	3 4	1.0	2.5	3.8	1.0	4.6	ns
			1.0	2.2	3.8	1.0	4.6	
t _{PHZ} t _{PLZ}	Output disable time nOEBA to nAx, nOEAB to nBx	3 4	1.7	3.4	4.4	1.7	5.2	ns
			1.3	2.6	3.9	1.3	4.2	

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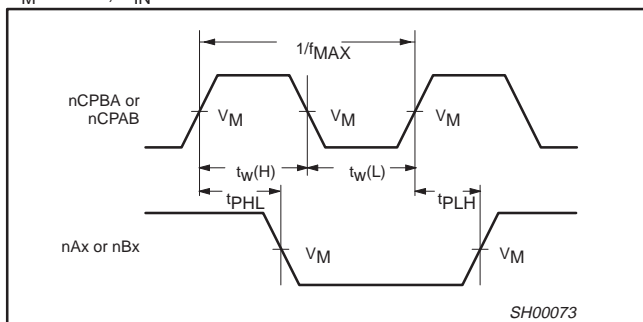
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AC SET-UP REQUIREMENTS

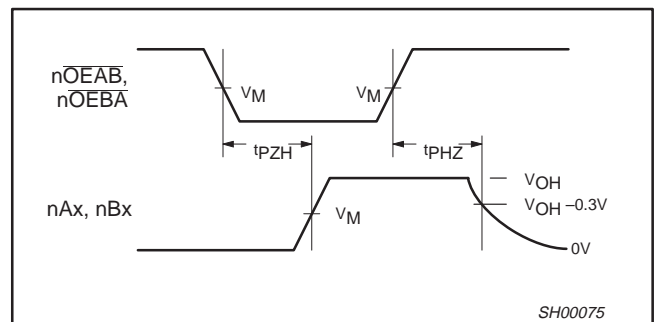
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{amb} = +25\text{ }^{\circ}\text{C}$ $V_{CC} = +5.0\text{ V}$		$T_{amb} = -40\text{ }^{\circ}\text{C to } +85\text{ }^{\circ}\text{C}$ $V_{CC} = +5.0\text{ V } \pm 0.5\text{ V}$	
			MIN	TYP	MIN	
$t_s(H)$ $t_s(L)$	Set-up time nAx to nCPAB or nBx to nCPBA	2	1.2 1.5	0.9 1.2	1.2 1.5	ns
$t_h(H)$ $t_h(L)$	Hold time nAx to nCPAB or nBx to nCPBA	2	0.0 0.0	-1.2 -0.9	0.0 0.0	ns
$t_s(H)$ $t_s(L)$	Set-up time nCEAB to nCPAB, nCEBA to nCPBA	2	1.2 1.6	0.9 1.1	1.2 1.6	ns
$t_h(H)$ $t_h(L)$	Hold time nCEAB to nCPAB, nCEBA to nCPBA	2	0.0 0.0	-1.1 -0.9	0.0 0.0	ns
$t_w(H)$ $t_w(L)$	nCPAB or nCPBA pulse width, HIGH or LOW	1	3.3 2.5	2.6 1.0	3.3 2.5	ns

AC WAVEFORMS

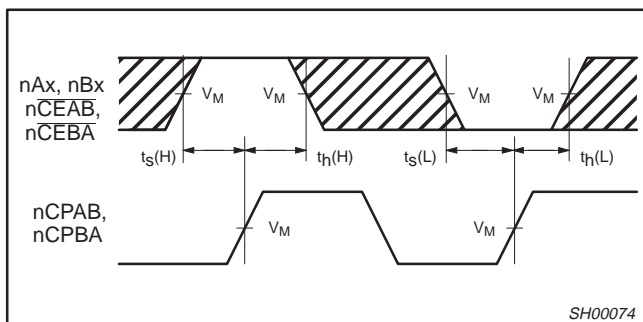
$V_M = 1.5\text{ V}$, $V_{IN} = \text{GND to } 3.0\text{ V}$



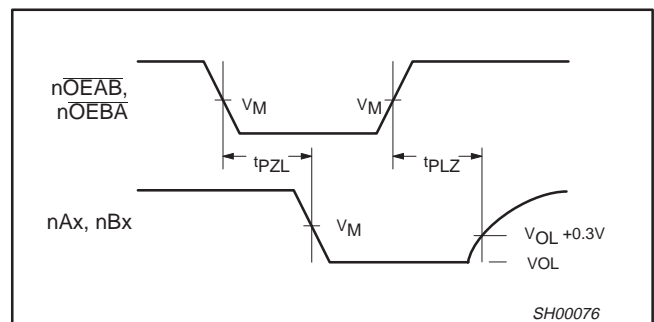
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 2. Data Set-up and Hold Times

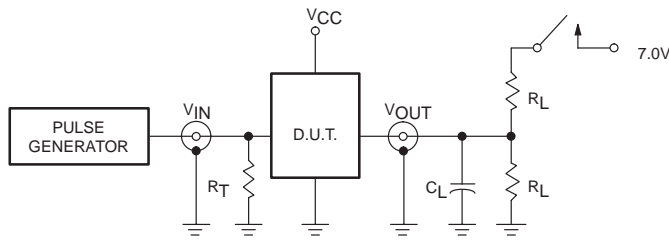


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

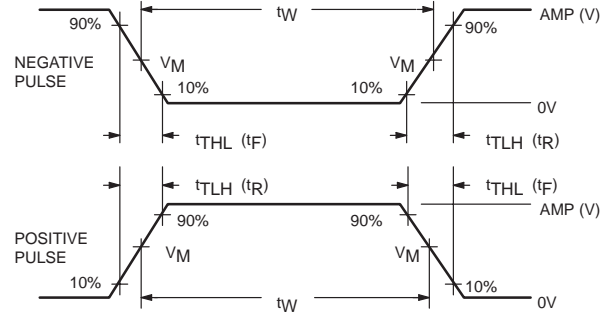
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TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



**VM = 1.5V
Input Pulse Definition**

SWITCH POSITION

TEST	SWITCH
tPLZ	closed
tPZL	closed
All other	open

DEFINITIONS

RL = Load resistor; see AC CHARACTERISTICS for value.
 CL = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 RT = Termination resistance should be equal to ZOUT of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	tW	tR	tF
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

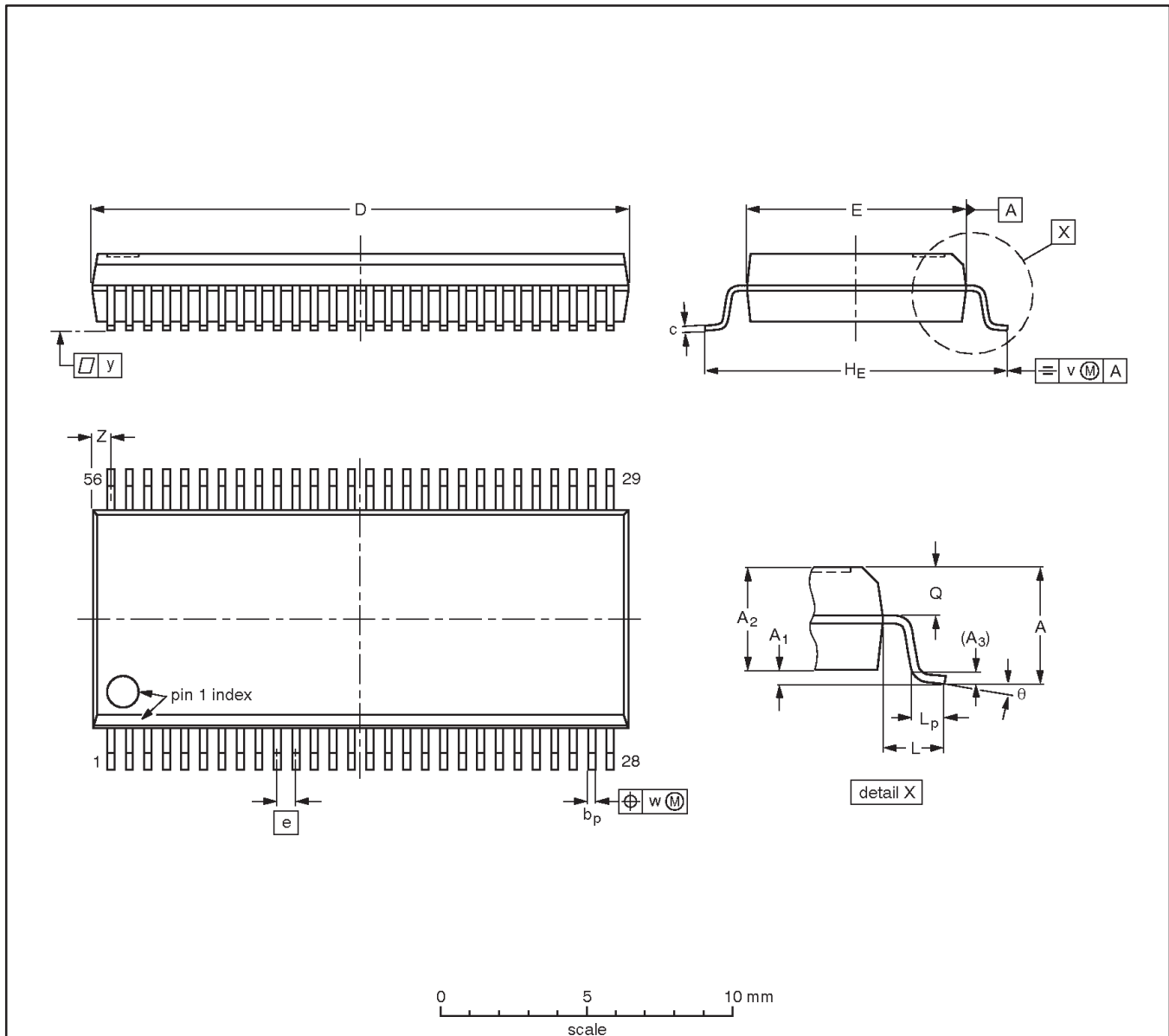
SA00018

16-bit registered transceiver (3-State)

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SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1




DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

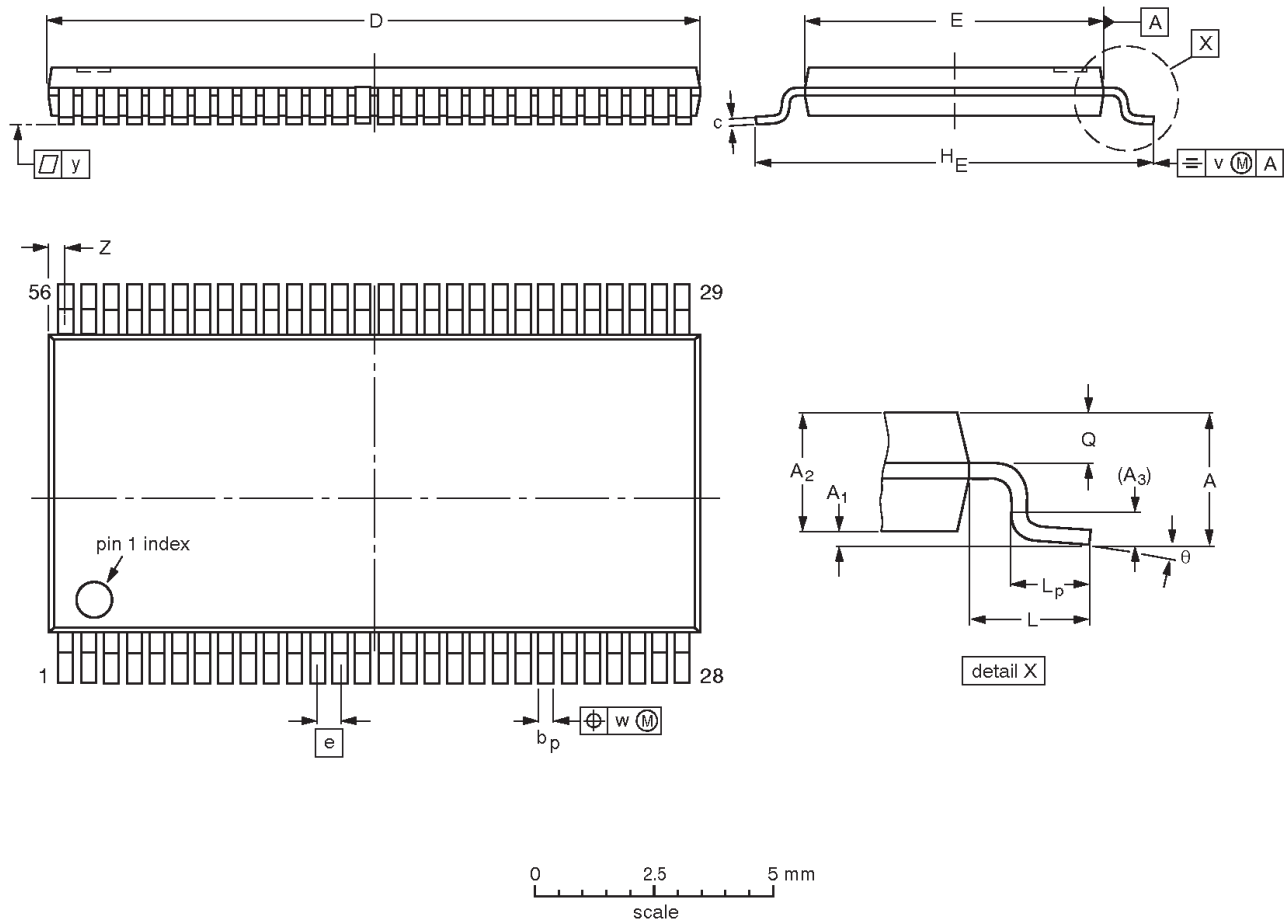
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118				95-02-04 99-12-27

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TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1.0	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT364-1		MO-153				95-02-10 99-12-27

16-bit registered transceiver (3-State)

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Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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For additional information please visit
<http://www.semiconductors.philips.com>. Fax: +31 40 27 24825

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Date of release: 04-02

For sales offices addresses send e-mail to:
sales.addresses@www.semiconductors.philips.com

Document order number:

9397 750 09693

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