DATA SHEET

74ABT16541
16-bit buffer/line driver (3-State)

Product data

2004 Jan 28

Replaces data sheet 74ABT16541/74ABTH16541 of 1998 Feb 25

Philips
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16-bit buffer/line driver (3-State) 74ABT16541

FEATURES

- Power-up 3-State
- Multiple V_{CC} and GND pins minimize switching noise
- Provides ideal interface and increases fan-out of MOS Microprocessors
- 3-State buffers sink 64 mA and source 32 mA
- Latch-up protection exceeds 500 mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Two 8-bit bus interfaces

DESCRIPTION

The 74ABT16541 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16541 has two octal buffers that are ideal for driving bus lines. The outputs are all capable of sinking 64 mA and sourcing 32 mA.

QUICK REFERENCE DATA

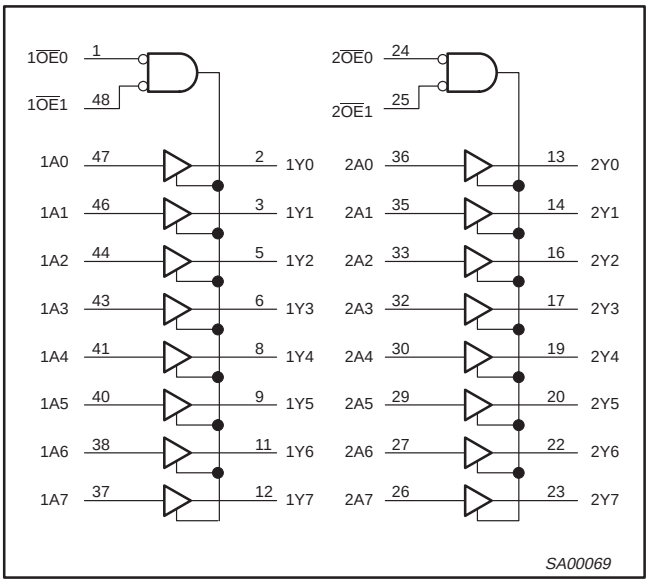
SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25 °C; GND = 0 V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50 pF; V_{CC} = 5 V	2.0 1.5	ns
C_{IN}	Input capacitance	V_I = 0 V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0 V or V_{CC}; 3-State	6	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} =5.5 V	500	µA
I_{CCL}		Outputs LOW; V_{CC} = 5.5 V	8	mA

ORDERING INFORMATION

T_{amb} = –40 °C to +85 °C

Type number	Package		
	Name	Description	Version
74ABT16541DL	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1
74ABT16541DGG	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

LOGIC SYMBOL

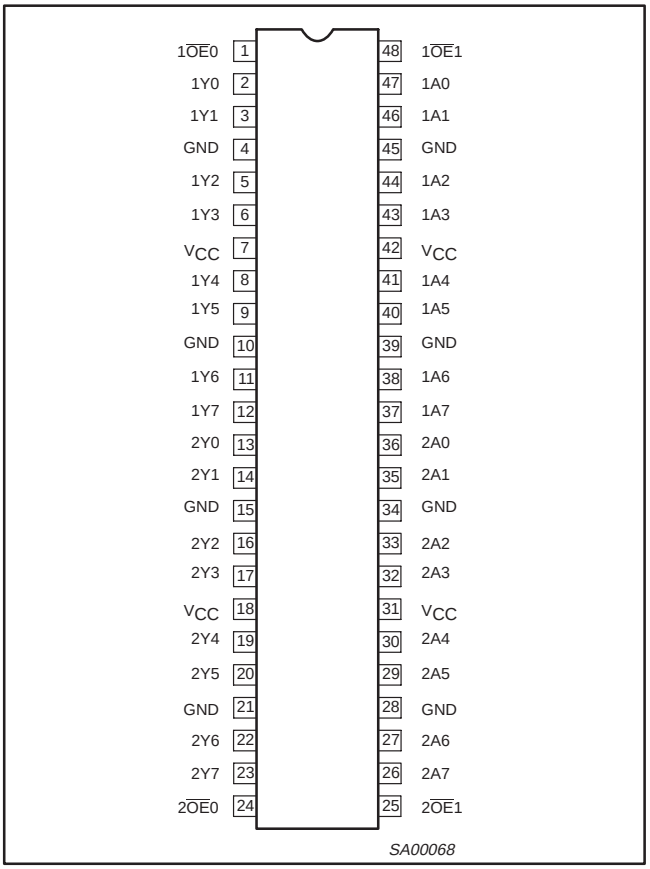


FUNCTION TABLE

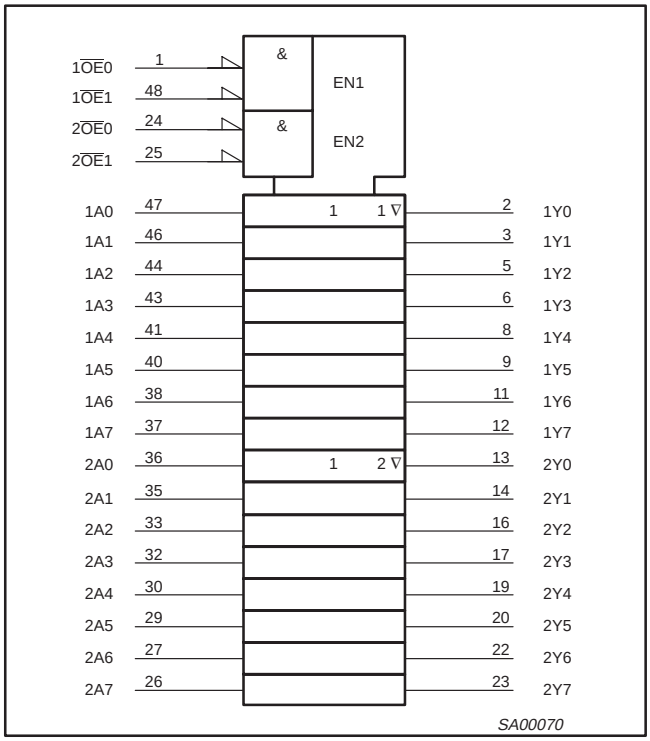
INPUTS			OUTPUTS
$n\overline{OE}0$	$n\overline{OE}1$	nAx	nYx
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance "off" state

PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1A0 - 1A7 2A0 - 2A7	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17 19, 20, 22, 23	1Y0 - 1Y7, 2Y0 - 2Y7	Data outputs
1, 48 24, 25	1$\overline{OE}$0, 1$\overline{OE}$1, 2$\overline{OE}$0, 2$\overline{OE}$1	Output enables
4, 10, 15, 21 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or HIGH state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in LOW state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	HIGH-level input voltage	2.0	–	V
V_{IL}	LOW-level Input voltage	–	0.8	V
I_{OH}	HIGH-level output current	–	–32	mA
I_{OL}	LOW-level output current	–	64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25 °C			T_{amb} = –40 °C to +85 °C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5 V; I_{IK} = –18 mA	–	–0.9	–1.2	–	–1.2	V
V_{OH}	HIGH-level output voltage	V_{CC} = 4.5 V; I_{OH} = –3 mA; V_I = V_{IL} or V_{IH}	2.5	2.9	–	2.5	–	V
		V_{CC} = 5.0 V; I_{OH} = –3 mA; V_I = V_{IL} or V_{IH}	3.0	3.4	–	3.0	–	V
		V_{CC} = 4.5 V; I_{OH} = –32 mA; V_I = V_{IL} or V_{IH}	2.0	2.4	–	2.0	–	V
V_{OL}	LOW-level output voltage	V_{CC} = 4.5 V; I_{OL} = 64 mA; V_I = V_{IL} or V_{IH}	–	0.42	0.55	–	0.55	V
I_I	Input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V	–	±0.01	±1.0	–	±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0 V; V_O or $V_I \leq$ 4.5 V	–	±5.0	±100	–	±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current	V_{CC} = 2.0 V; V_O = 0.5 V; V_I = GND or V_{CC}; $\overline{V_{OE}}$ = V_{CC}	–	±5.0	±50	–	±50	µA
I_{OZH}	3-State output HIGH current	V_{CC} = 5.5 V; V_O = 2.7 V; V_I = V_{IL} or V_{IH}	–	1.0	10	–	10	µA
I_{OZL}	3-State output LOW current	V_{CC} = 5.5 V; V_O = 0.5 V; V_I = V_{IL} or V_{IH}	–	–1.0	–10	–	–10	µA
I_{CEX}	Output high leakage current	V_{CC} = 5.5 V; V_O = 5.5 V; V_I = GND or V_{CC}	–	1.0	50	–	50	µA
I_O	Output current[1]	V_{CC} = 5.5 V; V_O = 2.5 V	–50	–70	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5 V; Outputs HIGH; V_I = GND or V_{CC}	–	0.5	1.0	–	1.0	mA
I_{CCL}		V_{CC} = 5.5 V; Outputs LOW; V_I = GND or V_{CC}	–	8	19	–	19	mA
I_{CCZ}		V_{CC} = 5.5 V; Outputs 3-State; V_I = GND or V_{CC}	–	0.5	1.0	–	1.0	mA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4 V, other inputs at V_{CC} or GND; V_{CC} = 5.5 V	–	100	250	–	250	µA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4 V.

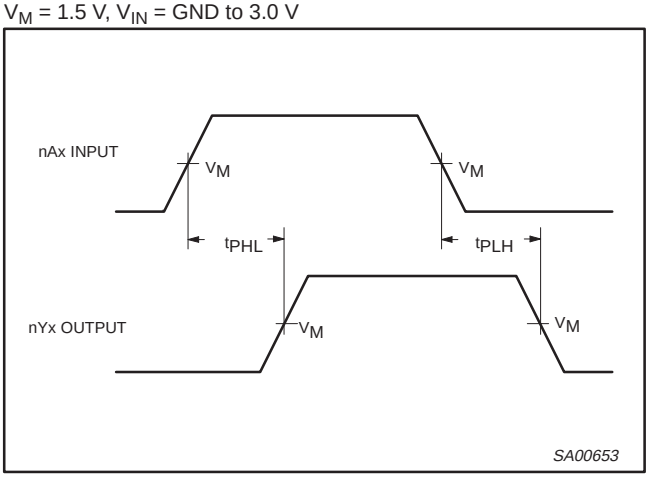
AC CHARACTERISTICS

GND = 0 V; $t_R = t_F$ = 2.5 ns; C_L = 50 pF, R_L = 500 Ω

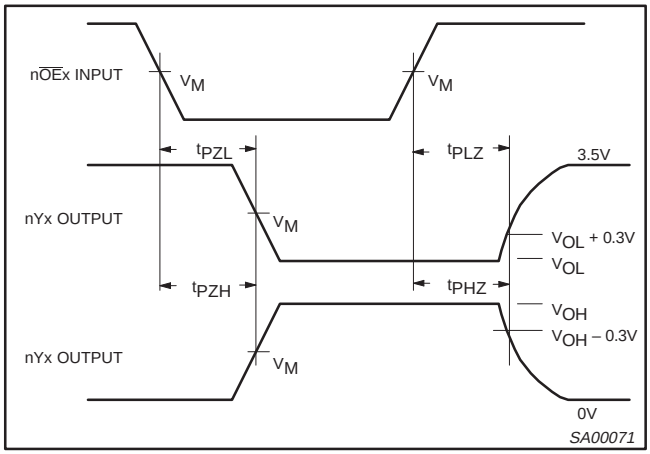
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25 °C V_{CC} = +5.0 V			T_{amb} = –40 °C to +85 °C V_{CC} = +5.0 V ± 0.5 V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	1.0 1.0	2.0 1.5	3.0 3.6	1.0 1.0	3.4 4.2	ns
t_{PZH} t_{PZL}	Output enable time to HIGH and LOW level	2	1.3 1.6	2.9 3.1	4.3 4.7	1.3 1.6	5.2 6.0	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH and LOW level	2	1.3 1.0	3.5 2.8	4.4 3.6	1.3 1.0	5.1 3.9	ns

AC WAVEFORMS

V_M = 1.5 V, V_{IN} = GND to 3.0 V

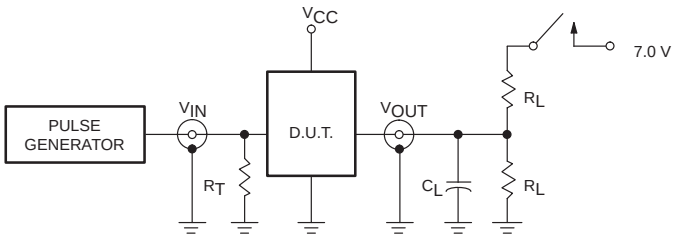


Waveform 1. Input (An) to Output (Yn) Propagation Delays

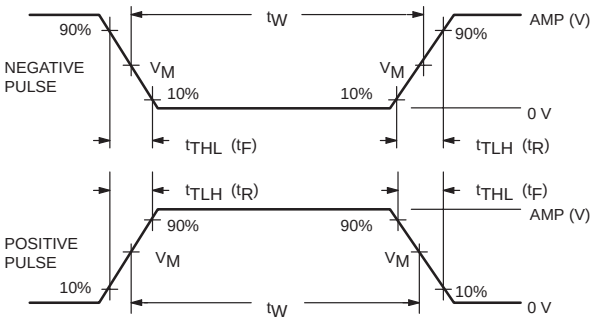


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5 V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

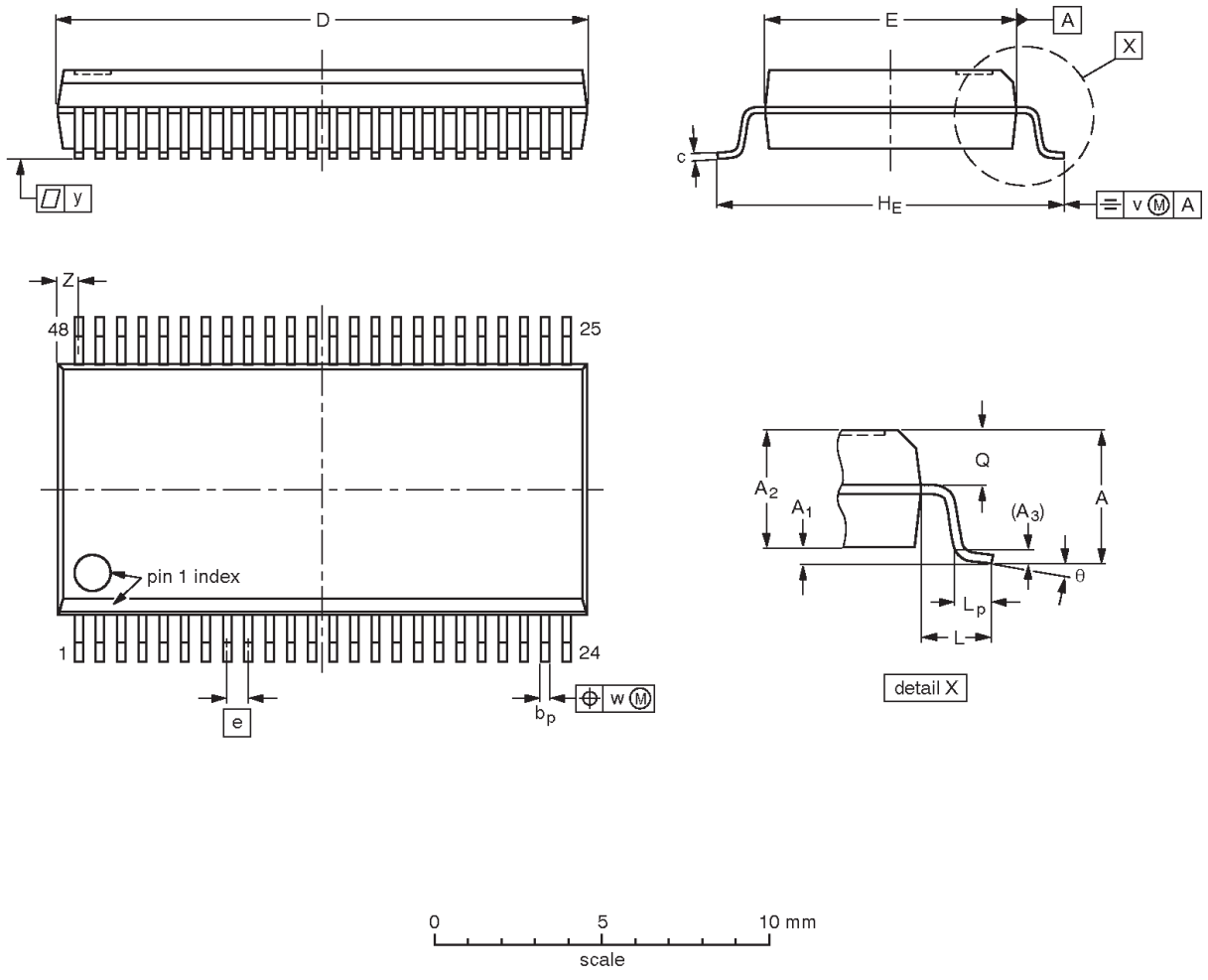
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0 V	1 MHz	500 ns	2.5 ns	2.5 ns

SA00654

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**



DIMENSIONS (mm are the original dimensions)

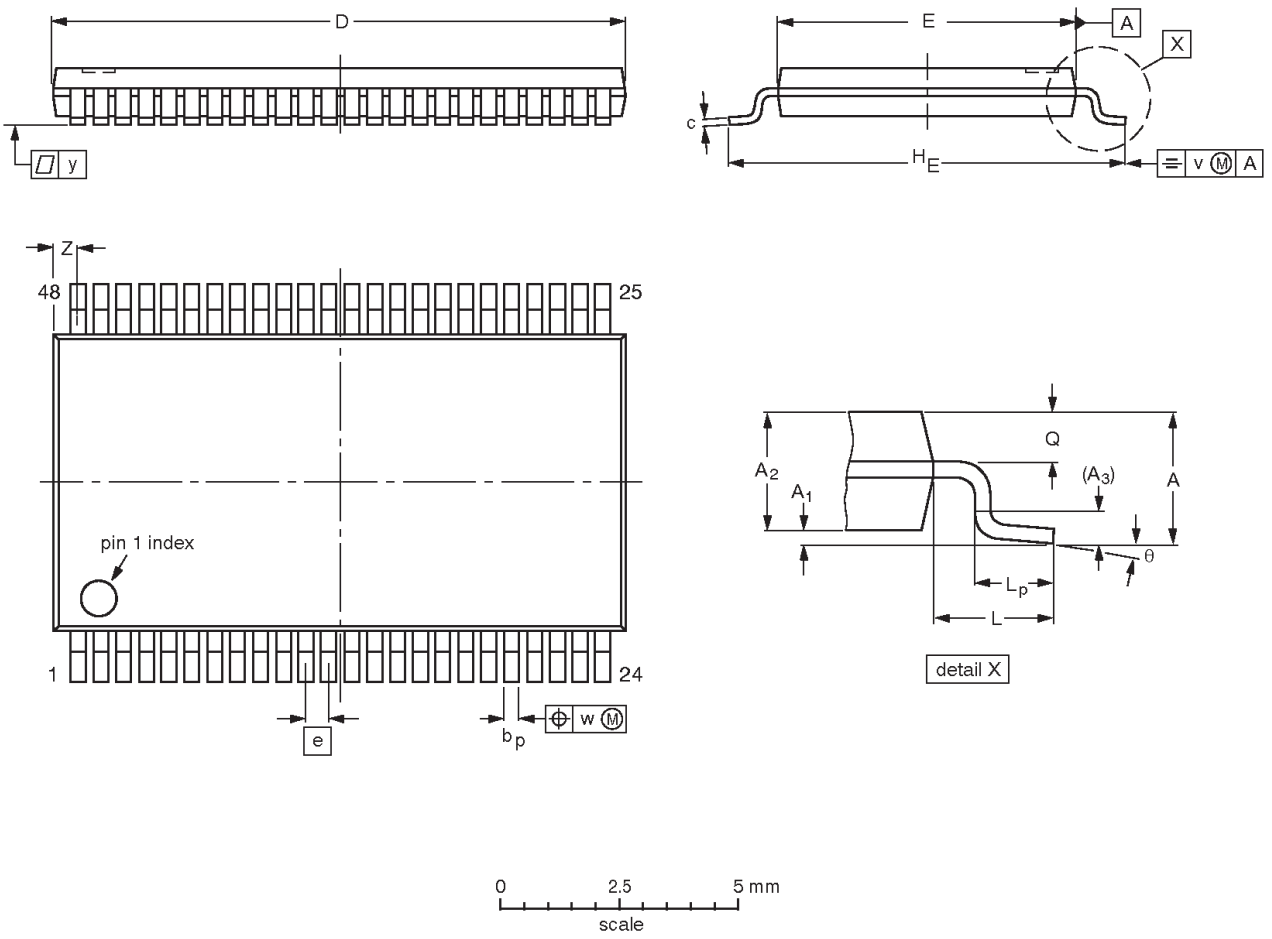
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT370-1		MO-118				~~99-12-27~~ 03-02-19

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~99-12-27~~ 03-02-19

REVISION HISTORY

Rev	Date	Description
_3	20040128	**Product data (9397 750 12819). 853-1807 ECN 01-A15431 of 27 January 2004.** **Replaces Product specification 74ABT16541_74ABTH16541_2 dated 1998 Feb 25 (9397 750 03495).** Modifications: • Delete all references to 74ABTH16541 (product discontinued). • Waveform 1 on page 6: corrected nYx waveform polarity.
_2	19980225	**Product specification (9397 750 03495). ECN 853-1807 19018 of 25 February 1998.** **Supersedes data of 1995 Sep 18.**

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Contact information

For additional information please visit
http://www.semiconductors.philips.com. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to:
sales.addresses@www.semiconductors.philips.com.

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