## DATA SHEET

## 74ABT162827A

 20-bit buffer/line driver, non-inverting, with $30 \Omega$ termination resistors (3-State)Product data

PHILIPS

## FEATURES

- Multiple $\mathrm{V}_{\mathrm{CC}}$ and GND pins minimize switching noise
- Live insertion/extraction permitted
- 3-State output buffers
- Power-up 3-State
- Output capability: +64 mA/-32 mA
- Latch-up protection exceeds 500 mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model


## DESCRIPTION

The 74ABT162827A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT162827A 20-bit buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. They have NOR Output Enables ( $\mathrm{nOE} 1, \mathrm{nOE} 2$ ) for maximum control flexibility.

The 74ABT162827A is designed with $30 \Omega$ series resistance in both the pull-up and pull-down output structures. This design reduces line noise in applications such as memory address drivers, clock drivers and bus receivers/transmitters.

## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS $\mathrm{T}_{\mathrm{amb}}=25^{\circ} \mathrm{C} ; \mathrm{GND}=0 \mathrm{~V}$ | TYPICAL | UNIT |
| :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \hline \text { tPLH } \\ & t_{\text {PHL }} \end{aligned}$ | Propagation delay nAx to nYx | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} ; \mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ | $\begin{aligned} & 1.8 \\ & 1.9 \end{aligned}$ | ns |
| $\mathrm{C}_{\text {IN }}$ | Input capacitance | $\mathrm{V}_{1}=0 \mathrm{~V}$ or $\mathrm{V}_{\mathrm{CC}}$ | 4 | pF |
| COUT | Output capacitance | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ or $\mathrm{V}_{\text {CC }} ; 3$-State | 6 | pF |
| ICCz | Quiescent supply current | Outputs disabled; $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$ | 500 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {CCL }}$ |  | Outputs LOW; $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$ | 9 | mA |

## ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | ORDER CODE | DWG NUMBER |
| :--- | :---: | :---: | :---: |
| 56-Pin Plastic SSOP Type III | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | $74 \mathrm{ABT162827ADL}$ | SOT371-1 |
| 56-Pin Plastic TSSOP Type II | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 74 ABT 162827 ADGG | SOT364-1 |

## PIN DESCRIPTION

| PIN NUMBER | SYMBOL | FUNCTION |
| :---: | :---: | :---: |
| $\begin{aligned} & 55,54,52,51,49,48,47,45,44,43, \\ & 42,41,40,38,37,36,34,33,31,30 \end{aligned}$ | $\begin{aligned} & \hline \text { 1A0 - 1A9 } \\ & 2 \mathrm{AO}-2 \mathrm{~A} 9 \end{aligned}$ | Data inputs |
| $\begin{gathered} 2,3,5,6,8,9,10,12,13,14 \\ 15,16,17,19,20,21,23,24,26,27 \end{gathered}$ | $\begin{aligned} & \hline \text { 1YO-1Y9 } \\ & 2 \mathrm{YO}-2 \mathrm{Y} 9 \end{aligned}$ | Data outputs |
| $\begin{aligned} & 1,56, \\ & 28,29 \end{aligned}$ | $\begin{aligned} & 1 \overline{\mathrm{OE}}, 1 \overline{\mathrm{OE}} 1 \\ & 2 \overline{\mathrm{OE}}, 2 \mathrm{OE} 1 \end{aligned}$ | Output enable inputs (Active-LOW) |
| 4, 11, 18, 25, 32, 39, 46, 53 | GND | Ground (0 V) |
| 7, 22, 35, 50 | $\mathrm{V}_{\mathrm{CC}}$ | Positive supply voltage |

20-bit buffer/line driver, non-inverting, with $30 \Omega$ termination resistors (3-State)

PIN CONFIGURATION


## LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)


FUNCTION TABLE

| INPUTS |  | OUTPUTS | OPERATING MODE |
| :---: | :---: | :---: | :---: |
| $\mathbf{n O E x}$ | $\mathbf{n A x}$ | $\mathbf{n Y x}$ |  |
| L | L | L | Transparent |
| L | H | H | Transparent |
| H | X | Z | High impedance |

[^0]20-bit buffer/line driver, non-inverting, with $30 \Omega$ termination resistors (3-State)

## SCHEMATIC OF Y OUTPUTS



## LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS ${ }^{1,2}$

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
| :---: | :--- | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | DC supply voltage |  | -0.5 to +7.0 | V |
| $\mathrm{I}_{\mathrm{IK}}$ | DC input diode current | $\mathrm{V}_{\mathrm{I}}<0 \mathrm{~V}$ | -18 | mA |
| $\mathrm{~V}_{\mathrm{I}}$ | DC input voltage ${ }^{3}$ |  | -1.2 to +7.0 | V |
| $\mathrm{I}_{\text {OK }}$ | DC output diode current | $\mathrm{V}_{\mathrm{O}}<0 \mathrm{~V}$ | -50 | mA |
| $\mathrm{~V}_{\text {OUT }}$ | DC output voltage ${ }^{3}$ | Output in Off or HIGH state | -0.5 to +5.5 | V |
| $\mathrm{I}_{\text {OUT }}$ | DC output current | Output in LOW state | 128 | mA |
|  |  | Output in HIGH state | -64 | mA |

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed $150^{\circ} \mathrm{C}$.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

20-bit buffer/line driver, non-inverting, with $30 \Omega$ termination resistors (3-State)

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS |  | UNIT |
| :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | DC supply voltage | 4.5 | 5.5 | V |
| $\mathrm{V}_{1}$ | Input voltage | 0 | $\mathrm{V}_{\mathrm{CC}}$ | V |
| $\mathrm{V}_{\mathrm{IH}}$ | HIGH-level input voltage | 2.0 | - | V |
| $\mathrm{V}_{\text {IL }}$ | LOW-level Input voltage | - | 0.8 | V |
| $\mathrm{IOH}^{\text {O }}$ | HIGH-level output current | - | -32 | mA |
| $\mathrm{I}_{\mathrm{OL}}$ | LOW-level output current | - | 12 | mA |
| $\Delta t / \Delta v$ | Input transition rise or fall rate | 0 | 10 | ns/V |
| $\mathrm{T}_{\mathrm{amb}}$ | Operating free-air temperature range | -40 | +85 | ${ }^{\circ} \mathrm{C}$ |

DC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS |  |  |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $\mathrm{T}_{\text {amb }}=+25^{\circ} \mathrm{C}$ |  |  | $\begin{gathered} \mathrm{T}_{\mathrm{amb}}=-40^{\circ} \mathrm{C} \\ \text { to }+85^{\circ} \mathrm{C} \end{gathered}$ |  |  |
|  |  |  | MIN | TYP | MAX | MIN | MAX |  |
| $\mathrm{V}_{\mathrm{IK}}$ | Input clamp voltage | $\mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V} ; \mathrm{I}_{\mathrm{IK}}=-18 \mathrm{~mA}$ |  | -0.9 | -1.2 |  | -1.2 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | HIGH-level output voltage | $\mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V} ; \mathrm{I}_{\mathrm{OH}}=-3 \mathrm{~mA} ; \mathrm{V}_{\mathrm{I}}=\mathrm{V}_{\mathrm{IL}}$ or $\mathrm{V}_{\mathrm{IH}}$ | 2.5 | 3.1 |  | 2.5 |  | V |
|  |  | $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V} ; \mathrm{I}_{\mathrm{OH}}=-3 \mathrm{~mA} ; \mathrm{V}_{\mathrm{I}}=\mathrm{V}_{\text {IL }}$ or $\mathrm{V}_{\mathrm{IH}}$ | 3.0 | 3.6 |  | 3.0 |  | V |
|  |  | $\mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V} ; \mathrm{I}_{\mathrm{OH}}=-32 \mathrm{~mA} ; \mathrm{V}_{\mathrm{I}}=\mathrm{V}_{\text {IL }}$ or $\mathrm{V}_{\text {IH }}$ | 2.0 | 2.7 |  | 2.0 |  | V |
| $\mathrm{V}_{\text {OL }}$ | LOW-level output voltage | $\mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V} ; \mathrm{l}_{\mathrm{OH}}=8 \mathrm{~mA} ; \mathrm{V}_{\mathrm{I}}=\mathrm{V}_{\mathrm{IL}}$ or $\mathrm{V}_{\mathrm{IN}}$ |  |  | 0.65 |  | 0.65 | V |
|  |  | $\mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V} ; \mathrm{l}_{\mathrm{OL}}=12 \mathrm{~mA} ; \mathrm{V}_{\mathrm{I}}=\mathrm{V}_{\mathrm{IL}}$ |  |  | 0.80 |  | 0.80 | V |
| 1 | Input leakage current | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V} ; \mathrm{V}_{\mathrm{I}}=\mathrm{GND}$ or 5.5 V |  | $\pm 0.01$ | $\pm 1.0$ |  | $\pm 1.0$ | $\mu \mathrm{A}$ |
| IOFF | Power-off leakage current | $\mathrm{V}_{\mathrm{CC}}=0.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{O}}=4.5 \mathrm{~V} ; \mathrm{V}_{\mathrm{I}}=0 \mathrm{~V}$ or 5.5 V |  | $\pm 5.0$ | $\pm 100$ |  | $\pm 100$ | $\mu \mathrm{A}$ |
| Ipu/lpd | Power-up/down 3-State output current ${ }^{3}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=2.1 \mathrm{~V} ; \mathrm{V}_{\mathrm{O}}=0.5 \mathrm{~V} ; \mathrm{V}_{\mathrm{I}}=\mathrm{GND} \text { or } \mathrm{V}_{\mathrm{CC}} ; \\ & \mathrm{V}_{\mathrm{OE}}=\text { Don't care } \end{aligned}$ |  | $\pm 5.0$ | $\pm 50$ |  | $\pm 50$ | $\mu \mathrm{A}$ |
| IOZH | 3-State output High current | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V} ; \mathrm{V}_{\mathrm{O}}=2.7 \mathrm{~V} ; \mathrm{V}_{\mathrm{I}}=\mathrm{V}_{\mathrm{IL}}$ or $\mathrm{V}_{\mathrm{IH}}$ |  | 1.0 | 10 |  | 10 | $\mu \mathrm{A}$ |
| Iozl | 3-State output Low current | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V} ; \mathrm{V}_{\mathrm{O}}=0.5 \mathrm{~V} ; \mathrm{V}_{\text {I }}=\mathrm{V}_{\text {IL }}$ or $\mathrm{V}_{\text {IH }}$ |  | -1.0 | -10 |  | -10 | $\mu \mathrm{A}$ |
| $I_{\text {CEX }}$ | Output High leakage current | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V} ; \mathrm{V}_{\mathrm{O}}=5.5 \mathrm{~V} ; \mathrm{V}_{\mathrm{I}}=\mathrm{GND}$ or $\mathrm{V}_{\mathrm{CC}}$ |  | 1.0 | 50 |  | 50 | $\mu \mathrm{A}$ |
| 10 | Output current ${ }^{1}$ | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V} ; \mathrm{V}_{\mathrm{O}}=2.5 \mathrm{~V}$ | -50 | -70 | -180 | -50 | -180 | mA |
| $\mathrm{I}_{\mathrm{CCH}}$ | Quiescent supply current | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$; Outputs HIGH, $\mathrm{V}_{\mathrm{I}}=\mathrm{GND}$ or $\mathrm{V}_{\mathrm{CC}}$ |  | 0.5 | 1 |  | 1 | mA |
| $\mathrm{I}_{\text {CCL }}$ |  | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$; Outputs LOW, $\mathrm{V}_{\mathrm{I}}=\mathrm{GND}$ or $\mathrm{V}_{\mathrm{CC}}$ |  | 9 | 19 |  | 19 | mA |
| ICCz |  | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$; Outputs 3-State; $\mathrm{V}_{\mathrm{I}}=$ GND or $\mathrm{V}_{\text {CC }}$ |  | 0.5 | 1 |  | 1 | mA |
| $\Delta_{\text {l }} \mathrm{C}$ | Additional supply current per input pin ${ }^{2}$ | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$; one input at 3.4 V , other inputs at $\mathrm{V}_{\mathrm{CC}}$ or GND |  | 0.2 | 1 |  | 1 | mA |

## NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4 V .
3. This parameter is valid for any $\mathrm{V}_{\mathrm{Cc}}$ between 0 V and 2.1 V with a transition time of up to 10 msec . From $\mathrm{V}_{\mathrm{CC}}=2.1 \mathrm{~V}$ to $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V} \pm 10 \%$ a transition time of up to $100 \mu \mathrm{sec}$ is permitted.

20-bit buffer/line driver, non-inverting, with $30 \Omega$ termination resistors (3-State)

AC CHARACTERISTICS
$\mathrm{GND}=0 \mathrm{~V}, \mathrm{t}_{\mathrm{R}}=\mathrm{t}_{\mathrm{F}}=2.5 \mathrm{~ns}, \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=500 \Omega$

| SYMBOL | PARAMETER | WAVEFORM | LIMITS |  |  |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $\begin{gathered} \mathrm{T}_{\mathrm{amb}}=+25^{\circ} \mathrm{C} \\ \mathrm{~V}_{\mathrm{CC}}=+5.0 \mathrm{~V} \end{gathered}$ |  |  | $\begin{gathered} \mathrm{T}_{\mathrm{amb}}=-40{ }^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\ \mathrm{~V}_{\mathrm{CC}}=+5.0 \mathrm{~V} \pm 0.5 \mathrm{~V} \end{gathered}$ |  |  |
|  |  |  | MIN | TYP | MAX | MIN | MAX |  |
| $\begin{aligned} & \hline \mathrm{t}_{\mathrm{PLH}} \\ & \mathrm{t}_{\mathrm{PHL}} \end{aligned}$ | Propagation delay nAx to nYx | 1 | $\begin{aligned} & 1.0 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & 1.8 \\ & 1.4 \end{aligned}$ | $\begin{aligned} & 2.6 \\ & 2.6 \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & 2.9 \\ & 2.9 \end{aligned}$ | ns |
| $\begin{aligned} & \hline \mathrm{t}_{\text {PZH }} \\ & \mathrm{t}_{\text {PZL }} \end{aligned}$ | Output enable time to High and Low level | 2 | $\begin{aligned} & 1.5 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & \hline 3.0 \\ & 3.6 \end{aligned}$ | $\begin{aligned} & 4.2 \\ & 4.9 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & \hline 5.2 \\ & 6.0 \end{aligned}$ | ns |
| $\begin{aligned} & \hline \mathrm{t}_{\mathrm{pHz}} \\ & \mathrm{t}_{\mathrm{pLZ}} \end{aligned}$ | Output disable time from High and Low level | 2 | $\begin{aligned} & 2.0 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & 3.4 \\ & 2.8 \end{aligned}$ | $\begin{aligned} & 4.8 \\ & 4.0 \end{aligned}$ | $\begin{aligned} & \hline 2.0 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & 5.4 \\ & 4.3 \end{aligned}$ | ns |

AC WAVEFORMS


Waveform 1. Input ( nAx ) to Output ( nYx ) Propagation Delays


Waveform 2. 3-State Output Enable and Disable Times

## TEST CIRCUIT AND WAVEFORM



20-bit buffer/line driver, non-inverting, with $30 \Omega$ termination resistors (3-State)


DIMENSIONS ( mm are the original dimensions)

| UNIT | $\mathbf{A}$ <br> max. | $\mathbf{A}_{\mathbf{1}}$ | $\mathbf{A}_{\mathbf{2}}$ | $\mathbf{A}_{\mathbf{3}}$ | $\mathbf{b}_{\mathbf{p}}$ | $\mathbf{c}$ | $\mathbf{D}^{(1)}$ | $\mathbf{E}^{(1)}$ | $\mathbf{e}$ | $\mathbf{H}_{\mathbf{E}}$ | $\mathbf{L}$ | $\mathbf{L}_{\mathbf{p}}$ | $\mathbf{Q}$ | $\mathbf{v}$ | $\mathbf{w}$ | $\mathbf{y}$ | $\mathbf{Z}^{(1)}$ | $\theta$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| mm | 2.8 | 0.4 | 2.35 | 0.25 | 0.3 | 0.22 | 18.55 | 7.6 | 0.635 | 10.4 | 1.4 | 1.0 | 1.2 | 0.25 | 0.18 | 0.1 | 0.85 | $8^{0}$ |
| 0.2 | 2.20 | 0.2 | 0.13 | 18.30 | 7.4 | 0.635 | 10.1 | 1.4 | 0.6 | 1.0 | 0.25 | $0^{0}$ |  |  |  |  |  |  |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE <br> VERSION | REFERENCES |  |  | EUROPEAN | ISSUE DATE |
| :--- | :---: | :---: | :---: | :---: | :---: |
|  | PROJECTION | EIAJ |  |  |  |
| SOT371-1 |  | JEDEC | MO-118 |  |  |

20-bit buffer/line driver, non-inverting, with $30 \Omega$ termination resistors (3-State)

detail X


DIMENSIONS (mm are the original dimensions).

| UNIT | $\underset{\text { max. }}{\mathrm{A}}$ | $\mathrm{A}_{1}$ | $\mathrm{A}_{2}$ | $\mathrm{A}_{3}$ | $\mathrm{b}_{\mathrm{p}}$ | c | $\mathrm{D}^{(1)}$ | $E^{(2)}$ | e | $\mathrm{H}_{\mathrm{E}}$ | L | $L_{p}$ | Q | v | w | y | Z | $\theta$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| mm | 1.2 | $\begin{aligned} & 0.15 \\ & 0.05 \end{aligned}$ | $\begin{aligned} & 1.05 \\ & 0.85 \end{aligned}$ | 0.25 | $\begin{aligned} & 0.28 \\ & 0.17 \end{aligned}$ | $\begin{aligned} & 0.2 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & 14.1 \\ & 13.9 \end{aligned}$ | $\begin{aligned} & 6.2 \\ & 6.0 \end{aligned}$ | 0.5 | $\begin{aligned} & 8.3 \\ & 7.9 \end{aligned}$ | 1.0 | $\begin{aligned} & 0.8 \\ & 0.4 \end{aligned}$ | $\begin{aligned} & 0.50 \\ & 0.35 \end{aligned}$ | 0.25 | 0.08 | 0.1 | 0.5 0.1 | $8^{0}$ $0^{\circ}$ |

## Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.


## Data sheet status

| Data sheet status ${ }^{[1]}$ | Product <br> status ${ }^{[2]}$ | Definitions |
| :--- | :--- | :--- |
| Objective data | Development | This data sheet contains data from the objective specification for product development. <br> Philips Semiconductors reserves the right to change the specification in any manner without notice. |
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Short-form specification - The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

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[^0]:    $X=$ Don't care
    Z = High impedance "off" state
    $\mathrm{H}=\mathrm{HIGH}$ voltage level
    L = LOW voltage level

