

DATA SHEET

74ABT162240

16-bit inverting buffer/driver with 30Ω
series termination resistors

Product data
Supersedes data of 1998 Feb 25

2004 Feb 18

16-bit inverting buffer/driver with 30Ω series termination resistors (3-State)

74ABT162240

FEATURES

- 16-bit bus interface
- 3-State buffers
- Output capability: +12mA/-32mA
- TTL input and output switching levels
- Live insertion/extraction permitted
- Power-up 3-State
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT162240 is a high-performance BiCMOS device which combines low static and dynamic power dissipation with high speed.

This device is an inverting 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables (1OE, 2OE, 3OE, 4OE), each controlling four of the 3-State outputs.

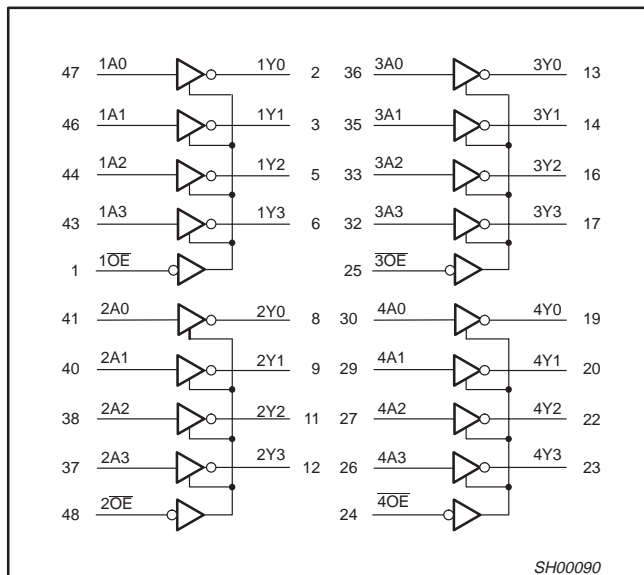
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T _{amb} = 25°C	TYPICAL	UNIT
t _{PLH} t _{PHL}	Propagation delay nAx to nYx	C _L = 50pF; V _{CC} =	2.7 2.6	ns
C _{IN}	Input capacitance nOE	V _I = 0V or 3.0V	4	pF
C _{OUT}	Output capacitance	Outputs disabled; V _O = 0V or	6	pF
I _{CCZ}	Quiescent supply current	Outputs disabled; V _{CC} =	500	μA
I _{CCL}		Outputs low; V _{CC} = 5.5V	8	mA

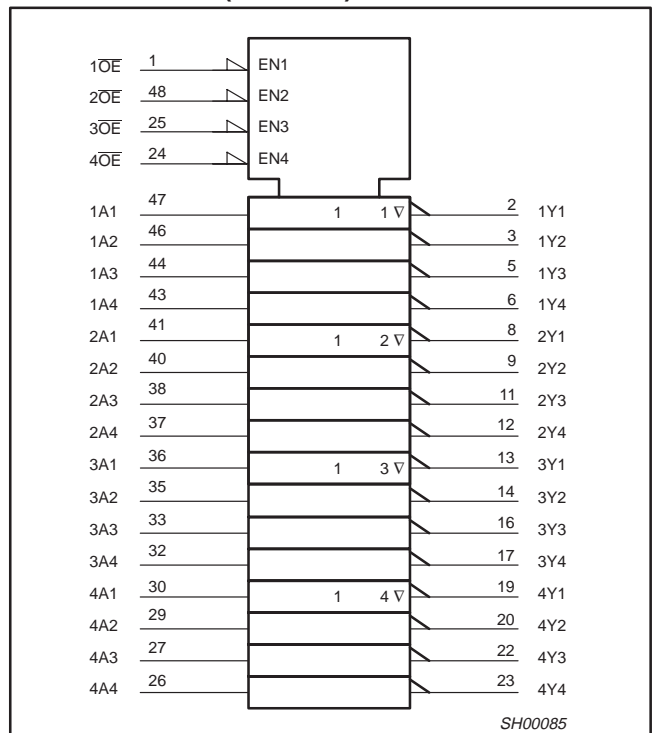
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	TYPE NUMBER	DWG NUMBER
48-Pin Plastic SSOP Type III	-40°C to +85°C	74ABT162240 DL	SOT370-1
48-Pin Plastic TSSOP Type II	-40°C to +85°C	74ABT162240 DGG	SOT362-1

LOGIC SYMBOL



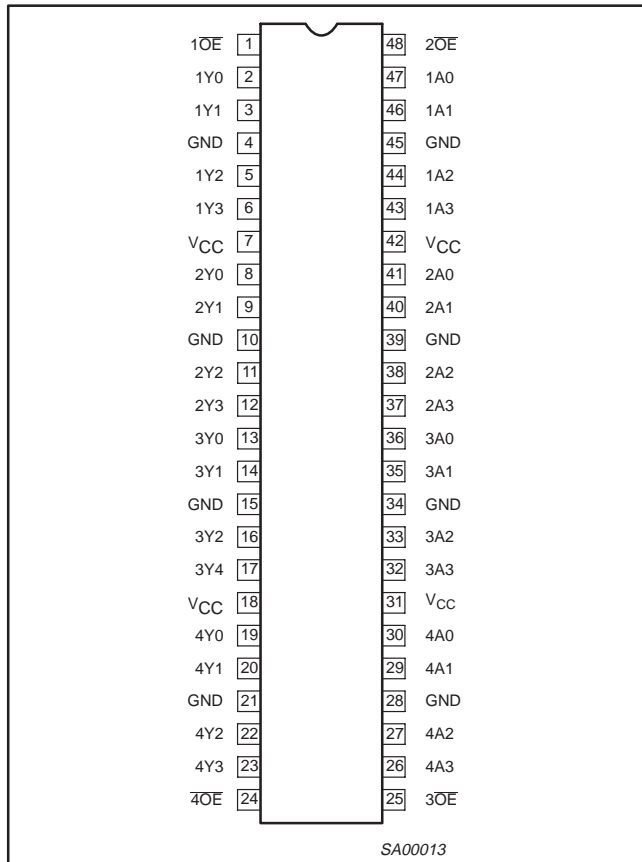
LOGIC SYMBOL (IEEE/IEC)



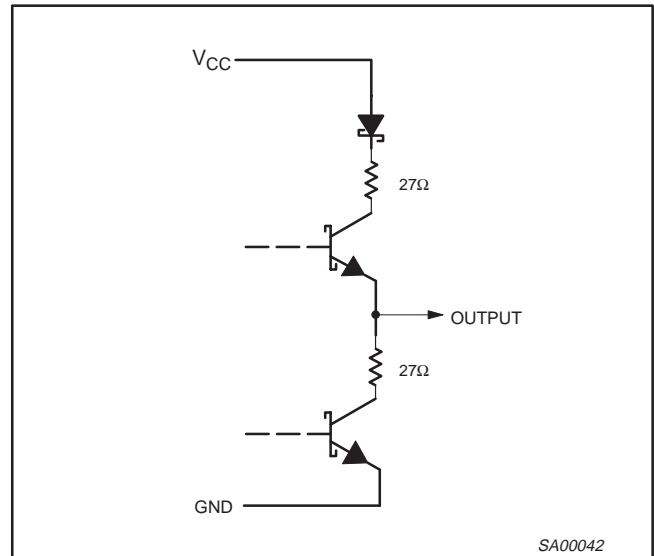
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PIN CONFIGURATION



SCHEMATIC OF Y OUTPUTS



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1A0-1A3 2A0-2A3 3A0-3A3 4A0-4A3	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1Y0-1Y3 2Y0-2Y3 3Y0-3Y3 4Y0-4Y3	Data outputs
1, 48, 25, 24	1OE, 2OE, 3OE, 4OE	Output enables
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V _{CC}	Positive supply voltage

FUNCTION TABLE

Inputs		Outputs
nOE	nAx	nYx
L	L	H
L	H	L
H	X	Z

H = High voltage level
 L = Low voltage level
 X = Don't care
 Z = High Impedance "off" state

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ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0	-18	mA
V _I	DC input voltage ³		-1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	-50	mA
V _{OUT}	DC output voltage ³	Output in Off or High state	-0.5 to +5.5	V
I _{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T _{stg}	Storage temperature range		-65 to +150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V _{CC}	DC supply voltage	4.5	5.5	V
V _I	Input voltage	0	V _{CC}	V
V _{IH}	High-level input voltage	2.0		V
V _{IL}	Input voltage		0.8	V
I _{OH}	High-level output current		-32	mA
I _{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		12	
Δt/Δv	Input transition rise or fall rate; Outputs enabled	0	10	ns/V
T _{amb}	Operating free-air temperature range	-40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _{amb} = +25°C			T _{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V _{IK}	Input clamp voltage	V _{CC} = 4.5V; I _{IK} = -18mA		-0.9	-1.2		-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 4.5V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}	2.5	2.9		2.5		V
		V _{CC} = 5.0V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}	3.0	3.4		3.0		V
		V _{CC} = 4.5V; I _{OH} = -32mA; V _I = V _{IL} or V _{IH}	2.0	2.4		2.0		V
V _{OL}	Low-level output voltage	V _{CC} = 4.5V; I _{OL} = 8mA; V _I = V _{IL} or V _{IH}			0.65		0.65	V
		V _{CC} = 4.5V; I _{OL} = 12mA; V _I = V _{IL} or V _{IH}			0.80		0.80	V
I _I	Input leakage current	V _{CC} = 5.5V; V _I = GND or 5.5V		±0.01	±1.0		±1.0	μA
I _{OFF}	Power-off leakage current	V _{CC} = 0.0V; V _O or V _I ≤ 4.5V		±5.0	±100		±100	μA
I _{PU} /I _{PD}	Power-up/down 3-State output current	V _{CC} = 2.0V; V _O = 0.5V; V _I = GND or V _{CC} ; V _{OE} = V _{CC}		±5.0	±50		±50	μA
I _{OZH}	3-State output High current	V _{CC} = 5.5V; V _O = 2.7V; V _I = V _{IL} or V _{IH}		1.0	10		10	μA
I _{OZL}	3-State output Low current	V _{CC} = 5.5V; V _O = 0.5V; V _I = V _{IL} or V _{IH}		-1.0	-10		-10	μA
I _{CEX}	Output high leakage current	V _{CC} = 5.5V; V _O = 5.5V; V _I = GND or V _{CC}		1.0	50		50	μA
I _O	Output current ¹	V _{CC} = 5.5V; V _O = 2.5V	-50	-70	-180	-50	-180	mA
I _{CCH}	Quiescent supply current	V _{CC} = 5.5V; Outputs High, V _I = GND or V _{CC}		0.5	1.0		1.0	mA
I _{CCL}		V _{CC} = 5.5V; Outputs Low, V _I = GND or V _{CC}		8	19		19	mA
I _{CCZ}		V _{CC} = 5.5V; Outputs 3-State; V _I = GND or V _{CC}		0.5	1.0		1.0	mA
ΔI _{CC}	Additional supply current per input pin ²	Outputs enabled, one input at 3.4V, other inputs at V _{CC} or GND; V _{CC} = 5.5V		10	200		200	μA

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.

AC CHARACTERISTICS

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = -40°C to +85°C.

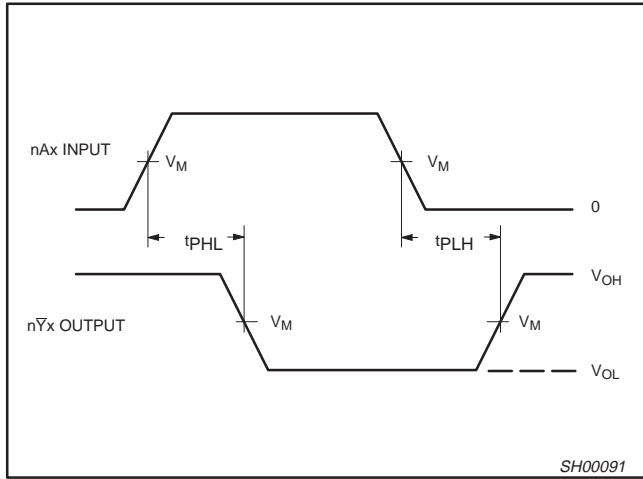
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V			T _{amb} = -40°C to +85°C V _{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay nAx to nYx	1	1.0 1.0	2.7 2.6	3.8 3.2	1.0 1.0	4.2 3.7	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	2	1.2 1.0	2.3 2.9	3.2 3.8	1.2 1.0	4.0 4.7	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	2	1.6 1.4	3.0 2.8	4.1 3.8	1.6 1.4	4.7 4.0	ns

AC WAVEFORMS

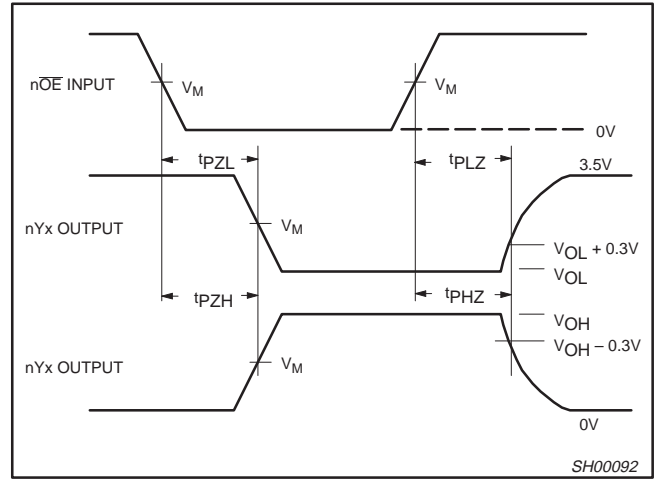
V_M = 1.5V, V_{IN} = GND to 2.7V

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Waveform 1. Input (nAx) to Output (nYx) Propagation Delays



Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS

Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t _{PLZ}	closed
t _{PZL}	7V
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

V_M = 1.5V
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t _W	t _R	t _F
74ABT16	3.0V	1MHz	500ns	2.5ns	2.5ns

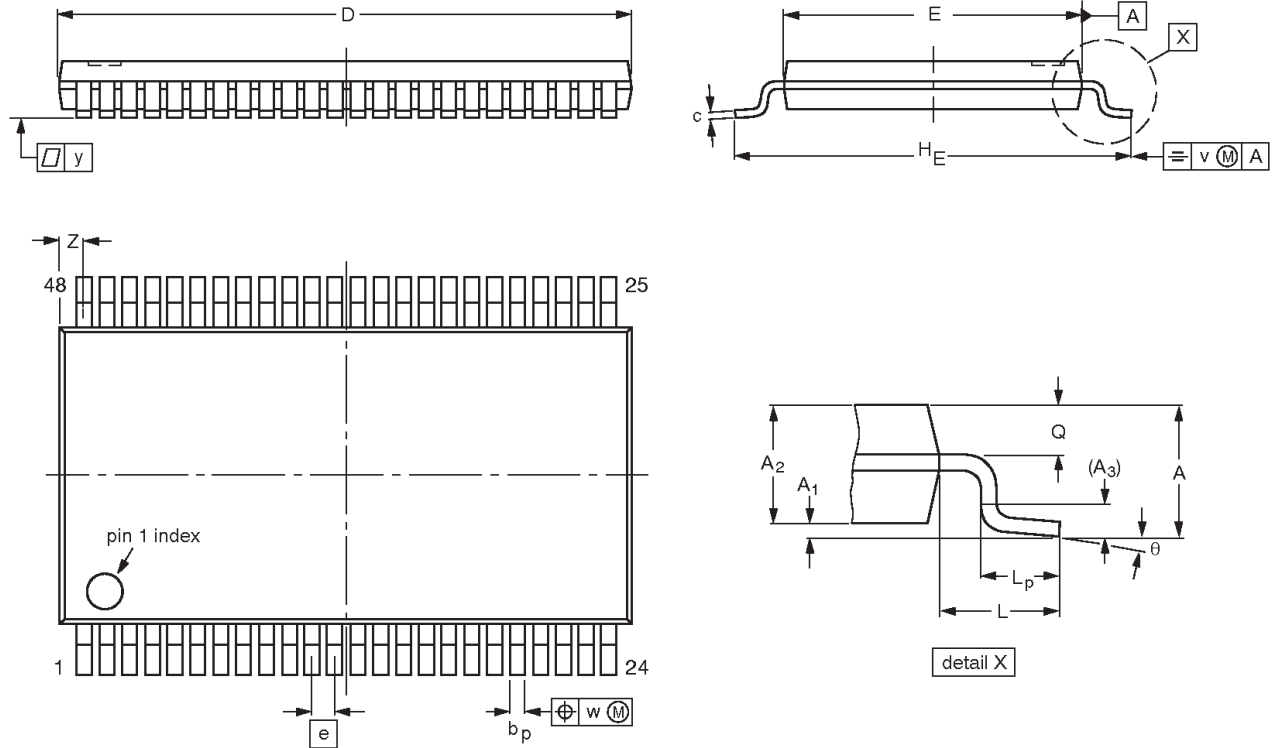
SH00093

16-bit inverting buffer/driver with 30Ω series termination resistors (3-State)

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TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

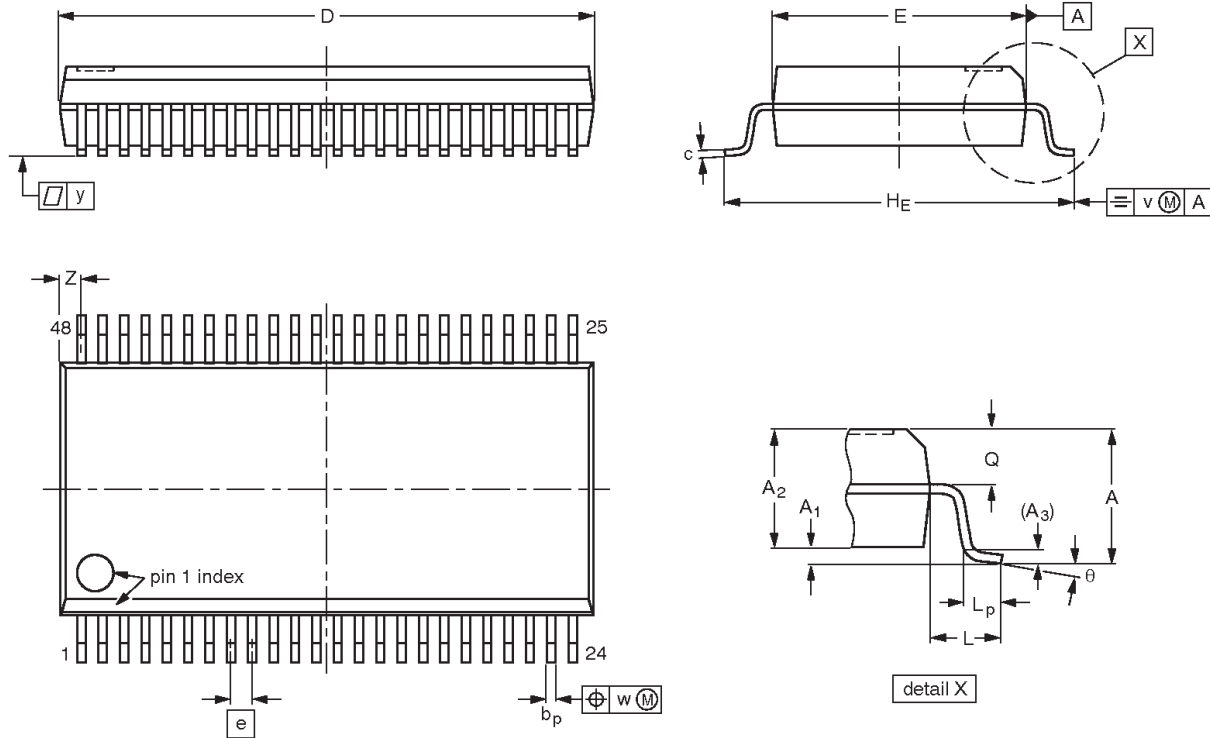
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				-99-12-27 03-02-19

16-bit inverting buffer/driver with 30Ω series termination resistors (3-State)

74ABT162240

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT370-1		MO-118				99-12-27 03-02-19

**16-bit inverting buffer/driver with 30Ω series
termination resistors (3-State)**

74ABT162240**REVISION HISTORY**

Rev	Date	Description
_4	20040218	Product data (9397 750 12935); 853-1825 ECN 01-A15419 of 26 January 2004. Supersedes data sheet 74ABT_H162240_3 of 1998 Feb 25 (9397 750 03482). Modifications: <ul style="list-style-type: none">• Delete all references to 74ABTH162240 (product discontinued).
_3	19980225	Product data (9397 750 03482); ECN 853-1825 19019 of 25 February 1998. Supersedes previous version.

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Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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