FAIRCHILD SEMICONDUCTOR™

August 2001
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74LCX32646
Low Voltage 32-Bit Transceiver/Register with 5V Tolerant Inputs and Outputs (Preliminary)

General Description

The LCX32646 contains thirty-two non-inverting bidirectional registered bus transceivers with 3-STATE outputs, providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Each byte has separate control inputs which can be shorted together for full 32-bit operation.The DIR_n inputs determine the direction of data flow through the device. The $CPAB_n$ and $CPBA_n$ inputs load data into the registers on the LOW-to-HIGH transition (see Functional Description).

The LCX32646 is designed for low voltage (2.5V or 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX32646 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- 2.3V–3.6V V_{CC} specifications provided
- 5.2 ns t_{PD} max (V_{CC} = 3.3V), 20 μA I_{CC} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- ±24 mA Output Drive (V_{CC} = 3.0V)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human Body Model > 2000V
  Machine Model > 200V
- Packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

Note 1: To ensure the high-impedance state during power up or down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

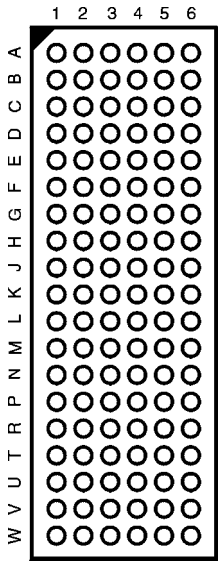
Ordering Code:

Order Number	Package Number	Package Description
74LCX32646GX (Note 2)	BGA114A (Preliminary)	114-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL]

Note 2: BGA package available in Tape and Reel only.

Connection Diagram

Pin Assignment for FBGA



(Top Thru View)

Pin Descriptions

Pin Names	Description
$1A_0$ - $1A_{15}$	Side A Inputs or 3-STATE Outputs
$2A_0$ - $2A_{15}$	
$1B_0$ - $1B_{15}$	Side B Inputs or 3-STATE Outputs
$2B_0$ - $2B_{15}$	
$\overline{OE}_n$	Output Enable Inputs
$CPAB_n$, $CPBA_n$	Clock Pulse Inputs
SAB_n, SBA_n	Select Inputs
DIR_n	Direction Control Inputs
NC	No Connect

FBGA Pin Assignments

	1	2	3	4	5	6
A	$1A_0$	SAB_1	$CPAB_1$	$CPBA_1$	SBA_1	$1B_0$
B	$1A_2$	$1A_1$	DIR_1	$\overline{OE}_1$	$1B_1$	$1B_2$
C	$1A_4$	$1A_3$	GND	GND	$1B_3$	1B4
D	$1A_6$	$1A_5$	V_{CC}	V_{CC}	$1B_5$	$1B_6$
E	$1A_8$	$1A_7$	GND	GND	$1B_7$	$1B_8$
F	$1A_{10}$	$1A_9$	GND	GND	$1B_9$	$1B_{10}$
G	$1A_{12}$	$1A_{11}$	V_{CC}	V_{CC}	$1B_{11}$	$1B_{12}$
H	$1A_{13}$	$1A_{14}$	GND	GND	$1B_{14}$	$1B_{13}$
J	$1A_{15}$	SAB_2	$CPAB_2$	$CPBA_2$	SBA_2	$1B_{15}$
K	NC	$CPAB_3$	DIR_2	$\overline{OE}_2$	$CPBA_3$	NC
L	$2A_0$	SAB_3	DIR_3	$\overline{OE}_3$	SBA_3	$2B_0$
M	$2A_2$	$2A_1$	GND	GND	$2B_1$	$2B_2$
N	$2A_4$	$2A_3$	V_{CC}	V_{CC}	$2B_3$	$2B_4$
P	$2A_6$	$2A_5$	GND	GND	$2B_5$	$2B_6$
R	$2A_8$	$2A_7$	GND	GND	$2B_7$	$2B_8$
T	$2A_{10}$	$2A_9$	V_{CC}	V_{CC}	$2B_9$	$2B_{10}$
U	$2A_{12}$	$2A_{11}$	GND	GND	$2B_{11}$	$2B_{12}$
V	$2A_{13}$	$2A_{14}$	$CPAB_4$	$CPBA_4$	$2B_{14}$	$2B_{13}$
W	$2A_{15}$	SAB_4	DIR_4	$\overline{OE}_4$	SBA_4	$2B_{15}$

Truth Table

(Note 3)

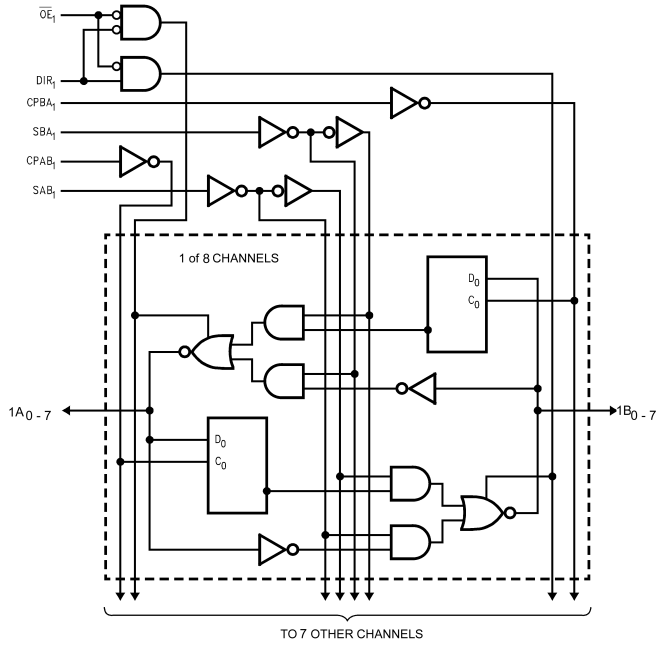
Inputs						Data I/O (Note 4)		Output Operation Mode
$\overline{OE}_1$	DIR_1	$CPAB_1$	$CPBA_1$	SAB_1	SBA_1	$1A_{0-7}$	$1B_{0-7}$	
H	X	H or L	H or L	X	X			Isolation
H	X	⌐	X	X	X	Input	Input	Clock A_n Data into A Register
H	X	X	⌐	X	X			Clock B_n Data Into B Register
L	H	X	X	L	X			A_n to B_n — Real Time (Transparent Mode)
L	H	⌐	X	L	X	Input	Output	Clock A_n Data to A Register
L	H	H or L	X	H	X			A Register to B_n (Stored Mode)
L	H	⌐	X	H	X			Clock A_n Data into A Register and Output to B_n
L	L	X	X	X	L			B_n to A_n — Real Time (Transparent Mode)
L	L	X	⌐	X	L	Output	Input	Clock B_n Data into B Register
L	L	X	H or L	X	H			B Register to A_n (Stored Mode)
L	L	X	⌐	X	H			Clock B_n into B Register and Output to A_n

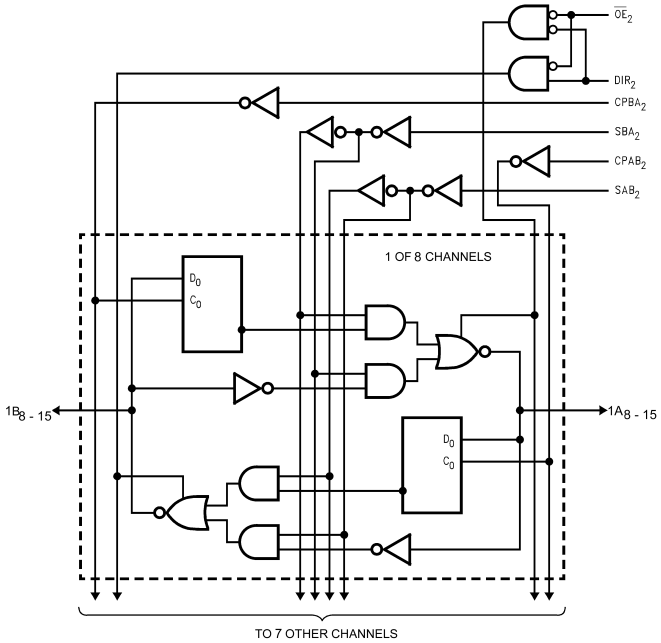
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition

Note 3: Data I/O paths (1A and 1B: 0 - 7) is shown. This also applies to data I/O (1A and 1B: 8 - 15) and #2 control pins, to data (2A and 2B: 0 - 7) and #3 control pins, to data (2A and 2B: 8 - 15) and #4 control pins.

Note 4: The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

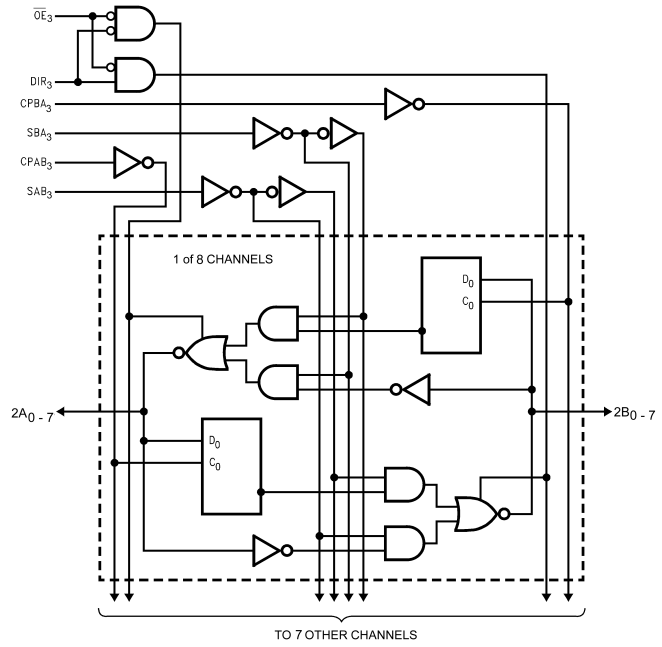
Logic Diagrams

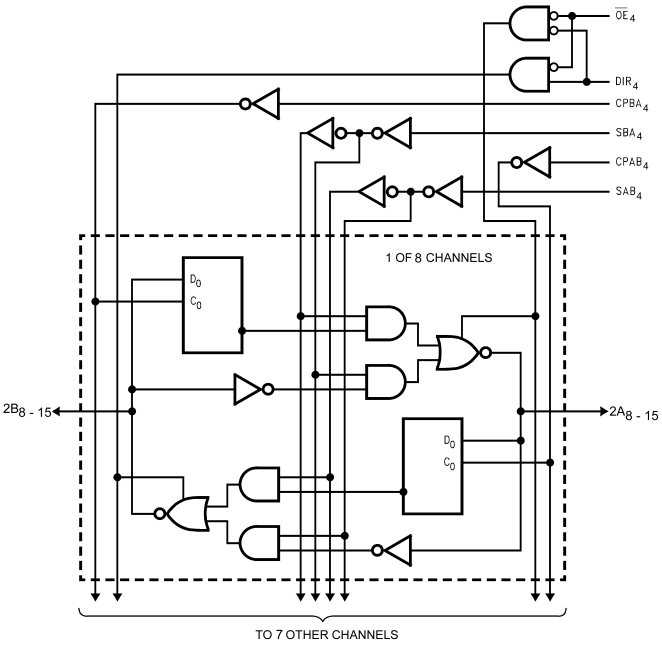




Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Logic Diagrams (Continued)





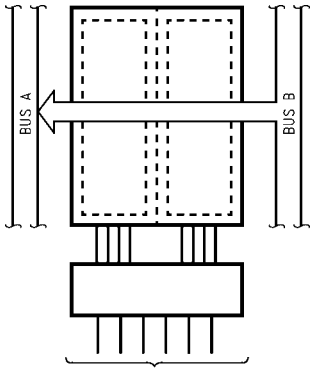
Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both. The select (SAB_n, SBA_n) controls can multiplex stored and real-time. The examples shown below demonstrate the four fundamental bus-management functions that can be performed for data I/O 1A and 1B: 0 - 7.

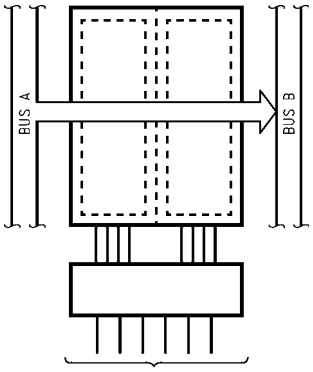
The direction control (DIR_n) determines which bus will receive data when $\overline{OE}_n$ is LOW. In the isolation mode ($\overline{OE}_n$ HIGH), A data may be stored in one register and/or B data may be stored in the other register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two busses, A or B, may be driven at a time.

Real-Time Transfer
Bus B to Bus A



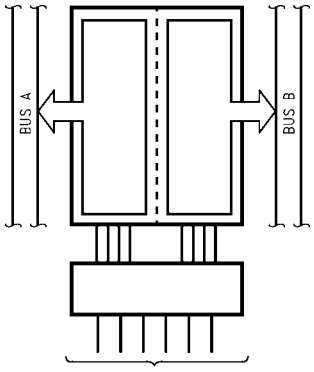
$\overline{OE}_1$	DIR_1	$CPAB_1$	$CPBA_1$	SAB_1	SBA_1
L	L	X	X	X	L

Real-Time Transfer
Bus A to Bus B



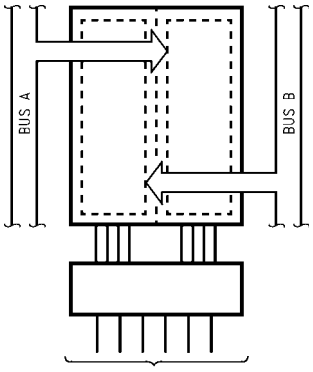
$\overline{OE}_1$	DIR_1	$CPAB_1$	$CPBA_1$	SAB_1	SBA_1
L	H	X	X	L	X

Transfer Storage
Data to A or B



$\overline{OE}_1$	DIR_1	$CPAB_1$	$CPBA_1$	SAB_1	SBA_1
L	L	X	H or L	X	H
L	H	H or L	X	H	X

Storage



$\overline{OE}_1$	DIR_1	$CPAB_1$	$CPBA_1$	SAB_1	SBA_1
L	H	⌐	X	L	X
L	X	X	⌐	X	L
H	X	⌐	X	X	X
H	X	X	⌐	X	X

Absolute Maximum Ratings(Note 5)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0 −0.5 to V_{CC} + 0.5	Output in 3-STATE Output in HIGH or LOW State (Note 6)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions (Note 7)

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		3-STATE	0	5.5	
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V – 3.6V		±24	mA
		V_{CC} = 2.7V – 3.0V		±12	
		V_{CC} = 2.3V – 2.7V		±8	
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

Note 5: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 6: I_O Absolute Maximum Rating must be observed.

Note 7: Unused inputs and I/Os must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.3 – 2.7	1.7		V
			2.7 – 3.6	2.0		
V_{IL}	LOW Level Input Voltage		2.3 – 2.7		0.7	V
			2.7 – 3.6		0.8	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 µA	2.3 – 3.6	V_{CC} – 0.2		V
		I_{OH} = −8 mA	2.3	1.8		
		I_{OH} = −12 mA	2.7	2.2		
		I_{OH} = −18 mA	3.0	2.4		
		I_{OH} = −24 mA	3.0	2.2		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA	2.3 – 3.6		0.2	V
		I_{OL} = 8 mA	2.3		0.6	
		I_{OL} = 12 mA	2.7		0.4	
		I_{OL} = 16 mA	3.0		0.4	
		I_{OL} = 24 mA	3.0		0.55	
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.3 – 3.6		±5.0	µA
I_{OZ}	3-STATE I/O Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.3 – 3.6		±5.0	µA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	µA

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40°C$ to $+85°C$		Units
				Min	Max	
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.3 – 3.6		20	µA
		$3.6V \le V_I, V_O \le 5.5V$ (Note 8)	2.3 – 3.6		±20	
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.3 – 3.6		500	µA

Note 8: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $R_L = 500\Omega$						Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		$V_{CC} = 2.5V \pm 0.2V$		
		$C_L = 50$ pF		$C_L = 50$ pF		$C_L = 30$ pF		
		Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	170						ns
t_{PHL}	Propagation Delay	1.5	5.2	1.5	6.0	1.5	6.2	ns
t_{PLH}	Bus to Bus	1.5	5.2	1.5	6.0	1.5	6.2	
t_{PHL}	Propagation Delay	1.5	6.0	1.5	7.0	1.5	7.2	ns
t_{PLH}	Clock to Bus	1.5	6.0	1.5	7.0	1.5	7.2	
t_{PHL}	Propagation Delay	1.5	6.0	1.5	7.0	1.5	7.2	ns
t_{PLH}	Select to Bus	1.5	6.0	1.5	7.0	1.5	7.2	
t_{PZL}	Output Enable Time	1.5	7.5	1.5	8.5	1.5	9.8	ns
t_{PZH}		1.5	7.5	1.5	8.5	1.5	9.8	
t_{PLZ}	Output Disable Time	1.5	6.5	1.5	7.5	1.5	7.8	ns
t_{PHZ}		1.5	6.5	1.5	7.5	1.5	7.8	
t_S	Setup Time	2.5		2.5		3.0		ns
t_H	Hold Time	1.5		1.5		2.0		ns
t_W	Pulse Width	3.0		3.0		3.5		ns

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
		$C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$	2.5	0.6	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	–0.8	V
		$C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$	2.5	–0.6	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10 MHz	20	pF

AC LOADING and WAVEFORMS Generic for LCX Family

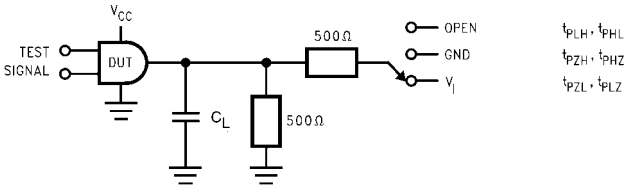
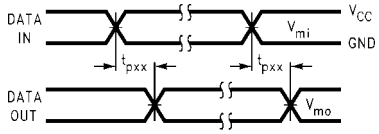
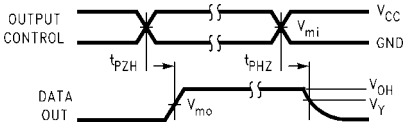


FIGURE 1. AC Test Circuit (C_L includes probe and jig capacitance)

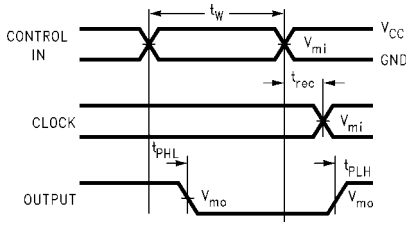
Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 ± 0.3V, and 2.7V V_{CC} x 2 at V_{CC} = 2.5 ± 0.2V
t_{PZH}, t_{PHZ}	GND



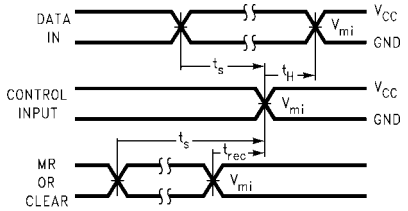
Waveform for Inverting and Non-Inverting Functions



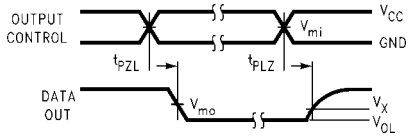
3-STATE Output High Enable and Disable Times for Logic



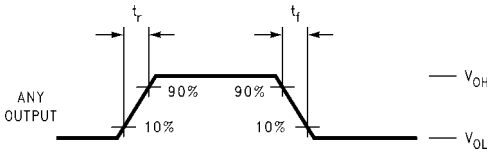
Propagation Delay. Pulse Width and t_{rec} Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output Low Enable and Disable Times for Logic

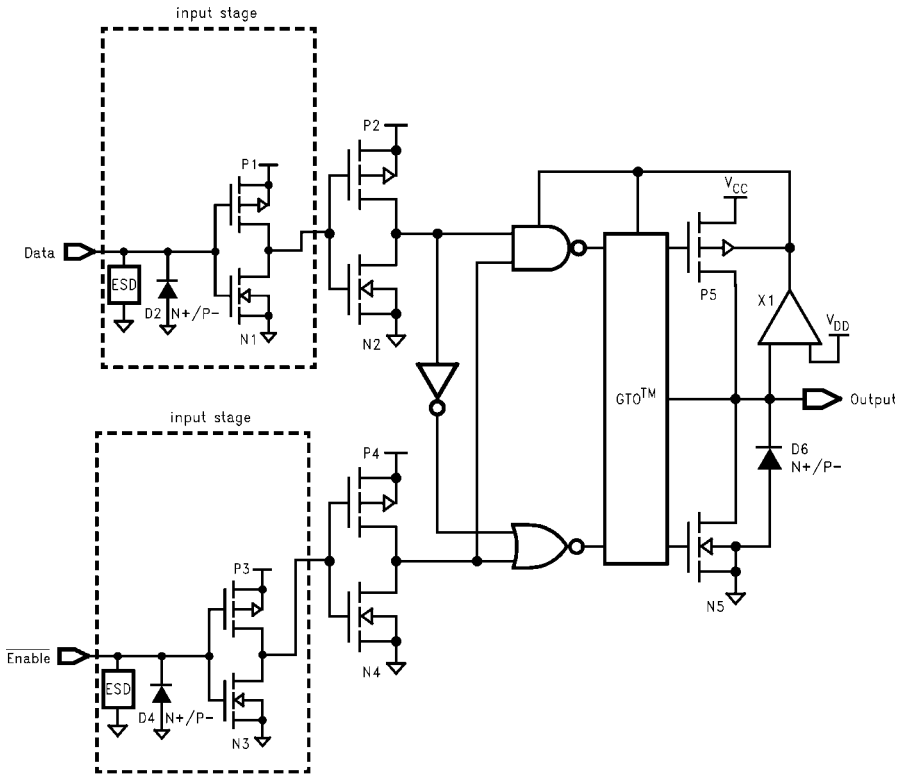


t_{rise} and t_{fall}

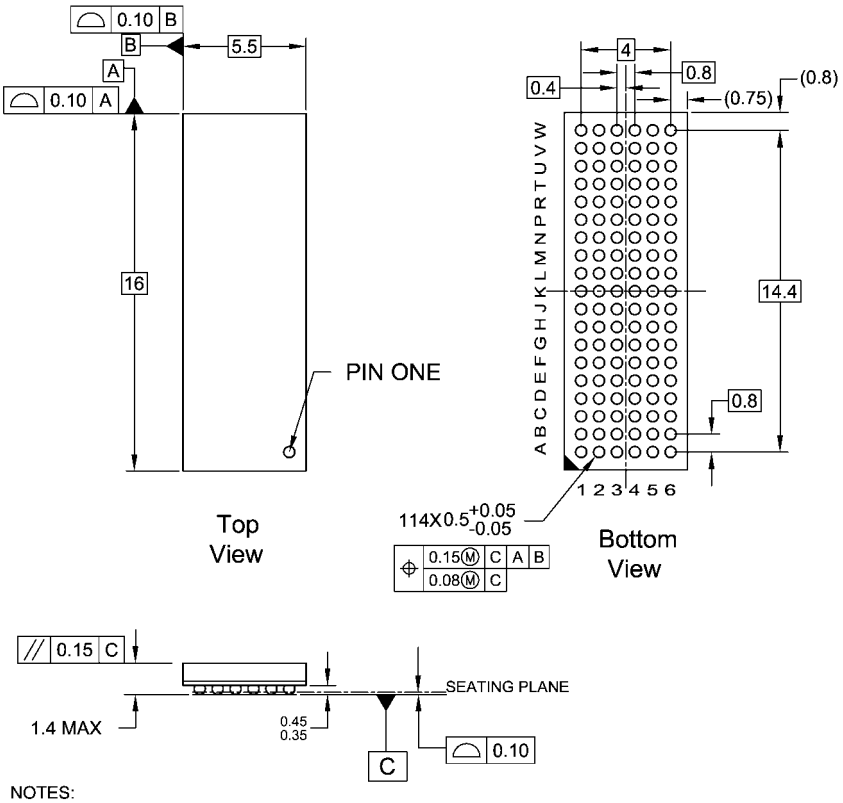
FIGURE 2. Waveforms
(Input Characteristics; f =1MHz, t_r = t_f = 3ns)

Symbol	V_{CC}		
	3.3V ± 0.3V	2.7V	2.5V ± 0.2V
V_{mi}	1.5V	1.5V	V_{CC}/2
V_{mo}	1.5V	1.5V	V_{CC}/2
V_x	V_{OL} + 0.3V	V_{OL} + 0.3V	V_{OL} + 0.15V
V_y	V_{OH} − 0.3V	V_{OH} − 0.3V	V_{OH} − 0.15V

Schematic Diagram Generic for LCX Family



Physical Dimensions inches (millimeters) unless otherwise noted



NOTES:

A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA114ArevE

114-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA114A
Preliminary

LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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