

To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

MITSUBISHI MICROCOMPUTERS

M35046-XXXSP/FP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

DESCRIPTION

The M35046-XXXSP/FP is a character pattern display control IC can display on the liquid crystal display and the plasma display. It uses a silicon gate CMOS process and it housed in a 20-pin shrink DIP package (M35046-XXXSP) or a 20-pin shrink SOP package (M35046-XXXFP).

For M35046-001SP/FP that is a standard ROM version of M35046-XXXSP/FP respectively, the character pattern is also mentioned.

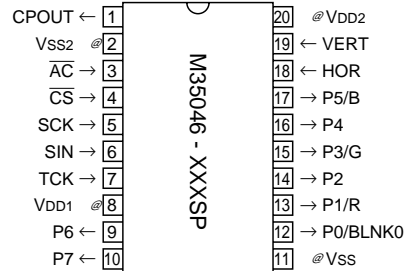
FEATURES

- Screen composition 24 columns × 12 lines
- Number of characters displayed 288 (Max.)
- Character composition 12 × 18 dot matrix
- Characters available 256 characters
- Character sizes available 4 (horizontal) × 4 (vertical)
- Display locations available
 - Horizontal direction 1000 locations
 - Vertical direction 1023 locations
- Blinking Character units
 - Cycle : division of vertical synchronization signal into 32 or 64
 - Duty : 25%, 50%, or 75%
- Data input By the 16-bit serial input function
- Coloring
 - Character color Character unit
 - Background coloring Character unit
 - Matrix-outline (shadow) coloring 8 colors (RGB output)
 - Specified by register
 - Border coloring 8 colors (RGB output)
 - Specified by register
 - Raster coloring 8 colors (RGB output)
 - Specified by register
- Blanking
 - Character size blanking
 - Border size blanking
 - Matrix-outline blanking
 - All blanking (all raster area)
- Output ports
 - 4 shared output ports (toggled between RGB output)
 - 4 dedicated output ports
- Display RAM erase function
- Display input frequency range $F_{osc} = 20\text{MHz to } 80\text{MHz}$
- Horizontal synchronous input frequency
 - $H_{sync} = 15\text{ kHz to } 130\text{ kHz}$
- Display oscillation stop function

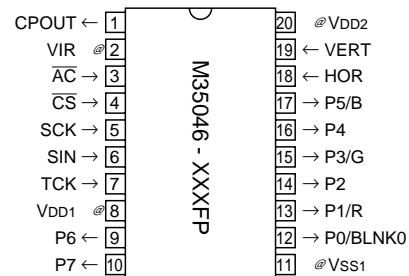
APPLICATION

Liquid crystal display, Plasma display, Video projector

PIN CONFIGURATION (TOP VIEW)

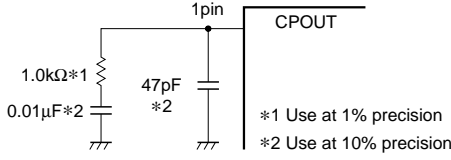


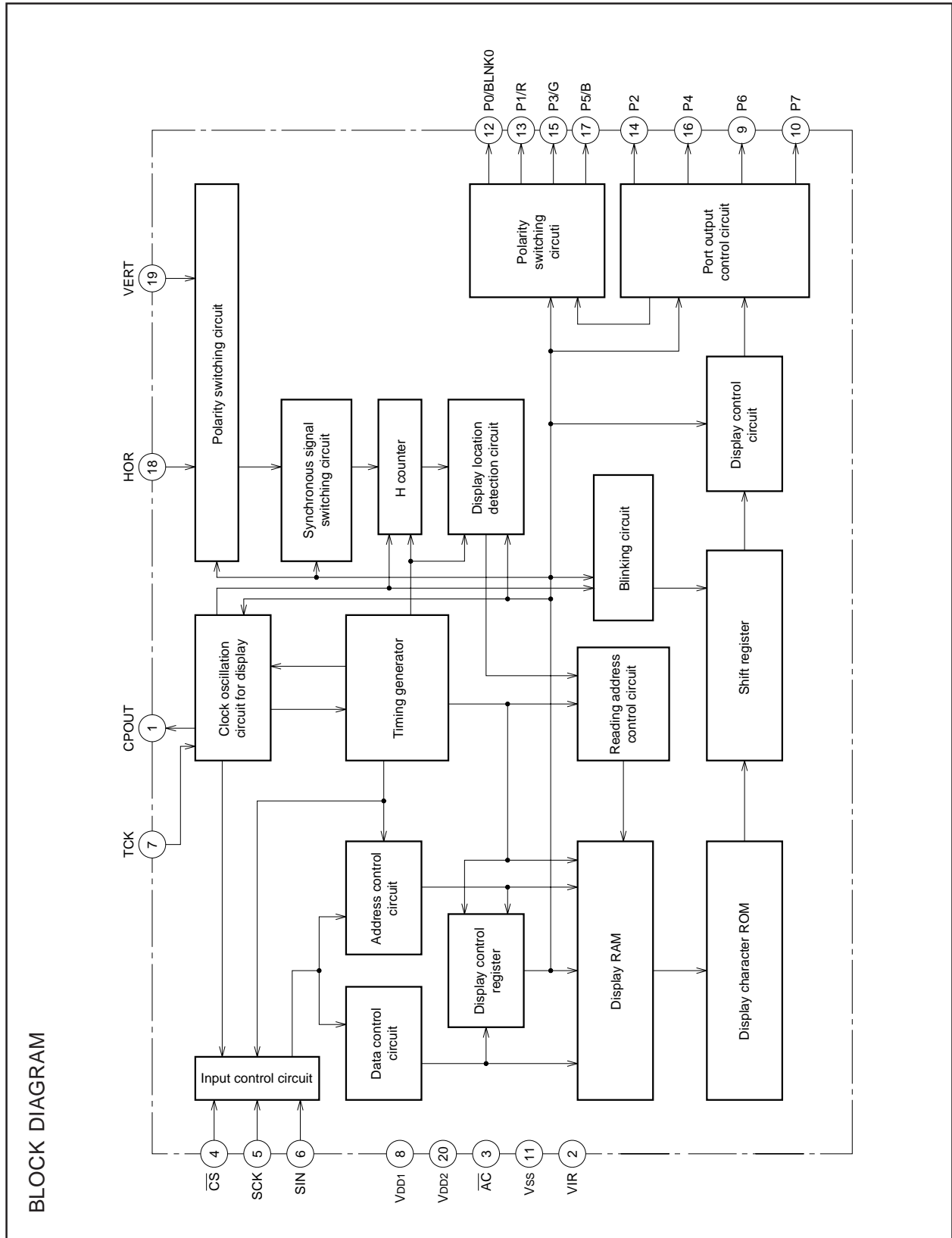
Outline 20P4B



Outline 20P2Q-A

PIN DESCRIPTION

| Pin Number | Symbol | Pin name | Input/Output | Function |
|------------|-----------------|-------------------------------------|--------------|--|
| 1 | CPOUT | Phase difference | Output | <p>Connect loop filter to this pin.</p>  <p>*1 Use at 1% precision *2 Use at 10% precision</p> |
| 2 | VSS2 | Earthing pin | – | Connect to GND. |
| 3 | \overline{AC} | Auto-clear input | Input | When “L”, this pin resets the internal IC circuit. Hysteresis input. Built-in pull-up resistor. |
| 4 | CS | Chip select input | Input | This is the chip select input pin, and when serial data transmission is being carried out, it goes to “L”. Hysteresis input. Built-in pull-up resistor. |
| 5 | SCK | Serial clock input | Input | When \overline{CS} pin is “L”, SIN serial data is taken in when SCK rises. Hysteresis input. Built-in pull-up resistor. |
| 6 | SIN | Serial data input | Input | This is the pin for serial input of data and addresses for the display control register and the display data memory. Hysteresis input. Built-in pull-up resistor. |
| 7 | TCK | External clock | Input | This is the pin for external clock input. |
| 8 | VDD1 | Power pin | – | Please connect to +5V with the power pin. |
| 9 | P6 | Port P6 output | Output | This is the output port. Port data is set by PTD6. |
| 10 | P7 | Port P7 output | Output | This is the output port. Port data is set by PTD7. |
| 11 | VSS1 | Earthing pin | – | Please connect to GND using circuit earthing pin. |
| 12 | P0/BLNK0 | Port P0 output | Output | This pin can be toggled between port pin output and BLNK0 signal output. |
| 13 | P1/R | Port P1 output | Output | This pin can be toggled between port pin output and R signal output. |
| 14 | P2 | Port P2 output | Output | This is the output port. Port data is set by PTD2. |
| 15 | P3/G | Port P3 output | Output | This pin can be toggled between port pin output and G signal output. |
| 16 | P4 | Port P4 output | Output | This is the output port. Port data is set by PTD4. |
| 17 | P5/B | Port P5 output | Output | This pin can be toggled between port pin output and B signal output. |
| 18 | HOR | Horizontal synchronous signal input | Input | This pin inputs the horizontal synchronous signal. Hysteresis input. |
| 19 | VERT | Vertical synchronous signal input | Input | This pin inputs the vertical synchronous signal. Hysteresis input. |
| 20 | VDD2 | Power pin | – | Please connect to +5V with the power pin. |



SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

MEMORY CONSTITUTION

Address 000₁₆ to 11F₁₆ are assigned to the display RAM, address 120₁₆ to 128₁₆ are assigned to the display control registers. The internal circuit is reset and all display control registers (address 120₁₆ to 128₁₆) are set to "0" when the \overline{AC} pin level is "L". And then RAM is erased.

Memory constitution is shown in Figure 1.

SCREEN CONSTITUTION

The screen lines and rows are determined from each address of the display RAM. The screen constitution is shown in Figure 2.

| | DAF | DAE | DAD | DAC | DAB | DAA | DA9 | DA8 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 |
|-------------------|-----|---------------------|--------|--------|----------|-----------------|--------|--------|----------------|-------|-------|-------|-------|-------|-------|-------|
| 000 ₁₆ | 0 | BB | BG | BR | BLINK | B | G | R | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| ⋮ | ⋮ | Background coloring | | | Blinking | Character color | | | Character code | | | | | | | |
| 11F ₁₆ | 0 | BB | BG | BR | BLINK | B | G | R | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 120 ₁₆ | 0 | EXCK0 | VJT | DIVS1 | DIVS0 | DIV10 | DIV9 | DIV8 | DIV7 | DIV6 | DIV5 | DIV4 | DIV3 | DIV2 | DIV1 | DIV0 |
| 121 ₁₆ | 0 | RSELO | PTD7 | PTD6 | PTD5 | PTD4 | PTD3 | PTD2 | PTD1 | PTD0 | PTC5 | PTC4 | PTC3 | PTC2 | PTC1 | PTC0 |
| 122 ₁₆ | 0 | RSEL1 | SPACE2 | SPACE1 | SPACE0 | TEST9 | HP9 | HP8 | HP7 | HP6 | HP5 | HP4 | HP3 | HP2 | HP1 | HP0 |
| 123 ₁₆ | 0 | EXCK1 | TEST3 | TEST2 | TEST1 | TEST0 | VP9 | VP8 | VP7 | VP6 | VP5 | VP4 | VP3 | VP2 | VP1 | VP0 |
| 124 ₁₆ | 0 | TEST14 | TEST5 | TEST4 | DSP11 | DSP10 | DSP9 | DSP8 | DSP7 | DSP6 | DSP5 | DSP4 | DSP3 | DSP2 | DSP1 | DSP0 |
| 125 ₁₆ | 0 | TEST10 | VSZ1H1 | VSZ1H0 | VSZ1L1 | VSZ1L0 | V1SZ1 | V1SZ0 | LIN9 | LIN8 | LIN7 | LIN6 | LIN5 | LIN4 | LIN3 | LIN2 |
| 126 ₁₆ | 0 | TEST11 | VSZ2H1 | VSZ2H0 | VSZ2L1 | VSZ2L0 | V18SZ1 | V18SZ0 | LIN17 | LIN16 | LIN15 | LIN14 | LIN13 | LIN12 | LIN11 | LIN10 |
| 127 ₁₆ | 0 | TEST12 | HSZ21 | HSZ20 | HSZ11 | HSZ10 | BETA14 | TEST8 | TEST7 | TEST6 | FB | FG | FR | RB | RG | RR |
| 128 ₁₆ | 0 | TEST13 | BLINK2 | BLINK1 | BLINK0 | DSPON | STOP | RAMERS | SYAD | BLK1 | BLK0 | POLH | POLV | VMASK | B/F | BCOL |

Fig. 1 Memory constitution

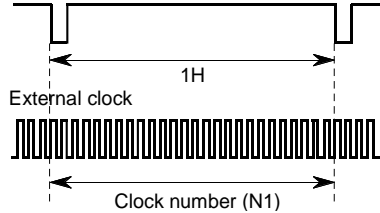
| Row Line | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |
|----------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| 1 | 000 ₁₆ | 001 ₁₆ | 002 ₁₆ | 003 ₁₆ | 004 ₁₆ | 005 ₁₆ | 006 ₁₆ | 007 ₁₆ | 008 ₁₆ | 009 ₁₆ | 00A ₁₆ | 00B ₁₆ | 00C ₁₆ | 00D ₁₆ | 00E ₁₆ | 00F ₁₆ | 010 ₁₆ | 011 ₁₆ | 012 ₁₆ | 013 ₁₆ | 014 ₁₆ | 015 ₁₆ | 016 ₁₆ | 017 ₁₆ |
| 2 | 018 ₁₆ | 019 ₁₆ | 01A ₁₆ | 01B ₁₆ | 01C ₁₆ | 01D ₁₆ | 01E ₁₆ | 01F ₁₆ | 020 ₁₆ | 021 ₁₆ | 022 ₁₆ | 023 ₁₆ | 024 ₁₆ | 025 ₁₆ | 026 ₁₆ | 027 ₁₆ | 028 ₁₆ | 029 ₁₆ | 02A ₁₆ | 02B ₁₆ | 02C ₁₆ | 02D ₁₆ | 02E ₁₆ | 02F ₁₆ |
| 3 | 030 ₁₆ | 031 ₁₆ | 032 ₁₆ | 033 ₁₆ | 034 ₁₆ | 035 ₁₆ | 036 ₁₆ | 037 ₁₆ | 038 ₁₆ | 039 ₁₆ | 03A ₁₆ | 03B ₁₆ | 03C ₁₆ | 03D ₁₆ | 03E ₁₆ | 03F ₁₆ | 040 ₁₆ | 041 ₁₆ | 042 ₁₆ | 043 ₁₆ | 044 ₁₆ | 045 ₁₆ | 046 ₁₆ | 047 ₁₆ |
| 4 | 048 ₁₆ | 049 ₁₆ | 04A ₁₆ | 04B ₁₆ | 04C ₁₆ | 04D ₁₆ | 04E ₁₆ | 04F ₁₆ | 050 ₁₆ | 051 ₁₆ | 052 ₁₆ | 053 ₁₆ | 054 ₁₆ | 055 ₁₆ | 056 ₁₆ | 057 ₁₆ | 058 ₁₆ | 059 ₁₆ | 05A ₁₆ | 05B ₁₆ | 05C ₁₆ | 05D ₁₆ | 05E ₁₆ | 05F ₁₆ |
| 5 | 060 ₁₆ | 061 ₁₆ | 062 ₁₆ | 063 ₁₆ | 064 ₁₆ | 065 ₁₆ | 066 ₁₆ | 067 ₁₆ | 068 ₁₆ | 069 ₁₆ | 06A ₁₆ | 06B ₁₆ | 06C ₁₆ | 06D ₁₆ | 06E ₁₆ | 06F ₁₆ | 070 ₁₆ | 071 ₁₆ | 072 ₁₆ | 073 ₁₆ | 074 ₁₆ | 075 ₁₆ | 076 ₁₆ | 077 ₁₆ |
| 6 | 078 ₁₆ | 079 ₁₆ | 07A ₁₆ | 07B ₁₆ | 07C ₁₆ | 07D ₁₆ | 07E ₁₆ | 07F ₁₆ | 080 ₁₆ | 081 ₁₆ | 082 ₁₆ | 083 ₁₆ | 084 ₁₆ | 085 ₁₆ | 086 ₁₆ | 087 ₁₆ | 088 ₁₆ | 089 ₁₆ | 08A ₁₆ | 08B ₁₆ | 08C ₁₆ | 08D ₁₆ | 08E ₁₆ | 08F ₁₆ |
| 7 | 090 ₁₆ | 091 ₁₆ | 092 ₁₆ | 093 ₁₆ | 094 ₁₆ | 095 ₁₆ | 096 ₁₆ | 097 ₁₆ | 098 ₁₆ | 099 ₁₆ | 09A ₁₆ | 09B ₁₆ | 09C ₁₆ | 09D ₁₆ | 09E ₁₆ | 09F ₁₆ | 0A0 ₁₆ | 0A1 ₁₆ | 0A2 ₁₆ | 0A3 ₁₆ | 0A4 ₁₆ | 0A5 ₁₆ | 0A6 ₁₆ | 0A7 ₁₆ |
| 8 | 0A8 ₁₆ | 0A9 ₁₆ | 0AA ₁₆ | 0AB ₁₆ | 0AC ₁₆ | 0AD ₁₆ | 0AE ₁₆ | 0AF ₁₆ | 0B0 ₁₆ | 0B1 ₁₆ | 0B2 ₁₆ | 0B3 ₁₆ | 0B4 ₁₆ | 0B5 ₁₆ | 0B6 ₁₆ | 0B7 ₁₆ | 0B8 ₁₆ | 0B9 ₁₆ | 0BA ₁₆ | 0BB ₁₆ | 0BC ₁₆ | 0BD ₁₆ | 0BE ₁₆ | 0BF ₁₆ |
| 9 | 0C0 ₁₆ | 0C1 ₁₆ | 0C2 ₁₆ | 0C3 ₁₆ | 0C4 ₁₆ | 0C5 ₁₆ | 0C6 ₁₆ | 0C7 ₁₆ | 0C8 ₁₆ | 0C9 ₁₆ | 0CA ₁₆ | 0CB ₁₆ | 0CC ₁₆ | 0CD ₁₆ | 0CE ₁₆ | 0CF ₁₆ | 0D0 ₁₆ | 0D1 ₁₆ | 0D2 ₁₆ | 0D3 ₁₆ | 0D4 ₁₆ | 0D5 ₁₆ | 0D6 ₁₆ | 0D7 ₁₆ |
| 10 | 0D8 ₁₆ | 0D9 ₁₆ | 0DA ₁₆ | 0DB ₁₆ | 0DC ₁₆ | 0DD ₁₆ | 0DE ₁₆ | 0DF ₁₆ | 0E0 ₁₆ | 0E1 ₁₆ | 0E2 ₁₆ | 0E3 ₁₆ | 0E4 ₁₆ | 0E5 ₁₆ | 0E6 ₁₆ | 0E7 ₁₆ | 0E8 ₁₆ | 0E9 ₁₆ | 0EA ₁₆ | 0EB ₁₆ | 0EC ₁₆ | 0ED ₁₆ | 0EE ₁₆ | 0EF ₁₆ |
| 11 | 0F0 ₁₆ | 0F1 ₁₆ | 0F2 ₁₆ | 0F3 ₁₆ | 0F4 ₁₆ | 0F5 ₁₆ | 0F6 ₁₆ | 0F7 ₁₆ | 0F8 ₁₆ | 0F9 ₁₆ | 0FA ₁₆ | 0FB ₁₆ | 0FC ₁₆ | 0FD ₁₆ | 0FE ₁₆ | 0FF ₁₆ | 100 ₁₆ | 101 ₁₆ | 102 ₁₆ | 103 ₁₆ | 104 ₁₆ | 105 ₁₆ | 106 ₁₆ | 107 ₁₆ |
| 12 | 108 ₁₆ | 109 ₁₆ | 10A ₁₆ | 10B ₁₆ | 10C ₁₆ | 10D ₁₆ | 10E ₁₆ | 10F ₁₆ | 110 ₁₆ | 111 ₁₆ | 112 ₁₆ | 113 ₁₆ | 114 ₁₆ | 115 ₁₆ | 116 ₁₆ | 117 ₁₆ | 118 ₁₆ | 119 ₁₆ | 11A ₁₆ | 11B ₁₆ | 11C ₁₆ | 11D ₁₆ | 11E ₁₆ | 11F ₁₆ |

f The hexadecimal numbers in the boxes show the display RAM address.

Fig. 2 Screen constitution

REGISTERS DESCRIPTION

(1) Address 120₁₆

| DA | Register | Contents | | Remarks | | | | | | | | | | | | | | | | | | | |
|----|---|-------------|---|---|---|---|--|-------------------------------------|-------------------------------------|-------------------------------------|---|---|-------------|------------|---|------------|-------------|---|------------|---|---|-------------|---|
| | | Status | Function | | | | | | | | | | | | | | | | | | | | |
| 0 | DIV0 | 0 | Set external clock frequency value of horizontal oscillation frequency. | Set display frequency by frequency value setting. Set N1 to be "N1=fosc/fH". fosc(MHz) : External clock frequency for TCK pin (=display frequency) fH(kHz) : Horizontal synchronous signal frequency for HOR pin Set registers DIVS0, DIVS1 (address 120 ₁₆), RSEL0 (address 121 ₁₆) and RSEL1 (address 122 ₁₆) according to external clock frequency. For details, see (2) Setting display frequencies under Register Supplementary Description. Any of this settings above is required only when EXCK1=1, EXCK0=1. | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | |
| 1 | DIV1 | 0 | $N1 = \sum_{n=0}^{10} (DIVn \times 2^n)$ N1: frequency value | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | |
| 2 | DIV2 | 0 | | | Horizontal synchronized signal  | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | |
| 3 | DIV3 | 0 | | | | External clock Clock number (N1) | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | |
| 4 | DIV4 | 0 | | | | | Horizontal synchronized signal External clock Clock number (N1) | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | |
| 5 | DIV5 | 0 | | | | | | External clock Clock number (N1) | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | |
| 6 | DIV6 | 0 | | | | | | | External clock Clock number (N1) | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | |
| 7 | DIV7 | 0 | | | | | | | | External clock Clock number (N1) | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | |
| 8 | DIV8 | 0 | | External clock Clock number (N1) | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | |
| 9 | DIV9 | 0 | External clock Clock number (N1) | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | |
| A | DIV10 | 0 | | | External clock Clock number (N1) | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | |
| B | DIVS0 | 0 | | | | For details, see (2) Setting display frequencies under Register Supplementary Description. | | | | | Set display frequency area. | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | |
| C | DIVS1 | 0 | | | | | For details, see (2) Setting display frequencies under Register Supplementary Description. | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | |
| D | VJT | 0 | | | | It should be fixed to "0". | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | Alleviates continuous vertical jitters. | | | | | | | | | | | | |
| E | EXCK0 | 0 | | | | <table border="1" data-bbox="467 1654 771 1780"> <thead> <tr> <th>EXCK1</th> <th>EXCK0</th> <th>Display clock input</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>20 to 30MHz</td> </tr> <tr> <td>0</td> <td>1</td> <td>Do not set</td> </tr> <tr> <td>1</td> <td>0</td> <td>Do not set</td> </tr> <tr> <td>1</td> <td>1</td> <td>20 to 80MHz</td> </tr> </tbody> </table> | EXCK1 | EXCK0 | Display clock input | | 0 | 0 | 20 to 30MHz | 0 | 1 | Do not set | 1 | 0 | Do not set | 1 | 1 | 20 to 80MHz | See setting External Clock Input Mode (to be input from the TCK terminal). EXCK1 : address 123 ₁₆ |
| | | | | | | EXCK1 | EXCK0 | Display clock input | | | | | | | | | | | | | | | |
| | | 0 | | | | 0 | 20 to 30MHz | | | | | | | | | | | | | | | | |
| | | 0 | | | | 1 | Do not set | | | | | | | | | | | | | | | | |
| 1 | 0 | Do not set | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 20 to 80MHz | | | | | | | | | | | | | | | | | | | | | |
| 1 | <table border="1" data-bbox="467 1654 771 1780"> <thead> <tr> <th>EXCK1</th> <th>EXCK0</th> <th>Display clock input</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>20 to 30MHz</td> </tr> <tr> <td>0</td> <td>1</td> <td>Do not set</td> </tr> <tr> <td>1</td> <td>0</td> <td>Do not set</td> </tr> <tr> <td>1</td> <td>1</td> <td>20 to 80MHz</td> </tr> </tbody> </table> | EXCK1 | EXCK0 | Display clock input | | 0 | 0 | 20 to 30MHz | 0 | 1 | Do not set | 1 | 0 | Do not set | 1 | 1 | 20 to 80MHz | | | | | | |
| | EXCK1 | EXCK0 | Display clock input | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 20 to 30MHz | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | Do not set | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | Do not set | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 20 to 80MHz | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | |

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(2) Address 121₁₆

| DA | Register | Contents | | Remarks |
|----|----------------|----------|--|---|
| | | Status | Function | |
| 0 | PTC0 | 0 | P0 output (port P0). Port data is set by PTD0. | BLNK0 outputs blanking signal. Blanking status is determined by BLK0, BLK1, and DSP0 to DSP11 settings. |
| | | 1 | BLNK0 output. Polarity is set by PTD0. | |
| 1 | PTC1 | 0 | P1 output (port P1). Port data is set by PTD1. | |
| | | 1 | R signal output. Polarity is set by PTD1. | |
| 2 | PTC2 | 0 | P2 output (port P2). Port data is set by PTD2. | |
| | | 1 | Can not be used. | |
| 3 | PTC3 | 0 | P3 output (port P3). Port data is set by PTD3. | |
| | | 1 | G signal output. Polarity is set by PTD3. | |
| 4 | PTC4 | 0 | P4 output (port P4). Port data is set by PTD4. | |
| | | 1 | Can not be used. | |
| 5 | PTC5 | 0 | P5 output (port P5). Port data is set by PTD5. | |
| | | 1 | B signal output. Polarity is set by PTD5. | |
| 6 | PTD0 (Note) | 0 | "L" output (P0 output) or negative polarity output (BLNK0 output). | P0 pin data control. |
| | | 1 | "H" output (P0 output) or positive polarity output (BLNK0 output). | |
| 7 | PTD1 (Note) | 0 | "L" output (P1 output) or negative polarity output (R signal output). | P1 pin data control. |
| | | 1 | "H" output (P1 output) or positive polarity output (R signal output). | |
| 8 | PTD2 (Note) | 0 | "L" output (P2 output). | P2 pin exclusive port output state control. |
| | | 1 | "H" output (P2 output). | |
| 9 | PTD3 (Note) | 0 | "L" output (P3 output) or negative polarity output (G signal output). | P3 pin data control. |
| | | 1 | "H" output (P3 output) or positive polarity output (G signal output). | |
| A | PTD4 (Note) | 0 | "L" output (P2 output). | P4 pin exclusive port output state control. |
| | | 1 | "H" output (P2 output). | |
| B | PTD5 (Note) | 0 | "L" output (P5 output) or negative polarity output (B signal output). | P5 pin data control. |
| | | 1 | "H" output (P5 output) or positive polarity output (B signal output). | |
| C | PTD6 (Note) | 0 | "L" output (P6 output). | P6 pin exclusive port output state control. |
| | | 1 | "H" output (P6 output). | |
| D | PTD7 (Note) | 0 | "L" output (P7 output). | P7 pin exclusive port output state control. |
| | | 1 | "H" output (P7 output). | |
| E | RSEL0 | 0 | For details, see (2) Setting display frequencies under Register Supplementary Description. | Set display frequency area. |
| | | 1 | To be used when EXCK0=1 and EXCK1=1. | |

Note. To determined this register, input clock (at least one clock) to the external clock pin (TCK).

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(3) Address 122₁₆

| DA | Register | Contents | | Remarks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----|-----------|----------|---|--|---|--|---|---|---|---|---|---|---|----|---|---|---|------------|---|---|---|-----------|---|---|---|-----------|---|---|---|-----------|---|---|---|-----------|---|---|---|-------|---|---|---|---------|
| | | Status | Function | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | HP0 (LSB) | 0 | If HS is the horizontal display start location, | Horizontal display start location is specified using the 10 bits from HP9 to HP0. HP9 to HP0 = (0000000002) and (00000101112) setting is forbidden. Note : In case of B/F register is "0". | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | $HS = T \times \sum_{n=0}^9 2^n HP_n + 6$ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | HP1 | 0 | T: The cycle of display frequency | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | 1000 settings are possible. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | HP2 | 0 | <p>HOR (Note)</p> <p>VP</p> <p>HP</p> <p>Display area</p> <p>VERT</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | HP3 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | HP4 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | HP5 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 6 | HP6 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 7 | HP7 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 8 | HP8 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 9 | HP9 (MSB) | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | TEST9 | 0 | It should be fixed to "0". | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | Can not be used. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | SPACE0 | 0 | <table border="1"> <thead> <tr> <th colspan="3">SPACE</th> <th rowspan="2">Number of Lines and Space (⊕ represents space)</th> </tr> <tr> <th>2</th> <th>1</th> <th>0</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>12</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1 ⊕ 10 1</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>2 ⊕ 8 2</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>3 ⊕ 6 3</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>4 ⊕ 4 4</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>5 ⊕ 2 5</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>6 ⊕ 6</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>6 ⊕ 6</td> </tr> </tbody> </table> <p>⊕ represents one line worth of spaces.</p> | SPACE | | | Number of Lines and Space (⊕ represents space) | 2 | 1 | 0 | 0 | 0 | 0 | 12 | 0 | 0 | 1 | 1 ⊕ 10 1 | 0 | 1 | 0 | 2 ⊕ 8 2 | 0 | 1 | 1 | 3 ⊕ 6 3 | 1 | 0 | 0 | 4 ⊕ 4 4 | 1 | 0 | 1 | 5 ⊕ 2 5 | 1 | 1 | 0 | 6 ⊕ 6 | 1 | 1 | 1 | 6 ⊕ 6 |
| | | SPACE | | | Number of Lines and Space (⊕ represents space) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | 1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | | 12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | | 1 ⊕ 10 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | | 2 ⊕ 8 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | | 3 ⊕ 6 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | | 4 ⊕ 4 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | | 5 ⊕ 2 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | | 6 ⊕ 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 6 ⊕ 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | SPACE1 | 0 | Leave one line worth of space in the vertical direction. For example, 6 ⊕ 6 indicates two sets of 6 lines with a line of spaces between lines 6 and 7. A line is 18 × N horizontal scan lines. N is determined by the character size in the vertical direction as follows: ×1 ... N = 1 ×2 ... N = 2 ×3 ... N = 3 ×4 ... N = 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | SPACE2 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RSEL1 | 0 | | For details, see (2) Setting display frequencies under Register Supplementary Description. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | To be used when EXCK0=1 and EXCK1=1. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(4) Address 123₁₆

| DA | Register | Contents | | Remarks |
|----|-----------|----------|---|---|
| | | Status | Function | |
| 0 | VP0 (LSB) | 0 | If VS is the vertical display start location, | The vertical start location is specified using the 10 bits from VP9 to VP0. VP9 to VP0 = (0000000000 ₂) setting is forbidden. Note : In case of B/F register is "0". |
| | | 1 | $VS = H \times \sum_{n=0}^9 2^n VP_n$ | |
| 1 | VP1 | 0 | H: Cycle with the horizontal synchronizing pulse | |
| | | 1 | 1023 settings are possible. | |
| 2 | VP2 | 0 | | |
| | | 1 | | |
| 3 | VP3 | 0 | | |
| | | 1 | | |
| 4 | VP4 | 0 | | |
| | | 1 | | |
| 5 | VP5 | 0 | | |
| | | 1 | | |
| 6 | VP6 | 0 | | |
| | | 1 | | |
| 7 | VP7 | 0 | | |
| | | 1 | | |
| 8 | VP8 | 0 | | |
| | | 1 | | |
| 9 | VP9 (MSB) | 0 | | |
| | | 1 | | |
| A | TEST0 | 0 | It should be fixed to "0". | |
| | | 1 | Can not be used. | |
| B | TEST1 | 0 | It should be fixed to "0". | |
| | | 1 | Can not be used. | |
| C | TEST2 | 0 | It should be fixed to "0". | |
| | | 1 | Can not be used. | |
| D | TEST3 | 0 | It should be fixed to "0". | |
| | | 1 | Can not be used. | |
| E | EXCK1 | 0 | For setting. See Register EXCK0 (address 120 ₁₆). | Sets input mode of external clock (input from TCK pin). |
| | | 1 | | |

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(5) Address 124₁₆

| DA | Register | Contents | | Remarks |
|----|----------|----------|---|-----------------------------------|
| | | Status | Function | |
| 0 | DSP0 | 0 | Blanking is in the display mode specified by BLK0 and BLK1. (Note) | Sets the display mode of line 1. |
| | | 1 | Blanking is in the display mode specified by except BLK0 and BLK1. (Note) | |
| 1 | DSP1 | 0 | Blanking is in the display mode specified by BLK0 and BLK1. (Note) | Sets the display mode of line 2. |
| | | 1 | Blanking is in the display mode specified by except BLK0 and BLK1. (Note) | |
| 2 | DSP2 | 0 | Blanking is in the display mode specified by BLK0 and BLK1. (Note) | Sets the display mode of line 3. |
| | | 1 | Blanking is in the display mode specified by except BLK0 and BLK1. (Note) | |
| 3 | DSP3 | 0 | Blanking is in the display mode specified by BLK0 and BLK1. (Note) | Sets the display mode of line 4. |
| | | 1 | Blanking is in the display mode specified by except BLK0 and BLK1. (Note) | |
| 4 | DSP4 | 0 | Blanking is in the display mode specified by BLK0 and BLK1. (Note) | Sets the display mode of line 5. |
| | | 1 | Blanking is in the display mode specified by except BLK0 and BLK1. (Note) | |
| 5 | DSP5 | 0 | Blanking is in the display mode specified by BLK0 and BLK1. (Note) | Sets the display mode of line 6. |
| | | 1 | Blanking is in the display mode specified by except BLK0 and BLK1. (Note) | |
| 6 | DSP6 | 0 | Blanking is in the display mode specified by BLK0 and BLK1. (Note) | Sets the display mode of line 7. |
| | | 1 | Blanking is in the display mode specified by except BLK0 and BLK1. (Note) | |
| 7 | DSP7 | 0 | Blanking is in the display mode specified by BLK0 and BLK1. (Note) | Sets the display mode of line 8. |
| | | 1 | Blanking is in the display mode specified by except BLK0 and BLK1. (Note) | |
| 8 | DSP8 | 0 | Blanking is in the display mode specified by BLK0 and BLK1. (Note) | Sets the display mode of line 9. |
| | | 1 | Blanking is in the display mode specified by except BLK0 and BLK1. (Note) | |
| 9 | DSP9 | 0 | Blanking is in the display mode specified by BLK0 and BLK1. (Note) | Sets the display mode of line 10. |
| | | 1 | Blanking is in the display mode specified by except BLK0 and BLK1. (Note) | |
| A | DSP10 | 0 | Blanking is in the display mode specified by BLK0 and BLK1. (Note) | Sets the display mode of line 11. |
| | | 1 | Blanking is in the display mode specified by except BLK0 and BLK1. (Note) | |
| B | DSP11 | 0 | Blanking is in the display mode specified by BLK0 and BLK1. (Note) | Sets the display mode of line 12. |
| | | 1 | Blanking is in the display mode specified by except BLK0 and BLK1. (Note) | |
| C | TEST4 | 0 | It should be fixed to "0". | |
| | | 1 | Can not be used. | |
| D | TEST5 | 0 | It should be fixed to "0". | |
| | | 1 | Can not be used. | |
| E | TEST14 | 0 | Can not be used. | |
| | | 1 | It should be fixed to "1". | |

Note: Refer to DISPLAY FORM1.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(6) Address 125₁₆

| DA | Register | Contents | | Remarks | | | | | | | | | | | | | | | |
|--------|---|-------------------------|---|---|--------|-------------------------|-------------------------|---|--------|--------|---|--------|--------|---|--------|--------|---|--------|--------|
| | | Status | Function | | | | | | | | | | | | | | | | |
| 0 | LIN2 | 0 | The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 2nd line. | | | | | | | | | | | | | | | |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1. | | | | | | | | | | | | | | | | |
| 1 | LIN3 | 0 | The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 3rd line. | | | | | | | | | | | | | | | |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1. | | | | | | | | | | | | | | | | |
| 2 | LIN4 | 0 | The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 4th line. | | | | | | | | | | | | | | | |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1. | | | | | | | | | | | | | | | | |
| 3 | LIN5 | 0 | The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 5th line. | | | | | | | | | | | | | | | |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1. | | | | | | | | | | | | | | | | |
| 4 | LIN6 | 0 | The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 6th line. | | | | | | | | | | | | | | | |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1. | | | | | | | | | | | | | | | | |
| 5 | LIN7 | 0 | The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 7th line. | | | | | | | | | | | | | | | |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1. | | | | | | | | | | | | | | | | |
| 6 | LIN8 | 0 | The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 8th line. | | | | | | | | | | | | | | | |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1. | | | | | | | | | | | | | | | | |
| 7 | LIN9 | 0 | The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 9th line. | | | | | | | | | | | | | | | |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1. | | | | | | | | | | | | | | | | |
| 8 | V1SZ0 | 0 | H: Cycle with the horizontal synchronizing pulse | Character size setting in the vertical direction for the 1st line. (display monitor 1 to 12 line) | | | | | | | | | | | | | | | |
| | | 1 | <table border="1"> <thead> <tr> <th>V1SZ1</th> <th>V1SZ0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table> | | V1SZ1 | V1SZ0 | Vertical direction size | 0 | 0 | 1H/dot | 0 | 1 | 2H/dot | 1 | 0 | 3H/dot | 1 | 1 | 4H/dot |
| V1SZ1 | V1SZ0 | Vertical direction size | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1H/dot | | | | | | | | | | | | | | | | | |
| 0 | 1 | 2H/dot | | | | | | | | | | | | | | | | | |
| 1 | 0 | 3H/dot | | | | | | | | | | | | | | | | | |
| 1 | 1 | 4H/dot | | | | | | | | | | | | | | | | | |
| 9 | V1SZ1 | 0 | <table border="1"> <thead> <tr> <th>V1SZ1</th> <th>V1SZ0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table> | V1SZ1 | V1SZ0 | Vertical direction size | 0 | 0 | 1H/dot | 0 | 1 | 2H/dot | 1 | 0 | 3H/dot | 1 | 1 | 4H/dot | |
| | | V1SZ1 | V1SZ0 | Vertical direction size | | | | | | | | | | | | | | | |
| 0 | 0 | 1H/dot | | | | | | | | | | | | | | | | | |
| 0 | 1 | 2H/dot | | | | | | | | | | | | | | | | | |
| 1 | 0 | 3H/dot | | | | | | | | | | | | | | | | | |
| 1 | 1 | 4H/dot | | | | | | | | | | | | | | | | | |
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| V1SZ1 | V1SZ0 | Vertical direction size | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1H/dot | | | | | | | | | | | | | | | | | |
| 0 | 1 | 2H/dot | | | | | | | | | | | | | | | | | |
| 1 | 0 | 3H/dot | | | | | | | | | | | | | | | | | |
| 1 | 1 | 4H/dot | | | | | | | | | | | | | | | | | |
| A | VSZ1L0 | 0 | H: Cycle with the horizontal synchronizing pulse | Character size setting in the vertical direction (display monitor 1 line) at "0" state in register LIN2 to LIN17. | | | | | | | | | | | | | | | |
| | | 1 | <table border="1"> <thead> <tr> <th>VSZ1L1</th> <th>VSZ1L0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table> | | VSZ1L1 | VSZ1L0 | Vertical direction size | 0 | 0 | 1H/dot | 0 | 1 | 2H/dot | 1 | 0 | 3H/dot | 1 | 1 | 4H/dot |
| VSZ1L1 | VSZ1L0 | Vertical direction size | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1H/dot | | | | | | | | | | | | | | | | | |
| 0 | 1 | 2H/dot | | | | | | | | | | | | | | | | | |
| 1 | 0 | 3H/dot | | | | | | | | | | | | | | | | | |
| 1 | 1 | 4H/dot | | | | | | | | | | | | | | | | | |
| B | VSZ1L1 | 0 | <table border="1"> <thead> <tr> <th>VSZ1L1</th> <th>VSZ1L0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table> | VSZ1L1 | VSZ1L0 | Vertical direction size | 0 | 0 | 1H/dot | 0 | 1 | 2H/dot | 1 | 0 | 3H/dot | 1 | 1 | 4H/dot | |
| | | VSZ1L1 | VSZ1L0 | Vertical direction size | | | | | | | | | | | | | | | |
| 0 | 0 | 1H/dot | | | | | | | | | | | | | | | | | |
| 0 | 1 | 2H/dot | | | | | | | | | | | | | | | | | |
| 1 | 0 | 3H/dot | | | | | | | | | | | | | | | | | |
| 1 | 1 | 4H/dot | | | | | | | | | | | | | | | | | |
| 1 | <table border="1"> <thead> <tr> <th>VSZ1L1</th> <th>VSZ1L0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table> | VSZ1L1 | VSZ1L0 | Vertical direction size | 0 | 0 | 1H/dot | 0 | 1 | 2H/dot | 1 | 0 | 3H/dot | 1 | 1 | 4H/dot | | | |
| VSZ1L1 | VSZ1L0 | Vertical direction size | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1H/dot | | | | | | | | | | | | | | | | | |
| 0 | 1 | 2H/dot | | | | | | | | | | | | | | | | | |
| 1 | 0 | 3H/dot | | | | | | | | | | | | | | | | | |
| 1 | 1 | 4H/dot | | | | | | | | | | | | | | | | | |
| C | VSZ1H0 | 0 | H: Cycle with the horizontal synchronizing pulse | Character size setting in the vertical direction (display monitor 1 line) at "1" state in register LIN2 to LIN17. | | | | | | | | | | | | | | | |
| | | 1 | <table border="1"> <thead> <tr> <th>VSZ1H1</th> <th>VSZ1H0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table> | | VSZ1H1 | VSZ1H0 | Vertical direction size | 0 | 0 | 1H/dot | 0 | 1 | 2H/dot | 1 | 0 | 3H/dot | 1 | 1 | 4H/dot |
| VSZ1H1 | VSZ1H0 | Vertical direction size | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1H/dot | | | | | | | | | | | | | | | | | |
| 0 | 1 | 2H/dot | | | | | | | | | | | | | | | | | |
| 1 | 0 | 3H/dot | | | | | | | | | | | | | | | | | |
| 1 | 1 | 4H/dot | | | | | | | | | | | | | | | | | |
| D | VSZ1H1 | 0 | <table border="1"> <thead> <tr> <th>VSZ1H1</th> <th>VSZ1H0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table> | VSZ1H1 | VSZ1H0 | Vertical direction size | 0 | 0 | 1H/dot | 0 | 1 | 2H/dot | 1 | 0 | 3H/dot | 1 | 1 | 4H/dot | |
| | | VSZ1H1 | VSZ1H0 | Vertical direction size | | | | | | | | | | | | | | | |
| 0 | 0 | 1H/dot | | | | | | | | | | | | | | | | | |
| 0 | 1 | 2H/dot | | | | | | | | | | | | | | | | | |
| 1 | 0 | 3H/dot | | | | | | | | | | | | | | | | | |
| 1 | 1 | 4H/dot | | | | | | | | | | | | | | | | | |
| 1 | <table border="1"> <thead> <tr> <th>VSZ1H1</th> <th>VSZ1H0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table> | VSZ1H1 | VSZ1H0 | Vertical direction size | 0 | 0 | 1H/dot | 0 | 1 | 2H/dot | 1 | 0 | 3H/dot | 1 | 1 | 4H/dot | | | |
| VSZ1H1 | VSZ1H0 | Vertical direction size | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1H/dot | | | | | | | | | | | | | | | | | |
| 0 | 1 | 2H/dot | | | | | | | | | | | | | | | | | |
| 1 | 0 | 3H/dot | | | | | | | | | | | | | | | | | |
| 1 | 1 | 4H/dot | | | | | | | | | | | | | | | | | |
| E | TEST10 | 0 | It should be fixed to "0". | | | | | | | | | | | | | | | | |
| | | 1 | Test mode | | | | | | | | | | | | | | | | |

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(7) Address 126₁₆

| DA | Register | Contents | | Remarks | | | | | | | | | | | | | | | |
|--------|---|-------------------------|---|---|--------|-------------------------|-------------------------|---|--------|--------|---|--------|--------|---|--------|--------|---|--------|--------|
| | | Status | Function | | | | | | | | | | | | | | | | |
| 0 | LIN10 | 0 | The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 10th line. | | | | | | | | | | | | | | | |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1. | | | | | | | | | | | | | | | | |
| 1 | LIN11 | 0 | The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 11th line. | | | | | | | | | | | | | | | |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1. | | | | | | | | | | | | | | | | |
| 2 | LIN12 | 0 | The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 12th line. | | | | | | | | | | | | | | | |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1. | | | | | | | | | | | | | | | | |
| 3 | LIN13 | 0 | The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 13th line. | | | | | | | | | | | | | | | |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1. | | | | | | | | | | | | | | | | |
| 4 | LIN14 | 0 | The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 14th line. | | | | | | | | | | | | | | | |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1. | | | | | | | | | | | | | | | | |
| 5 | LIN15 | 0 | The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 15th line. | | | | | | | | | | | | | | | |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1. | | | | | | | | | | | | | | | | |
| 6 | LIN16 | 0 | The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 16th line. | | | | | | | | | | | | | | | |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1. | | | | | | | | | | | | | | | | |
| 7 | LIN17 | 0 | The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 17th line. | | | | | | | | | | | | | | | |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1. | | | | | | | | | | | | | | | | |
| 8 | V18SZ0 | 0 | H: Cycle with the horizontal synchronizing pulse | Character size setting in the vertical direction for the 18th line. (display monitor 1 to 12 line) | | | | | | | | | | | | | | | |
| | | 1 | <table border="1"> <thead> <tr> <th>V18SZ1</th> <th>V18SZ0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table> | | V18SZ1 | V18SZ0 | Vertical direction size | 0 | 0 | 1H/dot | 0 | 1 | 2H/dot | 1 | 0 | 3H/dot | 1 | 1 | 4H/dot |
| V18SZ1 | V18SZ0 | Vertical direction size | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1H/dot | | | | | | | | | | | | | | | | | |
| 0 | 1 | 2H/dot | | | | | | | | | | | | | | | | | |
| 1 | 0 | 3H/dot | | | | | | | | | | | | | | | | | |
| 1 | 1 | 4H/dot | | | | | | | | | | | | | | | | | |
| 9 | V18SZ1 | 0 | <table border="1"> <thead> <tr> <th>V18SZ1</th> <th>V18SZ0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table> | V18SZ1 | V18SZ0 | Vertical direction size | 0 | 0 | 1H/dot | 0 | 1 | 2H/dot | 1 | 0 | 3H/dot | 1 | 1 | 4H/dot | |
| | | V18SZ1 | V18SZ0 | Vertical direction size | | | | | | | | | | | | | | | |
| 0 | 0 | 1H/dot | | | | | | | | | | | | | | | | | |
| 0 | 1 | 2H/dot | | | | | | | | | | | | | | | | | |
| 1 | 0 | 3H/dot | | | | | | | | | | | | | | | | | |
| 1 | 1 | 4H/dot | | | | | | | | | | | | | | | | | |
| 1 | <table border="1"> <thead> <tr> <th>V18SZ1</th> <th>V18SZ0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table> | V18SZ1 | V18SZ0 | Vertical direction size | 0 | 0 | 1H/dot | 0 | 1 | 2H/dot | 1 | 0 | 3H/dot | 1 | 1 | 4H/dot | | | |
| V18SZ1 | V18SZ0 | Vertical direction size | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1H/dot | | | | | | | | | | | | | | | | | |
| 0 | 1 | 2H/dot | | | | | | | | | | | | | | | | | |
| 1 | 0 | 3H/dot | | | | | | | | | | | | | | | | | |
| 1 | 1 | 4H/dot | | | | | | | | | | | | | | | | | |
| A | VSZ2L0 | 0 | H: Cycle with the horizontal synchronizing pulse | Character size setting in the vertical direction (display monitor for 2 to 12 line) at "0" state in register LIN2 to LIN17. | | | | | | | | | | | | | | | |
| | | 1 | <table border="1"> <thead> <tr> <th>VSZ2L1</th> <th>VSZ2L0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table> | | VSZ2L1 | VSZ2L0 | Vertical direction size | 0 | 0 | 1H/dot | 0 | 1 | 2H/dot | 1 | 0 | 3H/dot | 1 | 1 | 4H/dot |
| VSZ2L1 | VSZ2L0 | Vertical direction size | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1H/dot | | | | | | | | | | | | | | | | | |
| 0 | 1 | 2H/dot | | | | | | | | | | | | | | | | | |
| 1 | 0 | 3H/dot | | | | | | | | | | | | | | | | | |
| 1 | 1 | 4H/dot | | | | | | | | | | | | | | | | | |
| B | VSZ2L1 | 0 | <table border="1"> <thead> <tr> <th>VSZ2L1</th> <th>VSZ2L0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table> | VSZ2L1 | VSZ2L0 | Vertical direction size | 0 | 0 | 1H/dot | 0 | 1 | 2H/dot | 1 | 0 | 3H/dot | 1 | 1 | 4H/dot | |
| | | VSZ2L1 | VSZ2L0 | Vertical direction size | | | | | | | | | | | | | | | |
| 0 | 0 | 1H/dot | | | | | | | | | | | | | | | | | |
| 0 | 1 | 2H/dot | | | | | | | | | | | | | | | | | |
| 1 | 0 | 3H/dot | | | | | | | | | | | | | | | | | |
| 1 | 1 | 4H/dot | | | | | | | | | | | | | | | | | |
| 1 | <table border="1"> <thead> <tr> <th>VSZ2L1</th> <th>VSZ2L0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table> | VSZ2L1 | VSZ2L0 | Vertical direction size | 0 | 0 | 1H/dot | 0 | 1 | 2H/dot | 1 | 0 | 3H/dot | 1 | 1 | 4H/dot | | | |
| VSZ2L1 | VSZ2L0 | Vertical direction size | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1H/dot | | | | | | | | | | | | | | | | | |
| 0 | 1 | 2H/dot | | | | | | | | | | | | | | | | | |
| 1 | 0 | 3H/dot | | | | | | | | | | | | | | | | | |
| 1 | 1 | 4H/dot | | | | | | | | | | | | | | | | | |
| C | VSZ2H0 | 0 | H: Cycle with the horizontal synchronizing pulse | Character size setting in the vertical direction (display monitor for 2 to 12 line) at "1" state in register LIN2 to LIN17. | | | | | | | | | | | | | | | |
| | | 1 | <table border="1"> <thead> <tr> <th>VSZ2H1</th> <th>VSZ2H0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table> | | VSZ2H1 | VSZ2H0 | Vertical direction size | 0 | 0 | 1H/dot | 0 | 1 | 2H/dot | 1 | 0 | 3H/dot | 1 | 1 | 4H/dot |
| VSZ2H1 | VSZ2H0 | Vertical direction size | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1H/dot | | | | | | | | | | | | | | | | | |
| 0 | 1 | 2H/dot | | | | | | | | | | | | | | | | | |
| 1 | 0 | 3H/dot | | | | | | | | | | | | | | | | | |
| 1 | 1 | 4H/dot | | | | | | | | | | | | | | | | | |
| D | VSZ2H1 | 0 | <table border="1"> <thead> <tr> <th>VSZ2H1</th> <th>VSZ2H0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table> | VSZ2H1 | VSZ2H0 | Vertical direction size | 0 | 0 | 1H/dot | 0 | 1 | 2H/dot | 1 | 0 | 3H/dot | 1 | 1 | 4H/dot | |
| | | VSZ2H1 | VSZ2H0 | Vertical direction size | | | | | | | | | | | | | | | |
| 0 | 0 | 1H/dot | | | | | | | | | | | | | | | | | |
| 0 | 1 | 2H/dot | | | | | | | | | | | | | | | | | |
| 1 | 0 | 3H/dot | | | | | | | | | | | | | | | | | |
| 1 | 1 | 4H/dot | | | | | | | | | | | | | | | | | |
| 1 | <table border="1"> <thead> <tr> <th>VSZ2H1</th> <th>VSZ2H0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table> | VSZ2H1 | VSZ2H0 | Vertical direction size | 0 | 0 | 1H/dot | 0 | 1 | 2H/dot | 1 | 0 | 3H/dot | 1 | 1 | 4H/dot | | | |
| VSZ2H1 | VSZ2H0 | Vertical direction size | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1H/dot | | | | | | | | | | | | | | | | | |
| 0 | 1 | 2H/dot | | | | | | | | | | | | | | | | | |
| 1 | 0 | 3H/dot | | | | | | | | | | | | | | | | | |
| 1 | 1 | 4H/dot | | | | | | | | | | | | | | | | | |
| E | TEST11 | 0 | It should be fixed to "0". | | | | | | | | | | | | | | | | |
| | | 1 | Test mode | | | | | | | | | | | | | | | | |

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(8) Address 127₁₆

| DA | Register | Contents | | | | Remarks | |
|----|----------|----------|--------------------------------------|-------|---------------------------|---|----------------------------------|
| | | Status | Function | | | | |
| 0 | RR | 0 | RB | RG | RR | Color | Sets the color of all blankings. |
| | | 1 | 0 | 0 | 0 | Black | |
| 1 | RG | 0 | 0 | 0 | 1 | Red | |
| | | 1 | 0 | 1 | 0 | Green | |
| 2 | RB | 0 | 0 | 1 | 1 | Yellow | |
| | | 1 | 1 | 0 | 0 | Blue | |
| 3 | FR | 0 | 1 | 0 | 1 | Magenta | |
| | | 1 | 1 | 1 | 0 | Cyan | |
| 4 | FG | 0 | 1 | 1 | 1 | White | |
| | | 1 | | | | | |
| 5 | FB | 0 | | | | | |
| | | 1 | | | | | |
| 6 | TEST6 | 0 | It should be fixed to "0". | | | | |
| | | 1 | Can not be used. | | | | |
| 7 | TEST7 | 0 | It should be fixed to "0". | | | | |
| | | 1 | Can not be used. | | | | |
| 8 | TEST8 | 0 | It should be fixed to "0". | | | | |
| | | 1 | Can not be used. | | | | |
| 9 | BETA14 | 0 | Matrix-outline display (12 × 18 dot) | | | Set this register to the character font set by display RAM BR, BG and BB. | |
| | | 1 | Matrix-outline display (14 × 18 dot) | | | | |
| A | HSZ10 | 0 | T: Display frequency cycle | | | Character size setting in the horizontal direction for the first line. | |
| | | 1 | HSZ11 | HSZ10 | Horizontal direction size | | |
| B | HSZ11 | 0 | 0 | 0 | 1T/dot | | |
| | | 1 | 0 | 1 | 2T/dot | | |
| C | HSZ20 | 0 | 1 | 0 | 3T/dot | | |
| | | 1 | 1 | 1 | 4T/dot | | |
| D | HSZ21 | 0 | T: Display frequency cycle | | | | |
| | | 1 | VSZ21 | HSZ20 | Horizontal direction size | | |
| E | TEST12 | 0 | 0 | 0 | 1T/dot | | |
| | | 1 | 0 | 1 | 2T/dot | | |
| | | 0 | 1 | 0 | 3T/dot | | |
| | | 1 | 1 | 1 | 4T/dot | | |
| | | 0 | It should be fixed to "0". | | | | |
| | | 1 | Test mode | | | | |

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(9) Address 128₁₆

| DA | Register | Contents | | Remarks | | | | | | | | | | | | | | | | | | |
|-----|----------|---------------------|--|--|--|---------------|---|---|--|---|---|---------------------|---|---|----------------|---|---|-------------|---|---|---------------------|--|
| | | Status | Function | | | | | | | | | | | | | | | | | | | |
| 0 | BCOL | 0 | Blanking of BLK0, BLK1 | Sets all raster blanking | | | | | | | | | | | | | | | | | | |
| | | 1 | All raster blanking | | | | | | | | | | | | | | | | | | | |
| 1 | B/F | 0 | Synchronize with the leading edge of horizontal synchronization. | Synchronize with the front porch or back porch of the horizontal synchronization signal. | | | | | | | | | | | | | | | | | | |
| | | 1 | Synchronize with the trailing edge of horizontal synchronization. | | | | | | | | | | | | | | | | | | | |
| 2 | VMASK | 0 | Do not mask by VERT input signal | This register has or do not have mask at phase comparison operating. | | | | | | | | | | | | | | | | | | |
| | | 1 | Mask by VERT input signal | | | | | | | | | | | | | | | | | | | |
| 3 | POLV | 0 | VERT pin is negative polarity | Set VERT pin polarity. | | | | | | | | | | | | | | | | | | |
| | | 1 | VERT pin is positive polarity | | | | | | | | | | | | | | | | | | | |
| 4 | POLH | 0 | HOR pin is negative polarity | Set HOR pin polarity. | | | | | | | | | | | | | | | | | | |
| | | 1 | HOR pin is positive polarity | | | | | | | | | | | | | | | | | | | |
| 5 | BLK0 | 0 | <table border="1"> <thead> <tr> <th colspan="2">BLK</th> <th rowspan="2">Blanking mode</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td></td> </tr> <tr> <td>0</td> <td>0</td> <td>Matrix-outline size</td> </tr> <tr> <td>0</td> <td>1</td> <td>Character size</td> </tr> <tr> <td>1</td> <td>0</td> <td>Border size</td> </tr> <tr> <td>1</td> <td>1</td> <td>Matrix-outline size</td> </tr> </tbody> </table> | BLK | | Blanking mode | 1 | 0 | | 0 | 0 | Matrix-outline size | 0 | 1 | Character size | 1 | 0 | Border size | 1 | 1 | Matrix-outline size | Set blanking mode. (Note 1) An example of blanking mode at BCOL = "0", DSPn = "0" (n = 0 to 11) shown left. |
| BLK | | Blanking mode | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | Matrix-outline size | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | Character size | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | Border size | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | Matrix-outline size | | | | | | | | | | | | | | | | | | | | |
| 6 | BLK1 | 1 | | | | | | | | | | | | | | | | | | | | |
| 7 | SYAD | 0 | Border display of character | (Note 2) | | | | | | | | | | | | | | | | | | |
| | | 1 | Shadow display of character | | | | | | | | | | | | | | | | | | | |
| 8 | RAMERS | 0 | RAM not erased | There is no need to reset because there is no register for this bit. | | | | | | | | | | | | | | | | | | |
| | | 1 | RAM erased | | | | | | | | | | | | | | | | | | | |
| 9 | STOP | 0 | Oscillation of clock for display | R, G, B and BLNK0 output can be altered. | | | | | | | | | | | | | | | | | | |
| | | 1 | Stop the oscillation of clock for display | | | | | | | | | | | | | | | | | | | |
| A | DSPON | 0 | Display OFF | Display can be altered. | | | | | | | | | | | | | | | | | | |
| | | 1 | Display ON | | | | | | | | | | | | | | | | | | | |
| B | BLINK0 | 0 | <table border="1"> <thead> <tr> <th colspan="2">BLINK</th> <th rowspan="2">Duty</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td></td> </tr> <tr> <td>0</td> <td>0</td> <td>Blinking OFF</td> </tr> <tr> <td>0</td> <td>1</td> <td>25%</td> </tr> <tr> <td>1</td> <td>0</td> <td>50%</td> </tr> <tr> <td>1</td> <td>1</td> <td>75%</td> </tr> </tbody> </table> | BLINK | | Duty | 1 | 0 | | 0 | 0 | Blinking OFF | 0 | 1 | 25% | 1 | 0 | 50% | 1 | 1 | 75% | Blinking duty ratio can be altered. |
| | | BLINK | | Duty | | | | | | | | | | | | | | | | | | |
| 1 | 0 | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | Blinking OFF | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 25% | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 50% | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 75% | | | | | | | | | | | | | | | | | | | | |
| C | BLINK1 | 1 | | | | | | | | | | | | | | | | | | | | |
| D | BLINK2 | 0 | Divided into 64 of vertical synchronous signal | Blinking frequency can be altered. | | | | | | | | | | | | | | | | | | |
| | | 1 | Divided into 32 of vertical synchronous signal | | | | | | | | | | | | | | | | | | | |
| E | TEST13 | 0 | It should be fixed to "0". | | | | | | | | | | | | | | | | | | | |
| | | 1 | Test mode | | | | | | | | | | | | | | | | | | | |

Notes 1: Refer to DISPLAY FORM 1 2: Refer to DISPLAY FORM 3

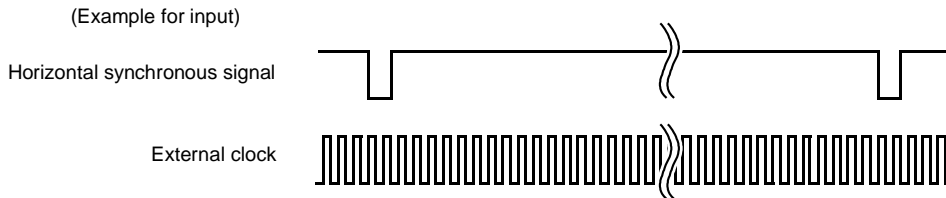
REGISTER SUPPLEMENTARY DESCRIPTION

(1) Setting external clock input mode (by use of EXCK0 (120₁₆) and EXCK1 (123₁₆))

Two modes given below are available for the external clock signal input. (the settings (EXCK1, EXCK0) = (0, 1), (1, 0) are forbidden.)

(a) When (EXCK1, EXCK0) = (0, 0), Fosc = 20 to 30 MHz
 Input from the TCK pin a constant-period continuous external clock that synchronizes with the horizontal synchronization signal. And input from HOR pin a constant-period continuous horizontal synchronous signal.
 Never stop inputting the clock while displaying.
 Do not have to set a display frequency because the clock just as it is entered from outside is used as the display clock.

(b) When (EXCK1, EXCK0) = (1, 1), Fosc = 20 to 80 MHz
 Input from the TCK pin a constant-period continuous external clock that synchronizes with the horizontal synchronization signal.
 Never stop inputting the clock while displaying.
 Be sure to set a display frequency because the internal clock made to synchronize with the clock input from outside is used as the display clock (see the next page).



(2) Setting display frequencies

Set a display frequency by setting a frequency value for the horizontal synchronization signal by use of DIV10 to DIV0 (120₁₆).

Set display frequency area in conformity with the frequency of the external clock signal.

Set display frequency area by use of DIVS0, DIVS1 (120₁₆), RSEL0 (121₁₆), and RSEL1 (122₁₆). Frequency area are as follows.

| RSEL1 | RSEL0 | DIVS1 | DIVS0 | Display frequency area |
|-------|-------|-------|-------|------------------------|
| 0 | 1 | 0 | 0 | 70.0 to 80.0 |
| 0 | 0 | 0 | 0 | 63.0 to 70.0 |
| 1 | 0 | 0 | 1 | 56.6 to 63.0 |
| 0 | 1 | 0 | 1 | 46.6 to 56.6 |
| 0 | 0 | 0 | 1 | 45.0 to 46.6 |
| 1 | 0 | 1 | 0 | 42.5 to 45.0 |
| 0 | 1 | 1 | 0 | 35.0 to 42.5 |
| 0 | 0 | 1 | 0 | 31.5 to 35.0 |
| 1 | 0 | 1 | 1 | 28.3 to 31.5 |
| 0 | 1 | 1 | 1 | 23.3 to 28.3 |
| 0 | 0 | 1 | 1 | 20.0 to 23.3 |

Cautions in setting a display frequency

To change the external clock frequency or the horizontal synchronization frequency, follow the steps in sequence given below.

- (a) Display OFF (DSPON = 0)
- (b) Set the display frequency (Use DIV10 to DIV0 (120₁₆), DIVS0, DIVS1 (120₁₆), RSEL0 (121₁₆), and RSEL1 (122₁₆).
- (c) 20-ms waiting time with the horizontal synchronization signal and the external clock signal being input
- (d) Display ON (DSPON = 1)

DISPLAY FORM1

Table 1 shows display form of blanking.

Table 1. Display mode

| BCOL | Standard blanking | | When the all of registers DSPn (Note 2) are set to "0" | When some of registers DSPn are set to "1" | | BLNK0 output |
|---------------|-------------------|------|--|--|--|---|
| | BLK1 | BLK0 | | DSPn = 0 | DSPn = 1 | |
| 0 | 0 | 0 | Matrix-outline and border display. color set: FR, FG, FB or display RAM (Note 4) | Matrix-outline and border display. color set: FR, FG, FB or display RAM (Note 4) | Matrix-outline display color set: display RAM (Note 3) | DSPn = "0" line } DSPn = "1" line } Matrix-outline size |
| | 0 | 1 | Character | Character | Border display color set: display RAM (Note 3) | |
| | 1 | 0 | Border display color set: display RAM (Note 3) | Border display color set: display RAM (Note 3) | Matrix-outline display color set: display RAM (Note 3) | DSPn = "0" line → Border size DSPn = "1" line → Matrix-outline size |
| | 1 | 1 | Matrix-outline display color set: display RAM (Note 3) | Matrix-outline display color set: display RAM (Note 3) | Character | DSPn = "0" line → Matrix-outline size DSPn = "1" line → Character size |
| 1 (Note 1) | 0 | 0 | Matrix-outline and border display. color set: FR, FG, FB or display RAM (Note 4) | Matrix-outline and border display. color set: FR, FG, FB or display RAM (Note 4) | Matrix-outline display color set: display RAM (Note 3) | All blanking size |
| | 0 | 1 | Character | Character | Border display color set: display RAM (Note 3) | |
| | 1 | 0 | Border display color set: display RAM (Note 3) | Border display color set: display RAM (Note 3) | Matrix-outline display color set: display RAM (Note 3) | |
| | 1 | 1 | Matrix-outline display color set: display RAM (Note 3) | Matrix-outline display color set: display RAM (Note 3) | Character | |

Notes 1: Color setting of raster area is set by register RR, RG and RB.

2: DSPn (n = 0 to 11)

3: Set by BR, BG and BB of display RAM.

4: Set border by register FR, FG and FB. Set matrix-outline by BR, BG and BB of display RAM.

DISPLAY FORM 2

M35046-XXXSP/FP has the following four display forms.

- (1) Character size
: Blanking same as the character size.
- (2) Border size
: Blanking the background as a size from character.
- (3) Matrix-outline size
: Blanking the background 12 × 18 dot.
When set register BETA14 to "1", setting of blanking the background 14 × 18 dot is possible.
- (4) All blanking size
: When set register BCOL to "1", all raster area is blanking.

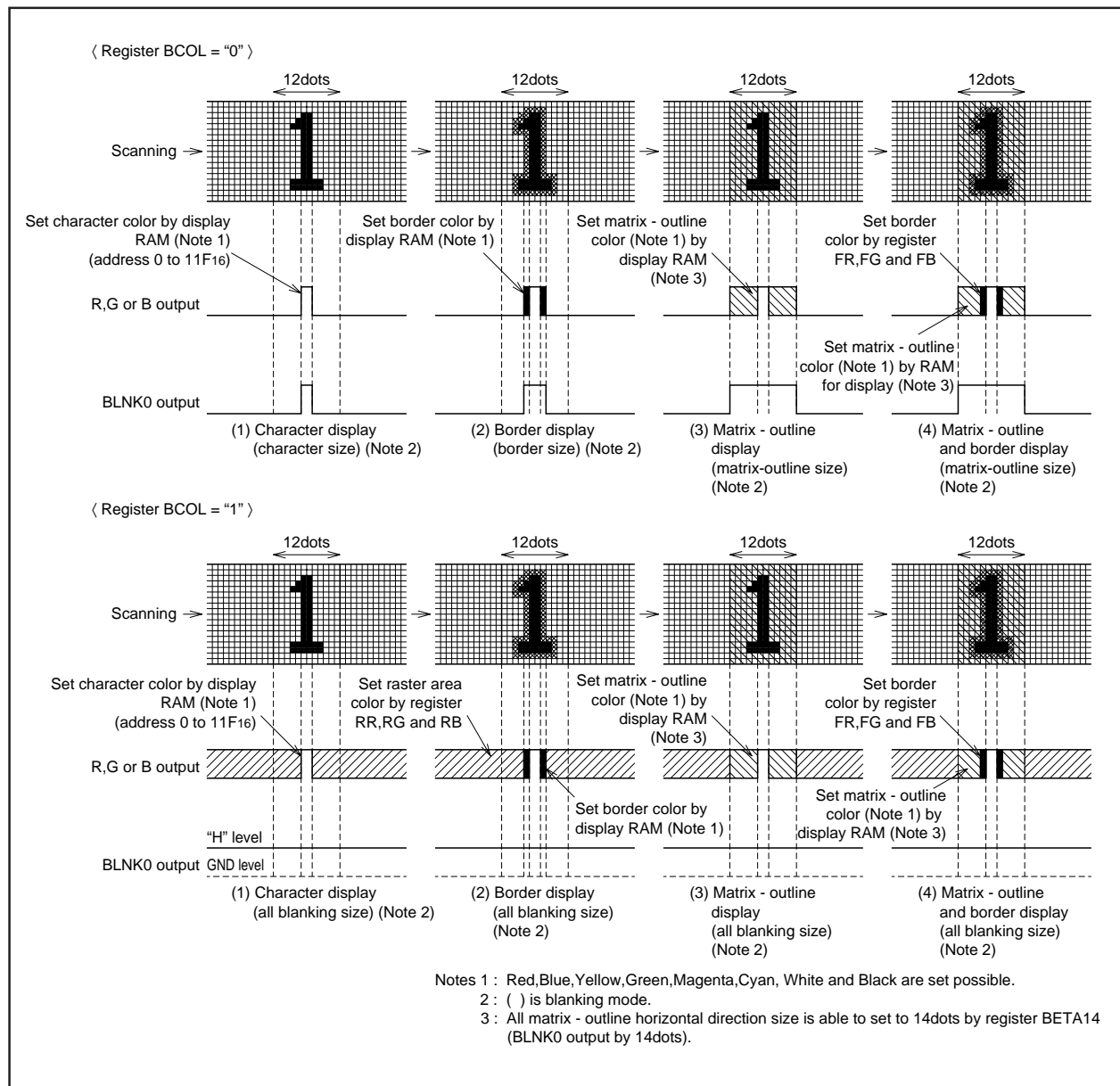


Fig. 3 Display form

DISPLAY FORM 3

When border display mode, if set SYAD = "0" to "1", it change to shadow display mode.

Border and shadow display are shown below.

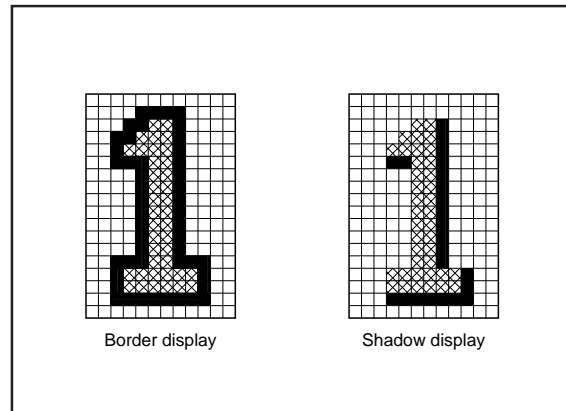


Fig. 4 Border and shadow display

Set shadow display color by display RAM or register FR, FG and FB.

DATA INPUT EXAMPLE

Data of display RAM and display control registers can be set by the serial input function. Example of data setting is shown in Figure 5 and Figure 6.

(1) At EXCK0 = "0", EXCK1 = "0" setting

| Example of data setting by the serial input function (M35046-XXXSP/FP) | | | | | | | | | | | | | | | | | | |
|--|---------------------------|-----------------------|----------------------------|------|------|----------|-----------------|-----|----------------|-----|-----|-----|------|------|-----|-----|-------------------|-------------------------------------|
| | | DAF | DAE | DAD | DAC | DAB | DAA | DA9 | DA8 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 | Addition |
| | | 200 msec hold | | | | | | | | | | | | | | | System set-up | |
| 1 | address 120 ₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Address set |
| 2 | data 120 ₁₆ | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | (Note 1) |
| 3 | data 121 ₁₆ | 0 | 0 | PTD7 | PTD6 | 1 | PTD4 | 1 | PTD2 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | Output setting |
| 4 | data 122 ₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | HP9 | HP8 | HP7 | HP6 | HP5 | HP4 | HP3 | HP2 | HP1 | HP0 | Horizontal display location setting |
| 5 | data 123 ₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | VP9 | VP8 | VP7 | VP6 | VP5 | VP4 | VP3 | VP2 | VP1 | VP0 | Vertical display location setting |
| 6 | data 124 ₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Display form setting |
| 7 | data 125 ₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Character size setting |
| 8 | data 126 ₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Character size setting |
| 9 | data 127 ₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Color, character size setting |
| 10 | data 128 ₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | POLH | POLV | 0 | 0 | 0 | Display OFF, display form (Note 2) |
| 11 | data 000 ₁₆ | 0 | BB | BG | BR | BLINK | B | G | R | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 | |
| 12 ⋮ ⋮ ⋮ 297 | ⋮ ⋮ ⋮ ⋮ ⋮ | ⋮ ⋮ ⋮ ⋮ ⋮ | Character background color | | | Blinking | Character color | | Character code | | | | | | | | Character setting | |
| 298 | data 11F ₁₆ | 0 | BB | BG | BR | BLINK | B | G | R | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 | |
| 299 | address 128 ₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | Address setting |
| 300 | data 128 ₁₆ | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | POLH | POLV | 0 | 0 | 0 | Display ON, display form (Note 2) |

Notes 1 : Input the horizontal synchronous signal to the HOR pin and the vertical synchronous signal to the VERT pin. If serrated pulses are present in the vertical synchronous signal, set the register VMASK to 1.
2 : Matrix-outline display in this data.

Fig. 5 Example of data setting by the serial input function (1)

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(2) At EXCK0 = "1", EXCK1 = "1" setting

| | | DAF | DAE | DAD | DAC | DAB | DAA | DA9 | DA8 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 | Addition |
|--------------------------|---------------------------|---|----------------------------|------|-------|-----------|-----------------|------|------|----------------|------|------|------|------|------|------|---------------|--|
| | | 200 msec hold | | | | | | | | | | | | | | | System set-up | |
| 1 | address 120 ₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Address set |
| 2 | data 120 ₁₆ | 0 | 1 | 1 | DIVS1 | DIVS0 | DIV10 | DIV9 | DIV8 | DIV7 | DIV6 | DIV5 | DIV4 | DIV3 | DIV2 | DIV1 | DIV0 | Set frequency value of horizontal synchronous frequency(Note 1) |
| 3 | data 121 ₁₆ | 0 | RSEL0 | PTD7 | PTD6 | 1 | PTD4 | 1 | PTD2 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | Output setting Oscillation circuit setting |
| 4 | data 122 ₁₆ | 0 | RSEL1 | 0 | 0 | 0 | 0 | HP9 | HP8 | HP7 | HP6 | HP5 | HP4 | HP3 | HP2 | HP1 | HP0 | Horizontal display location setting Oscillation circuit setting |
| 5 | data 123 ₁₆ | 0 | 1 | 0 | 0 | 0 | 0 | VP9 | VP8 | VP7 | VP6 | VP5 | VP4 | VP3 | VP2 | VP1 | VP0 | Vertical display location setting |
| 6 | data 124 ₁₆ | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Display form setting |
| 7 | data 125 ₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Character size setting |
| 8 | data 126 ₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Character size setting |
| 9 | data 127 ₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Color, character size setting |
| 10 | data 128 ₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | POLH | POLV | 0 | 0 | 0 | Display OFF, display form (Note 2) |
| | | Hold the time length as 1V of vertical synchronous signal | | | | | | | | | | | | | | | | |
| 11 | data 000 ₁₆ | 0 | BB | BG | BR | BLINK | B | G | R | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 | Character setting |
| 12 ⋮ ⋮ ⋮ 297 | ⋮ ⋮ ⋮ ⋮ | ⋮ ⋮ ⋮ ⋮ | Character background color | | | BLINK-ING | Character color | | | Character code | | | | | | | | |
| 298 | data 11F ₁₆ | 0 | BB | BG | BR | BLINK | B | G | R | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 | |
| 299 | address 128 ₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | |
| 300 | data 128 ₁₆ | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | POLH | POLV | 0 | 0 | 0 | Display ON, display form (Note 2) |

Notes 1 : From this time, input clock to TCK pin. And, input the horizontal synchronous signal to the HOR pin and the vertical synchronous signal to the VERT pin. If serrated pulses are present in the vertical synchronous signal, set the register VMASK to 1.
2 : Matrix-outline display in this data.

Fig. 6 Example of data setting by the serial input function (2)

SERIAL DATA INPUT TIMING

- (1) Serial data should be input with the LSB first.
- (2) The address consists of 16 bits.
- (3) The data consists of 16 bits.
- (4) The 16 bits in the SCK after the \overline{CS} signal has fallen are the address, and for succeeding input data, the address is incremented every 16 bits. Therefore, it is not necessary to input the address from the second data.

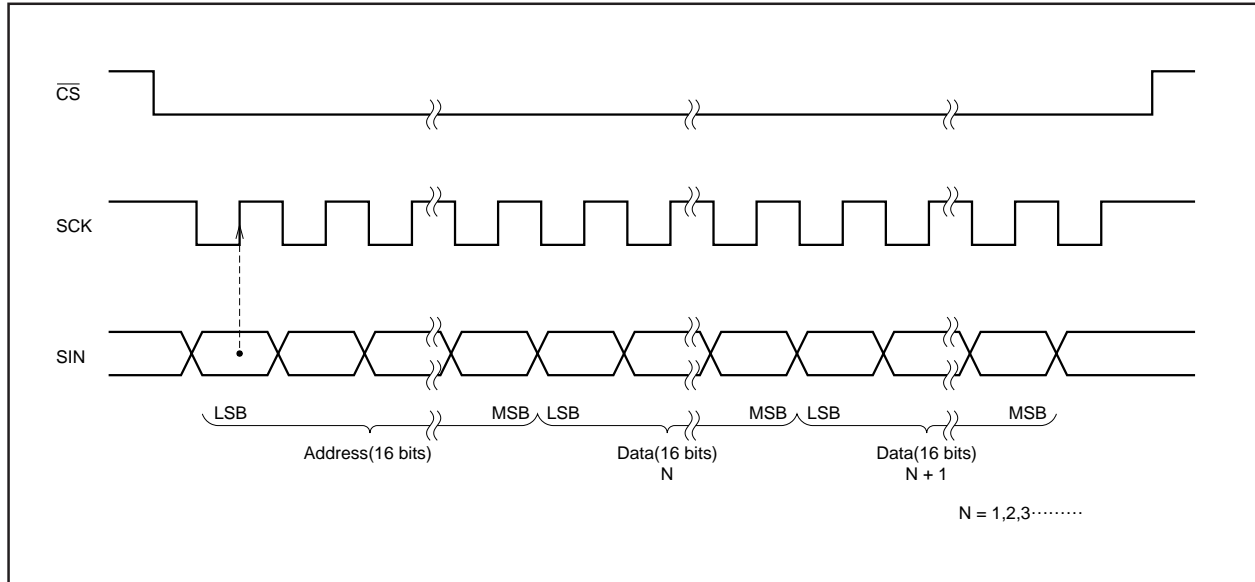


Fig. 7 Serial input timing

CHARACTER FONT

Images are composed on a 12 × 18 dot matrix, and characters can be linked vertically and horizontally with other characters to allow the display the continuous symbols.

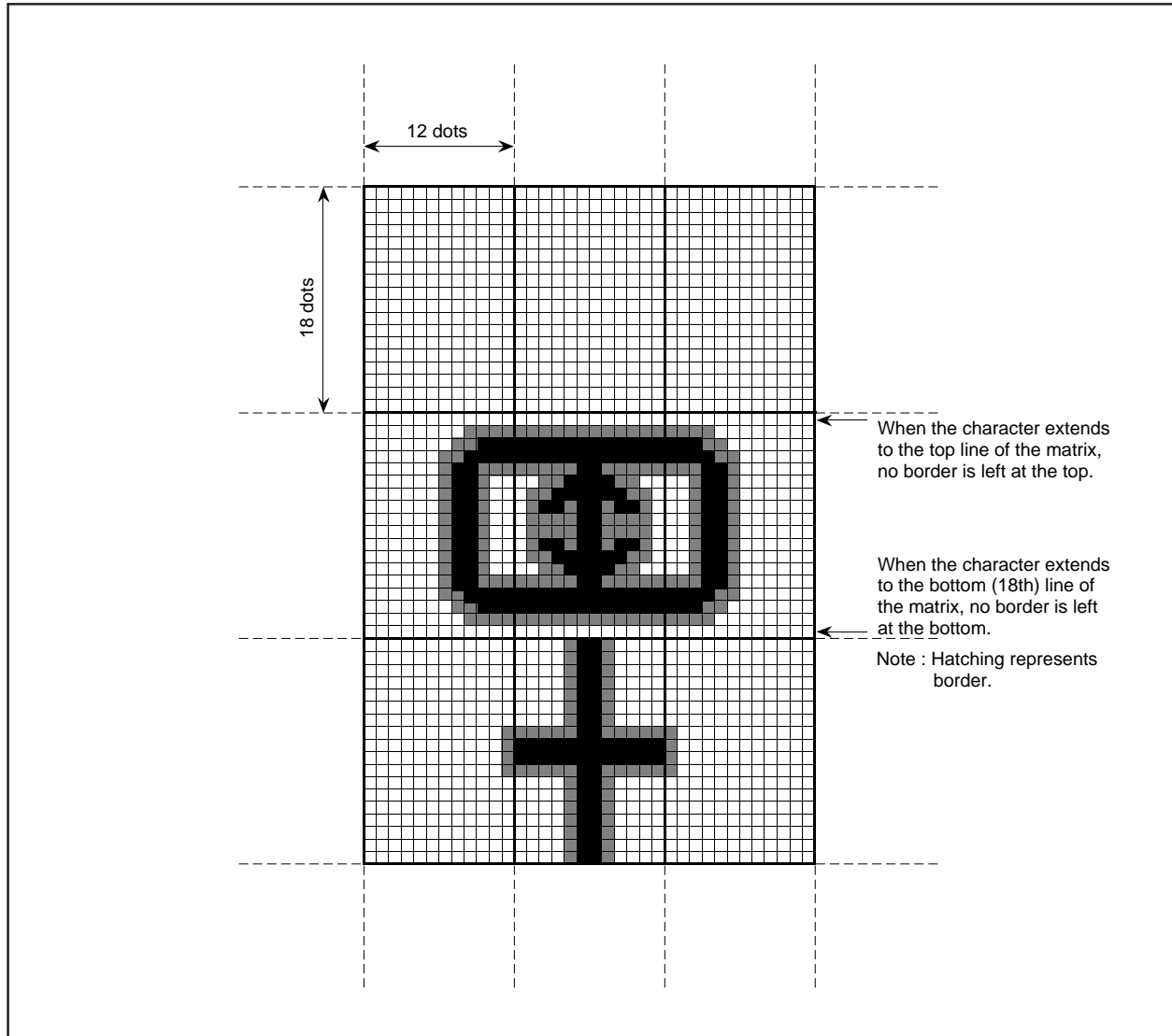


Fig. 8 Example for displaying a continuous pattern after combining characters in the horizontal or vertical direction

Character code FF16 is fixed as a blank without background.
Therefore, cannot register a character font in this code.

TIMING REQUIREMENTS ($T_a = -20^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{DD} = 5 \pm 0.25\text{V}$, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit | Remarks |
|----------------------|---------------------|--------|------|------|---------------|--------------|
| | | Min. | Typ. | Max. | | |
| $t_w(\text{SCK})$ | SCK width | 200 | — | — | ns | See Figure 9 |
| $t_{su}(\text{CS})$ | CS setup time | 200 | — | — | ns | |
| $t_h(\text{CS})$ | CS hold time | 2 | — | — | μs | |
| $t_{su}(\text{SIN})$ | SIN setup time | 200 | — | — | ns | |
| $t_h(\text{SIN})$ | SIN hold time | 200 | — | — | ns | |
| t_{word} | 1 word writing time | 10 | — | — | μs | |

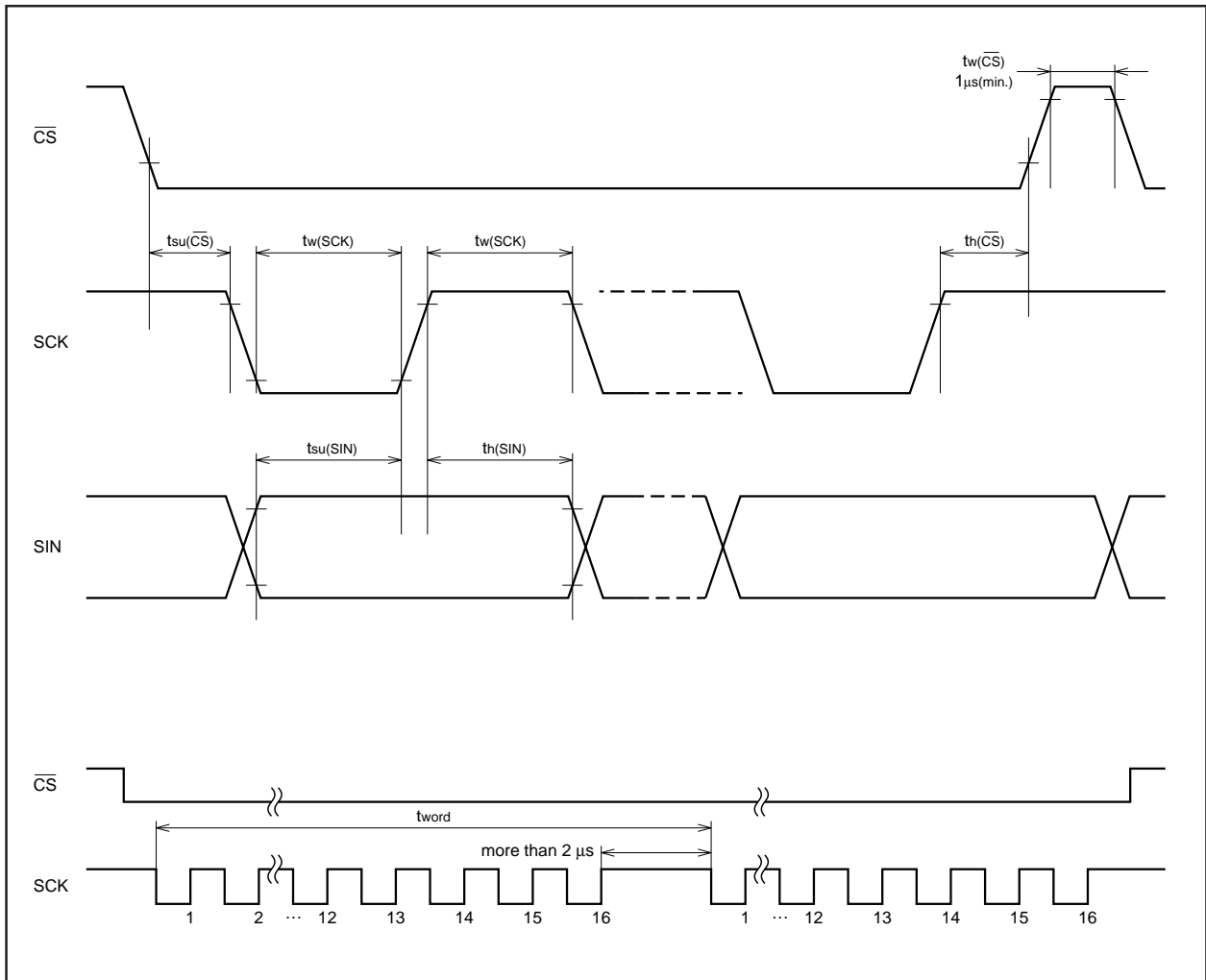


Fig. 9 Serial input timing requirements

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|------------------|-----------------------|-----------------------------------|--|------|
| V _{DD} | Supply voltage | With respect to V _{SS} . | -0.3 to +6.0 | V |
| V _I | Input voltage | | V _{SS} - 0.3 ≤ V _I ≤ V _{DD} + 0.3 | V |
| V _O | Output voltage | | V _{SS} ≤ V _O ≤ V _{DD} | V |
| P _d | Power dissipation | T _a = 25°C | 300 | mW |
| T _{opr} | Operating temperature | | -20 to +85 | °C |
| T _{stg} | Storage temperature | | -40 to +125 | °C |

RECOMMENDED OPERATING CONDITIONS (V_{DD} = 5V, T_a = -20 to +85°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|-------------------|---|--------------------|-----------------|--------------------|------|
| | | Min. | Typ. | Max. | |
| V _{DD} | Supply voltage | 4.75 | 5.0 | 5.25 | V |
| V _{IH} | "H" level input voltage SIN, SCK, $\overline{\text{CS}}$, $\overline{\text{AC}}$ HOR, VERT | 0.8V _{DD} | V _{DD} | V _{DD} | V |
| V _{IL} | "L" level input voltage SIN, SCK, $\overline{\text{CS}}$, $\overline{\text{AC}}$ HOR, VERT | 0 | 0 | 0.2V _{DD} | V |
| F _{OSC} | Oscillating frequency for display | 20.0 | — | 80.0 | MHz |
| H _{sync} | Horizontal synchronous signal input frequency | 15.0 | — | 130.0 | kHz |

ELECTRICAL CHARACTERISTICS (V_{DD} = 5V, T_a = 25°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|------------------|---|---------------------------------|--------------------|------|--------------------|-----------------|
| | | | Min. | Typ. | Max. | |
| V _{DD} | Supply voltage | T _a = -20 to +85°C | 4.75 | 5.0 | 5.25 | V |
| I _{DD} | Supply current | V _{DD} = 5.25V | — | 30 | 50 | mA |
| V _{OH} | "H" level output voltage | P0 to P7 | 3.5 | — | — | V |
| | | CPOUT | | | | |
| V _{OL} | "L" level output voltage | P0 to P7 | — | — | 0.4 | V |
| | | CPOUT | | | | |
| R _I | Pull-up resistance SCK, $\overline{\text{AC}}$, $\overline{\text{CS}}$, SIN | V _{DD} = 5.0V | 10 | 30 | 100 | kΩ |
| V _{TCK} | External clock input width | 4.75V < V _{DD} ≤ 5.25V | 0.7V _{DD} | — | 0.9V _{DD} | V _{PP} |

NOTE FOR SUPPLYING POWER

Timing of power supplying to AC pin

The internal circuit of M35046-XXXSP/FP is reset when the level of the auto clear input pin \overline{AC} is "L". This pin is hysteresis input with the pull-up resistor. The timing about power supplying of \overline{AC} pin is shown in Figure 11.

Timing of power supplying to VDD1 and VDD2.

Supply power to VDD1 and VDD2 at the same time.

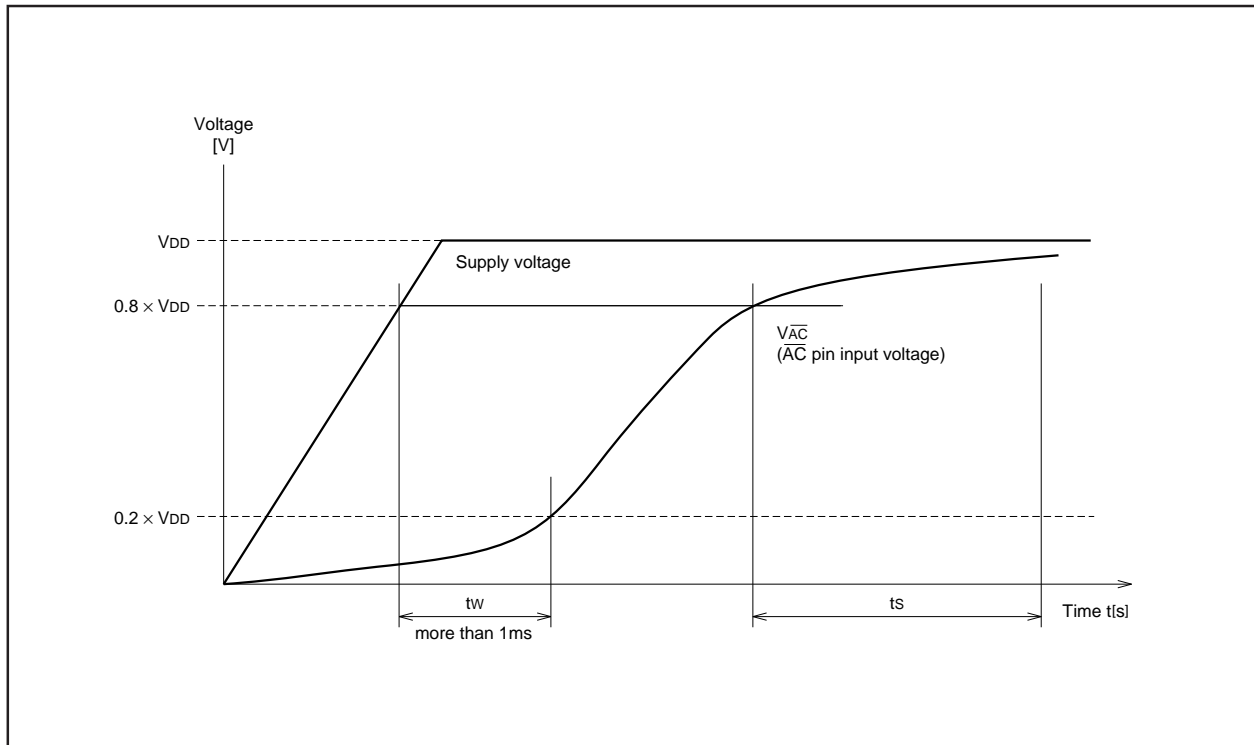


Fig. 11 Timing of power supplying to \overline{AC} pin

After supplying the power (V_{DD} and V_{SS}) to M35046-XXXSP/FP and the supply voltage becomes more than $0.8 \times V_{DD}$, it needs to keep V_{IL} time; t_w of the \overline{AC} pin for more than 1ms.

Start inputting from microcomputer after \overline{AC} pin supply voltage becomes more than $0.8 \times V_{DD}$ and keeping 200ms wait time.

PRECAUTION FOR USE

Notes on noise and latch-up

In order to avoid noise and latch-up, connect a bypass capacitor ($\approx 0.1\mu F$) directly between the V_{DD1} pin and V_{SS} pin, and the V_{DD2} pin and V_{SS} pin using a heavy wire.

DATA REQUIRED FOR MASK ROM ORDERING

Please send the following data for mask orders.

- (1) M35046-XXXSP/FP mask ROM order confirmation form
- (2) 20P4B mask specification form
- (3) 20P2Q-A mask specification form
- (4) ROM data (EPROM 3 sets)
- (5) Floppy disks containing the character font generating program + character data

STANDARD ROM TYPE : M35046-001SP/FP

M35046-001SP/FP is a standard ROM type of M35046-XXXSP/FP.

The character patterns are fixed to the contents of Figure 12 to 15.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

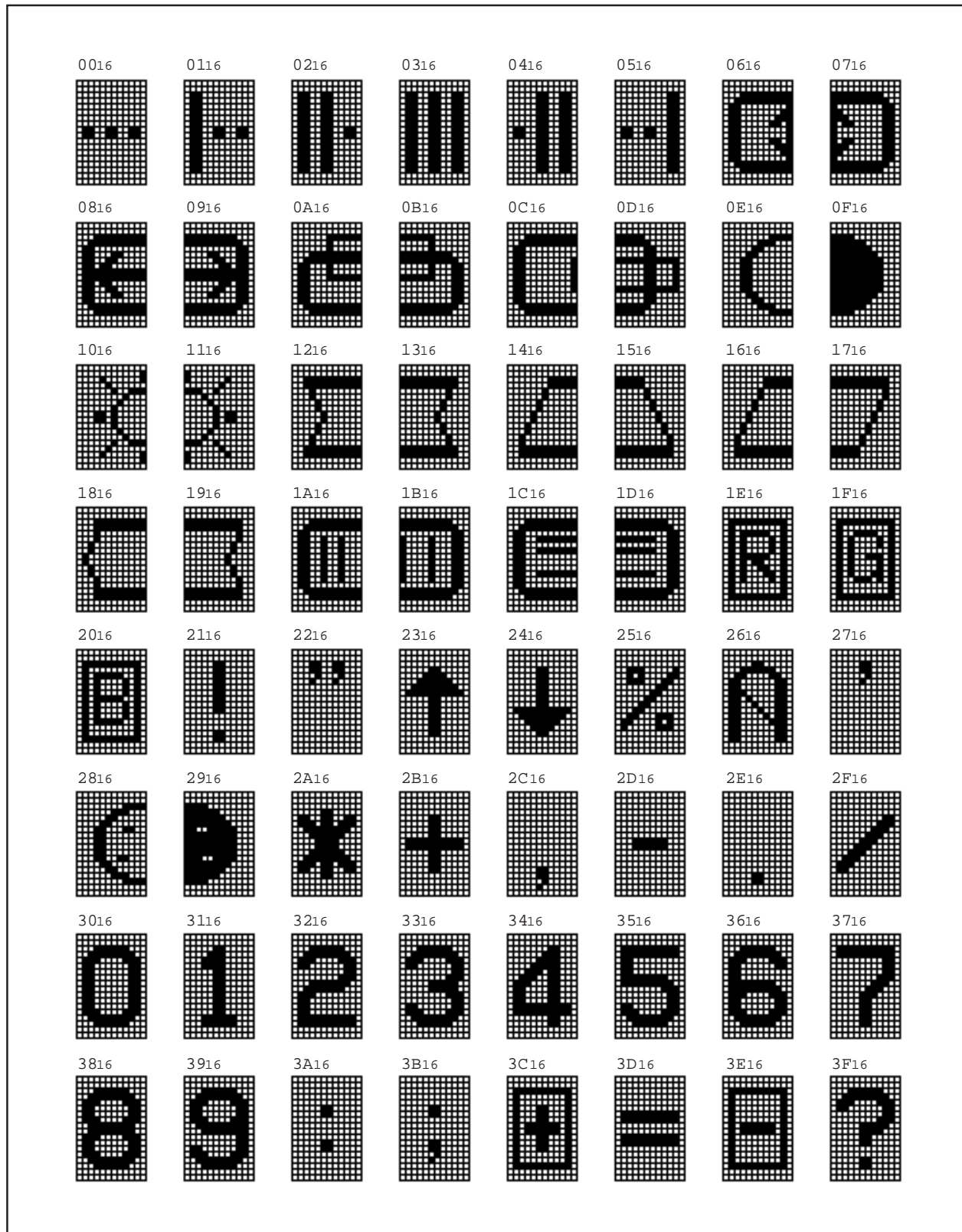


Fig. 12 M35046-001SP/FP character pattern (1)

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS



Fig. 13 M35046-001SP/FP character pattern (2)

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

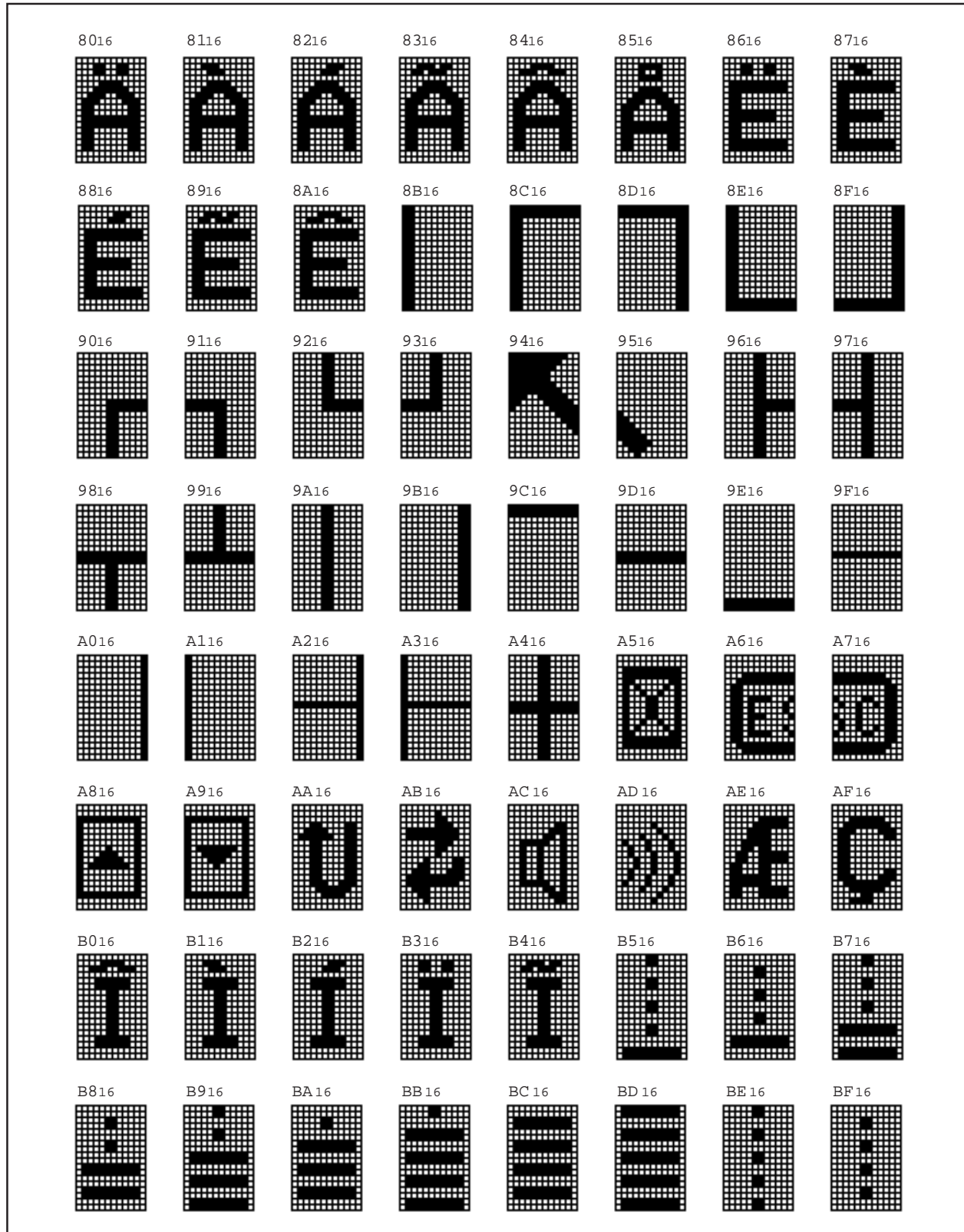


Fig. 14 M35046-001SP/FP character pattern (3)

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

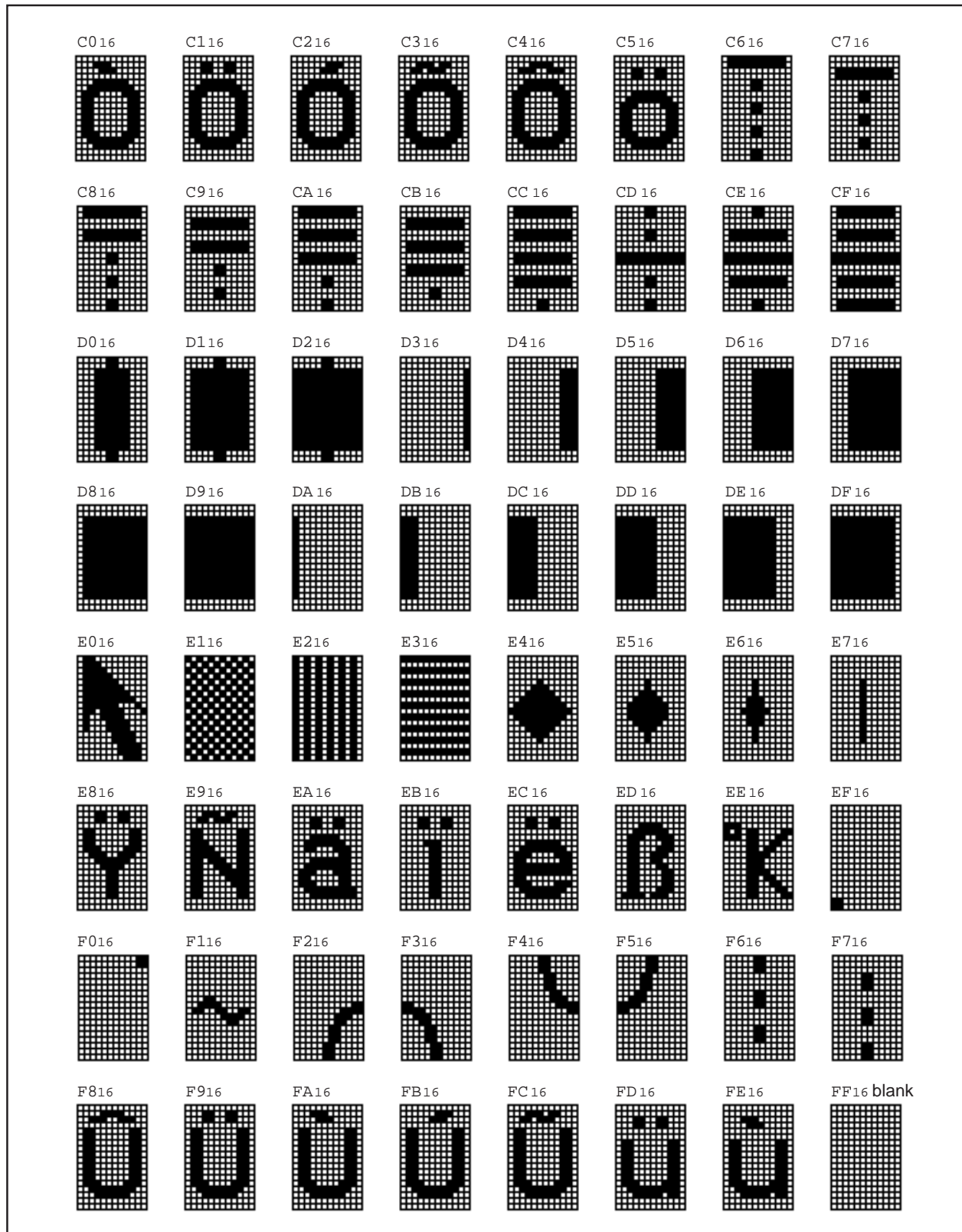


Fig. 15 M35046-001SP/FP character pattern (4)

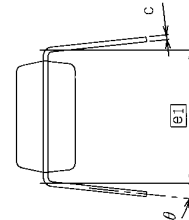
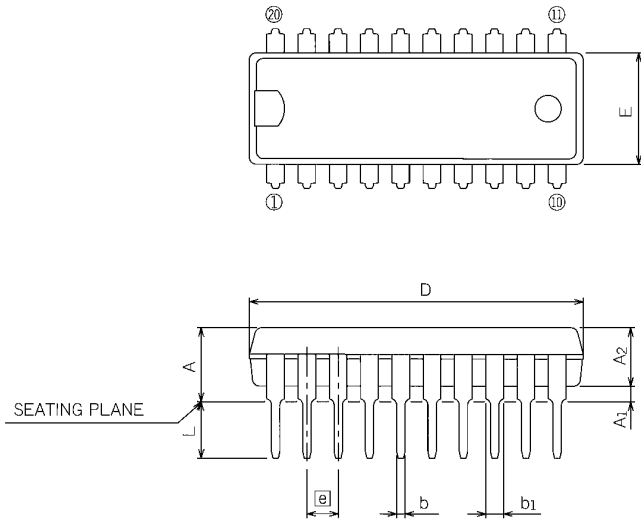
PACKAGE OUTLINE

20P4B

Plastic 20pin 300mil SDIP

| | | | |
|-------------------|------------|------------|---------------|
| EIAJ Package Code | JEDEC Code | Weight (g) | Lead Material |
| SDIP20-P-300-1.78 | — | 1.0 | |

Scale : 2.5/1



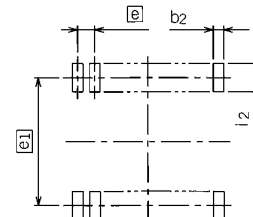
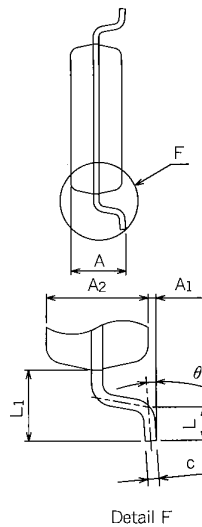
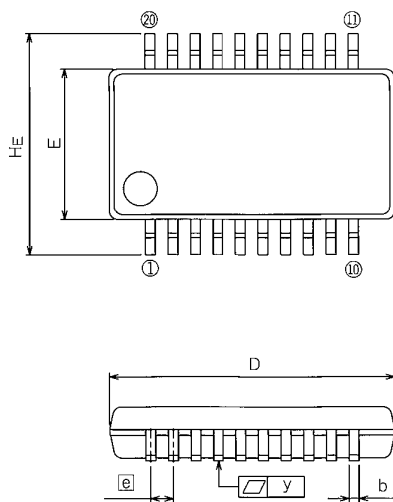
| Symbol | Dimension in Millimeters | | |
|--------|--------------------------|-------|------|
| | Min | Nom | Max |
| A | — | — | 4.5 |
| A1 | 0.51 | — | — |
| A2 | — | 3.3 | — |
| b | 0.38 | 0.48 | 0.58 |
| b1 | 0.9 | 1.0 | 1.3 |
| c | 0.22 | 0.27 | 0.34 |
| D | 18.8 | 19.0 | 19.2 |
| E | 6.15 | 6.3 | 6.45 |
| e | — | 1.778 | — |
| e1 | — | 7.62 | — |
| L | 3.0 | — | — |
| θ | 0° | — | 15° |

20P2Q-A

Plastic 20pin 300mil SSOP

| | | | |
|-------------------|------------|------------|---------------|
| EIAJ Package Code | JEDEC Code | Weight (g) | Lead Material |
| SSOP020-P-0300 | — | 0.2 | Cu Alloy |

Scale : 4/1



Recommended Mount Pad

| Symbol | Dimension in Millimeters | | |
|--------|--------------------------|------|------|
| | Min | Nom | Max |
| A | — | — | 2.1 |
| A1 | 0 | 0.1 | 0.2 |
| A2 | — | 1.8 | — |
| b | 0.3 | 0.35 | 0.45 |
| c | 0.18 | 0.2 | 0.25 |
| D | 10.0 | 10.1 | 10.2 |
| E | 5.2 | 5.3 | 5.4 |
| e | — | 0.8 | — |
| HE | 7.5 | 7.8 | 8.1 |
| L | 0.4 | 0.6 | 0.8 |
| L1 | — | 1.25 | — |
| y | — | — | 0.1 |
| θ | 0° | — | 8° |
| b2 | — | 0.5 | — |
| e1 | — | 7.62 | — |
| l2 | 1.27 | — | — |

Renesas Technology Corp.

Nippon Bldg.,6-2,Otemachi 2-chome,Chiyoda-ku,Tokyo,100-0004 Japan

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REVISION DESCRIPTION LIST

M35046-XXXSP/FP DATA SHEET

| Rev. No. | Revision Description | Rev. date |
|----------|---|-----------|
| 1.0 | First Edition | 9902 |
| 1.1 | Delete Mask ROM ORDER CONFIRMATION FORM and MASK SPECIFICATION FORM | 0008 |
| | | |