M35075-XXXFP

REJ03B0180-0110
Rev.1.10
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SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

DESCRIPTION

The M35075-XXXFP is a character pattern display control IC can display on the CRT display the liquid crystal display and the plasma display. It uses a silicon gate CMOS process and it housed in a 24-pin shrink SOP package (M35075-XXXFP).
For M35075-001FP that is a standard ROM version of M35075-XXXFP respectively, the character pattern is also mentioned.

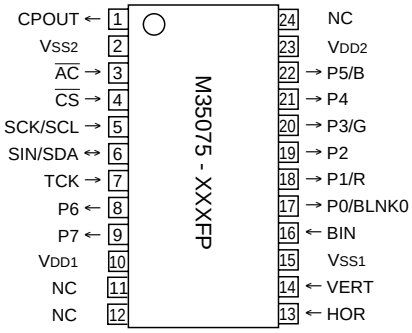
FEATURES

- Screen composition ..... 24 characters × 12 lines
- Number of characters displayed ..... 288 (Max.)
- Character composition ..... 12 × 18 dot matrix
- Characters available ..... ROM character:255 characters
  RAM character:8 characters
- Character sizes available ..... 4 (vertical) × 2 (horizontal)
- Display locations available
  Horizontal direction ..... 2007 locations
  Vertical direction ..... 2047 locations
- Blinking ..... Character units
  Cycle : division of vertical synchronization signal into 32 or 64
  Duty : 25%, 50%, or 75%
- Data input ..... By the I²C-BUS serial input function
- Coloring for ROM character
  Character color ..... 8 colors (Character unit)
  Background coloring ..... 8 colors (Character unit)
  Border (shadow) coloring ..... 8 colors (unit of screen / character unit)
  Raster coloring..... 8 colors (unit of screen)
- Blanking for ROM character
  Character size blanking
  Border size blanking
  Matrix-outline blanking
  All blanking (all raster area)
- Coloring for RAM character..... 8 colors (dot by dot)
- Blanking for RAM character
  Character size blanking
  Matrix-outline blanking
  All blanking (all raster area)
- Output ports
  4 shared output ports (toggled between RGB output)
  4 dedicated output ports
- Display RAM erase function
- Display input frequency range ..... Fosc = 20.0MHz to 110.0MHz
- Horizontal synchronous input frequency
  ..... H.sync = 15 kHz to 130 kHz
- Display oscillation stop function

<VDD=5V>

- Display input frequency range
  External clock mode 1 ..... Fosc = 6.3 MHz to 80.0 MHz
  External clock mode 2 ..... Fosc = 20.0 MHz to 110.0 MHz
  Internal clock mode ..... Fosc = 20.0 MHz to 110.0 MHz
- Horizontal synchronous input frequency
  ..... H.sync = 15 kHz to 130 kHz

PIN CONFIGURATION (TOP VIEW)



Outline 24P2Q

<VDD=3V>

- Display input frequency range
  External clock mode 1 ..... Fosc = 6.3 MHz to 40 MHz
- Horizontal synchronous input frequency
  ..... H.sync = 15 kHz to 60 kHz

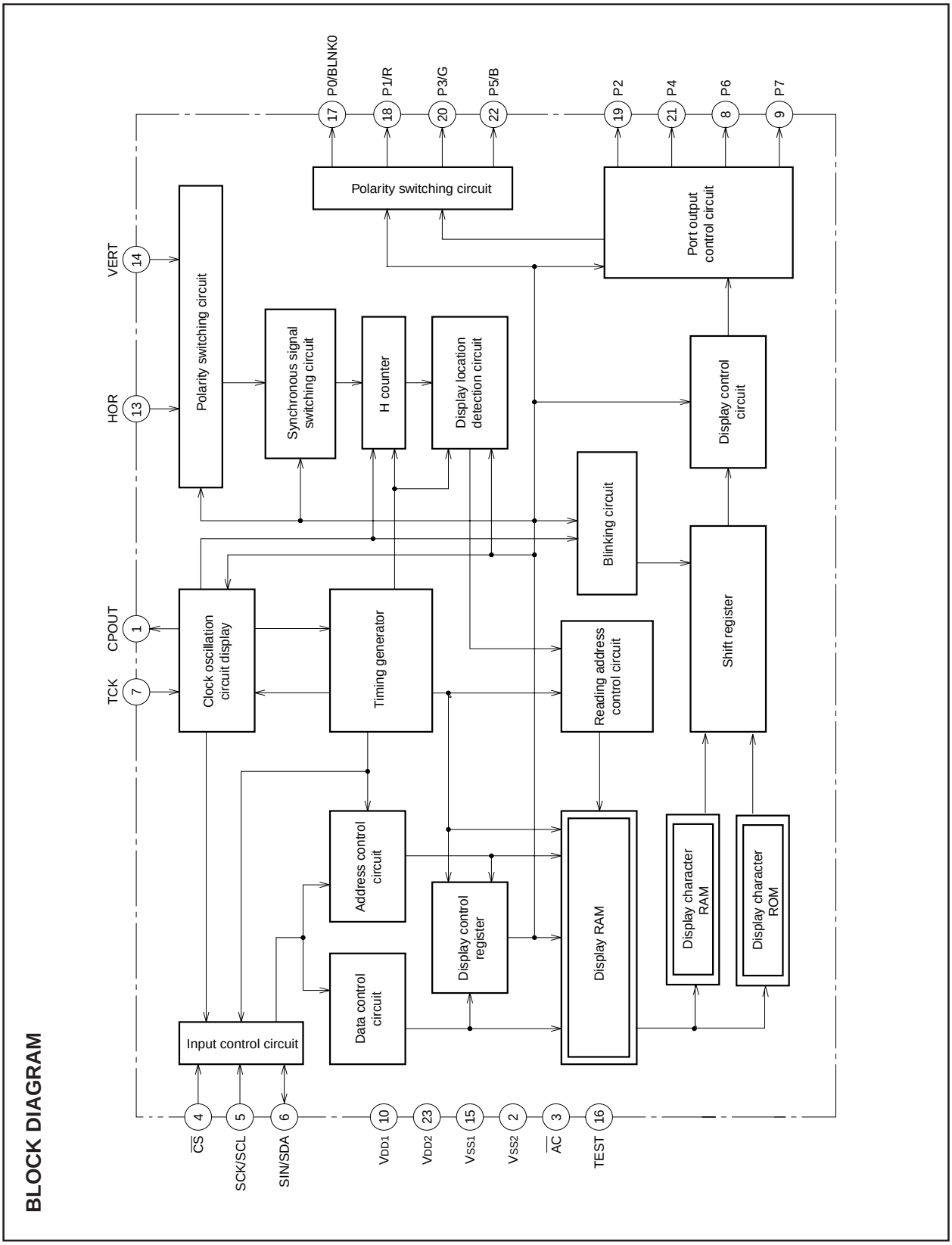
APPLICATION

CRT display, Liquid crystal display, Plasma display

PIN DESCRIPTION

Pin Number	Symbol	Pin name	Input/ Output	Function
1	CPOUT	Filter output	Output	Filter output. Connect loop filter to this pin.
2	V_{SS2}	Earthing pin	–	Please connect to GND using circuit earthing pin.
3	$\overline{AC}$	Auto-clear input	Input	When “L”, this pin resets the internal IC circuit. Hysteresis input. Built-in pull-up resistor.
4	$\overline{CS}$	Chip select input	Input	<at the 16-bit serial communication> Chip select pin. Set this pin to "L" level at serial data transfer. Hysteresis input. Built-in pull-up resistor.
				<at the I²C-BUS serial communication> Set this pin to “H” level.
5	SCK/SCL	Clock input	Input	<at the 16-bit serial communication> SIN pin serial data is taken in when SCK rises at $\overline{CS}$ pin "L" level. Hysteresis input.
				<at the I²C-BUS serial communication> SDA pin serial data is taken in synchronized with SCL.
6	SIN/SDA	Data input	Input	<at the 16-bit serial communication> This is the pin for serial input of display control register and display RAM data. Hysteresis input.
		Data I/O	I/O	<at the I²C-BUS serial communication> Hysteresis input. This is the pin for serial input of display control register and display RAM data. Also this pin output acknowledge signal.
7	TCK	External clock	Input	This is the pin for external clock input.
8	P6	Port P6 output	Output	This is the output port.
9	P7	Port P7 output	Output	This is the output port.
10	V_{DD1}	Power pin	–	Please connect to +5V with the power pin.
11	NC	–	–	This is NC pin. Please open this pin.
12	NC	–	–	This is NC pin. Please open this pin.
13	HOR	Horizontal synchro-nous signal input	Input	This pin inputs the horizontal synchronous signal. Hysteresis input.
14	VERT	Vertical synchro-nous signal input	Input	This pin inputs the vertical synchronous signal. Hysteresis input.
15	V_{SS1}	Earthing pin	–	Please connect to GND using circuit earthing pin.
16	BIN	Test pin	Input	Test pin. Connect to 0V.
17	P0/BLNK0	Port P0 output	Output	This pin can be toggled between port pin output and BLNK0 signal output.
18	P1/R	Port P1 output	Output	This pin can be toggled between port pin output and R signal output.
19	P2	Port P2 output	Output	This is the output port.
20	P3/G	Port P3 output	Output	This pin can be toggled between port pin output and G signal output.
21	P4	Port P4 output	Output	This is the output port.
22	P5/B	Port P5 output	Output	This pin can be toggled between port pin output and B signal output.
23	V_{DD2}	Power pin	–	Please connect to +5V with the power pin.
24	NC	–	–	This is NC pin. Please open this pin.

BLOCK DIAGRAM



MEMORY CONSTITUTION

Address 000_{16} to $11F_{16}$ are assigned to the display RAM, address 120_{16} to 129_{16} are assigned to the display control registers and address 200_{16} to $2F1_{16}$ are assigned to the RAM characters. The internal circuit is reset and all display control registers (address 120_{16} to 129_{16}) are set to "0" when the $\overline{AC}$ pin level is "L". And then, RAM is not erased and be undefinited. For detail, see "DATA INPUT EXAMPLE". Memory constitution is shown in Figure 1 to 9.

Addresses	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
000_{16}	0	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
001_{16}	0	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
⋮	⋮	Background coloring			Blink-ing	Character color			Character code							
$11E_{16}$	0	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
$11F_{16}$	0	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
120_{16}	0	SPACE2	SPACE1	SPACE0	TEST10	DIV10	DIV9	DIV8	DIV7	DIV6	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0
121_{16}	0	EXCK1	EXCK0	RSEL1	RSEL0	DIVS2	DIVS1	DIVS0	PTC7	PTC6	PTC5	PTC4	PTC3	PTC2	PTC1	PTC0
122_{16}	0	TEST17	TEST16	TEST15	TEST14	TEST13	TEST12	TEST11	PTD7	PTD6	PTD5	PTD4	PTD3	PTD2	PTD1	PTD0
123_{16}	0	TEST3	TEST2	TEST1	TEST0	HP10	HP9	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0
124_{16}	0	TEST20	RBLK0	TEST19	TEST18	VP10	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
125_{16}	0	TEST23	TEST22	TEST21	DSP11	DSP10	DSP9	DSP8	DSP7	DSP6	DSP5	DSP4	DSP3	DSP2	DSP1	DSP0
126_{16}	0	TEST24	VSZ1H1	VSZ1H0	VSZ1L1	VSZ1L0	V1SZ1	V1SZ0	LIN9	LIN8	LIN7	LIN6	LIN5	LIN4	LIN3	LIN2
127_{16}	0	TEST25	VSZ2H1	VSZ2H0	VSZ2L1	VSZ2L0	V18SZ1	V18SZ0	LIN17	LIN16	LIN15	LIN14	LIN13	LIN12	LIN11	LIN10
128_{16}	0	TEST29	TEST32	HSZ20	TEST31	HSZ10	BETA14	TEST28	TEST27	TEST26	FB	FG	FR	RB	RG	RR
129_{16}	0	TEST30	BLINK2	BLINK1	BLINK0	DSPON	STOP	RAMERS	SYAD	BLK1	BLK0	POLH	POLV	VMASK	B/$\overline{F}$	BCOL

Fig.1 Memory constitution (Display RAM, Display Control register)

Address	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
200$_{16}$	0	BS	GS	RS	FR000B	FR000A	FR0009	FR0008	FR0007	FR0009	FR0005	FR0004	FR0003	FR0002	FR0001	FR0000
201$_{16}$	0	BS	GS	RS	FR001B	FR001A	FR0019	FR0018	FR0017	FR0019	FR0015	FR0014	FR0013	FR0012	FR0011	FR0010
202$_{16}$	0	BS	GS	RS	FR002B	FR002A	FR0029	FR0028	FR0027	FR0026	FR0025	FR0024	FR0023	FR0022	FR0021	FR0020
203$_{16}$	0	BS	GS	RS	FR003B	FR003A	FR0039	FR0038	FR0037	FR0036	FR0035	FR0034	FR0033	FR0032	FR0031	FR0030
204$_{16}$	0	BS	GS	RS	FR004B	FR004A	FR0049	FR0048	FR0047	FR0046	FR0045	FR0044	FR0043	FR0042	FR0041	FR0040
205$_{16}$	0	BS	GS	RS	FR005B	FR005A	FR0059	FR0058	FR0057	FR0056	FR0055	FR0054	FR0053	FR0052	FR0051	FR0050
206$_{16}$	0	BS	GS	RS	FR006B	FR006A	FR0069	FR0068	FR0067	FR0066	FR0065	FR0064	FR0063	FR0062	FR0061	FR0060
207$_{16}$	0	BS	GS	RS	FR007B	FR007A	FR0079	FR0078	FR0077	FR0076	FR0075	FR0074	FR0073	FR0072	FR0071	FR0070
208$_{16}$	0	BS	GS	RS	FR008B	FR008A	FR0089	FR0088	FR0087	FR0086	FR0085	FR0084	FR0083	FR0082	FR0081	FR0080
209$_{16}$	0	BS	GS	RS	FR009B	FR009A	FR0099	FR0098	FR0097	FR0096	FR0095	FR0094	FR0093	FR0092	FR0091	FR0090
20A$_{16}$	0	BS	GS	RS	FR00AB	FR00AA	FR00A9	FR00A8	FR00A7	FR00A6	FR00A5	FR00A4	FR00A3	FR00A2	FR00A1	FR00A0
20B$_{16}$	0	BS	GS	RS	FR00BB	FR00BA	FR00B9	FR00B8	FR00B7	FR00B6	FR00B5	FR00B4	FR00B3	FR00B2	FR00B1	FR00B0
20C$_{16}$	0	BS	GS	RS	FR00CB	FR00CA	FR00C9	FR00C8	FR00C7	FR00C6	FR00C5	FR00C4	FR00C3	FR00C2	FR00C1	FR00C0
20D$_{16}$	0	BS	GS	RS	FR00DB	FR00DA	FR00D9	FR00D8	FR00D7	FR00D6	FR00D5	FR00D4	FR00D3	FR00D2	FR00D1	FR00D0
20E$_{16}$	0	BS	GS	RS	FR00EB	FR00EA	FR00E9	FR00E8	FR00E7	FR00E6	FR00E5	FR00E4	FR00E3	FR00E2	FR00E1	FR00E0
20F$_{16}$	0	BS	GS	RS	FR00FB	FR00FA	FR00F9	FR00F8	FR00F7	FR00F6	FR00F5	FR00F4	FR00F3	FR00F2	FR00F1	FR00F0
210$_{16}$	0	BS	GS	RS	FR010B	FR010A	FR0109	FR0108	FR0107	FR0106	FR0105	FR0104	FR0103	FR0102	FR0101	FR0100
211$_{16}$	0	BS	GS	RS	FR011B	FR011A	FR0119	FR0118	FR0117	FR0116	FR0115	FR0114	FR0113	FR0112	FR0111	FR0110
212$_{16}$ ⋮ 21F$_{16}$	Can not be used															

Fig.2 Memory constitution (RAM character 0)

Address	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
220$_{16}$	0	BS	GS	RS	FR100B	FR100A	FR1009	FR1008	FR1007	FR1006	FR1005	FR1004	FR1003	FR1002	FR1001	FR1000
221$_{16}$ ⋮ 230$_{16}$	RAM character 1 data															
231$_{16}$	0	BS	GS	RS	FR111B	FR111A	FR1119	FR1118	FR1117	FR1116	FR1115	FR1114	FR1113	FR1112	FR1111	FR1110
232$_{16}$ ⋮ 23F$_{16}$	Can not be used															

Fig.3 Memory constitution (RAM character 1)

Address	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
240_{16}	0	BS	GS	RS	FR200B	FR200A	FR2009	FR2008	FR2007	FR2006	FR2005	FR2004	FR2003	FR2002	FR2001	FR2000
241_{16} ⋮ 250_{16}	RAM character 2 data															
251_{16}	0	BS	GS	RS	FR211B	FR211A	FR2119	FR2118	FR2117	FR2116	FR2115	FR2114	FR2113	FR2112	FR2111	FR2110
252_{16} ⋮ $25F_{16}$	Can not be used															

Fig.4 Memory constitution (RAM character 2)

Address	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
260_{16}	0	BS	GS	RS	FR300B	FR300A	FR3009	FR3008	FR3007	FR3006	FR3005	FR3004	FR3003	FR3002	FR3001	FR3000
261_{16} ⋮ 270_{16}	RAM character 3 data															
271_{16}	0	BS	GS	RS	FR311B	FR311A	FR3119	FR3118	FR3117	FR3116	FR3115	FR3114	FR3113	FR3112	FR3111	FR3110
272_{16} ⋮ $27F_{16}$	Can not be used															

Fig.5 Memory constitution (RAM character 3)

Address	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
280_{16}	0	BS	GS	RS	FR400B	FR400A	FR4009	FR4008	FR4007	FR4006	FR4005	FR4004	FR4003	FR4002	FR4001	FR4000
281_{16} ⋮ 290_{16}	RAM character 4 data															
291_{16}	0	BS	GS	RS	FR411B	FR411A	FR4119	FR4118	FR4117	FR4116	FR4115	FR4114	FR4113	FR4112	FR4111	FR4510
292_{16} ⋮ $29F_{16}$	Can not be used															

Fig.6 Memory constitution (RAM character 4)

Address	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	D00
$2A0_{16}$	0	BS	GS	RS	FR500B	FR500A	FR5009	FR5008	FR5007	FR5006	FR5005	FR5004	FR5003	FR5002	FR5001	FR5000
$2A1_{16}$ ⋮ $2B0_{16}$	RAM character 5 data															
$2B1_{16}$	0	BS	GS	RS	FR511B	FR511A	FR5119	FR5118	FR5117	FR5116	FR5115	FR5114	FR5113	FR5112	FR5111	FR5110
$2B2_{16}$ ⋮ $2BF_{16}$	Can not be used															

Fig.7 Memory constitution (RAM character 5)

Address	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
$2C0_{16}$	0	BS	GS	RS	FR600B	FR600A	FR6009	FR6008	FR6007	FR6006	FR6005	FR6004	FR6003	FR6002	FR6001	FR6000
$2C1_{16}$ ⋮ $2D0_{16}$	RAM character 6 data															
$2D1_{16}$	0	BS	GS	RS	FR611B	FR611A	FR6119	FR6118	FR6117	FR6116	FR6115	FR6114	FR6113	FR6112	FR6111	FR6110
$2D2_{16}$ ⋮ $2DF_{16}$	Can not be used															

Fig.8 Memory constitution (RAM character 6)

Address	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
$2E0_{16}$	0	BS	GS	RS	FR700B	FR700A	FR7009	FR7008	FR7007	FR7006	FR7005	FR7004	FR7003	FR7002	FR7001	FR7000
$2E1_{16}$ ⋮ $2F0_{16}$	RAM character 7 data															
$2F1_{16}$	0	BS	GS	RS	FR711B	FR711A	FR7119	FR7118	FR7117	FR7116	FR7115	FR7114	FR7113	FR7112	FR7111	FR7110

Fig.9 Memory constitution (RAM character 7)

SCREEN CONSTITUTION

The screen lines and rows are determined from each address of the display RAM . The screen constitution is shown in Figure 10.

Row / Line	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	000_{16}	001_{16}	002_{16}	003_{16}	004_{16}	005_{16}	006_{16}	007_{16}	008_{16}	009_{16}	$00A_{16}$	$00B_{16}$	$00C_{16}$	$00D_{16}$	$00E_{16}$	$00F_{16}$	010_{16}	011_{16}	012_{16}	013_{16}	014_{16}	015_{16}	016_{16}	017_{16}
2	018_{16}	019_{16}	$01A_{16}$	$01B_{16}$	$01C_{16}$	$01D_{16}$	$01E_{16}$	$01F_{16}$	020_{16}	021_{16}	022_{16}	023_{16}	024_{16}	025_{16}	026_{16}	027_{16}	028_{16}	029_{16}	$02A_{16}$	$02B_{16}$	$02C_{16}$	$02D_{16}$	$02E_{16}$	$02F_{16}$
3	030_{16}	031_{16}	032_{16}	033_{16}	034_{16}	035_{16}	036_{16}	037_{16}	038_{16}	039_{16}	$03A_{16}$	$03B_{16}$	$03C_{16}$	$03D_{16}$	$03E_{16}$	$03F_{16}$	040_{16}	041_{16}	042_{16}	043_{16}	044_{16}	045_{16}	046_{16}	047_{16}
4	048_{16}	049_{16}	$04A_{16}$	$04B_{16}$	$04C_{16}$	$04D_{16}$	$04E_{16}$	$04F_{16}$	050_{16}	051_{16}	052_{16}	053_{16}	054_{16}	055_{16}	056_{16}	057_{16}	058_{16}	059_{16}	$05A_{16}$	$05B_{16}$	$05C_{16}$	$05D_{16}$	$05E_{16}$	$05F_{16}$
5	060_{16}	061_{16}	062_{16}	063_{16}	064_{16}	065_{16}	066_{16}	067_{16}	068_{16}	069_{16}	$06A_{16}$	$06B_{16}$	$06C_{16}$	$06D_{16}$	$06E_{16}$	$06F_{16}$	070_{16}	071_{16}	072_{16}	073_{16}	074_{16}	075_{16}	076_{16}	077_{16}
6	078_{16}	079_{16}	$07A_{16}$	$07B_{16}$	$07C_{16}$	$07D_{16}$	$07E_{16}$	$07F_{16}$	080_{16}	081_{16}	082_{16}	083_{16}	084_{16}	085_{16}	086_{16}	087_{16}	088_{16}	089_{16}	$08A_{16}$	$08B_{16}$	$08C_{16}$	$08D_{16}$	$08E_{16}$	$08F_{16}$
7	090_{16}	091_{16}	092_{16}	093_{16}	094_{16}	095_{16}	096_{16}	097_{16}	098_{16}	099_{16}	$09A_{16}$	$09B_{16}$	$09C_{16}$	$09D_{16}$	$09E_{16}$	$09F_{16}$	$0A0_{16}$	$0A1_{16}$	$0A2_{16}$	$0A3_{16}$	$0A4_{16}$	$0A5_{16}$	$0A6_{16}$	$0A7_{16}$
8	$0A8_{16}$	$0A9_{16}$	$0AA_{16}$	$0AB_{16}$	$0AC_{16}$	$0AD_{16}$	$0AE_{16}$	$0AF_{16}$	$0B0_{16}$	$0B1_{16}$	$0B2_{16}$	$0B3_{16}$	$0B4_{16}$	$0B5_{16}$	$0B6_{16}$	$0B7_{16}$	$0B8_{16}$	$0B9_{16}$	$0BA_{16}$	$0BB_{16}$	$0BC_{16}$	$0BD_{16}$	$0BE_{16}$	$0BF_{16}$
9	$0C0_{16}$	$0C1_{16}$	$0C2_{16}$	$0C3_{16}$	$0C4_{16}$	$0C5_{16}$	$0C6_{16}$	$0C7_{16}$	$0C8_{16}$	$0C9_{16}$	$0CA_{16}$	$0CB_{16}$	$0CC_{16}$	$0CD_{16}$	$0CE_{16}$	$0CF_{16}$	$0D0_{16}$	$0D1_{16}$	$0D2_{16}$	$0D3_{16}$	$0D4_{16}$	$0D5_{16}$	$0D6_{16}$	$0D7_{16}$
10	$0D8_{16}$	$0D9_{16}$	$0DA_{16}$	$0DB_{16}$	$0DC_{16}$	$0DD_{16}$	$0DE_{16}$	$0DF_{16}$	$0E0_{16}$	$0E1_{16}$	$0E2_{16}$	$0E3_{16}$	$0E4_{16}$	$0E5_{16}$	$0E6_{16}$	$0E7_{16}$	$0E8_{16}$	$0E9_{16}$	$0EA_{16}$	$0EB_{16}$	$0EC_{16}$	$0ED_{16}$	$0EE_{16}$	$0EF_{16}$
11	$0F0_{16}$	$0F1_{16}$	$0F2_{16}$	$0F3_{16}$	$0F4_{16}$	$0F5_{16}$	$0F6_{16}$	$0F7_{16}$	$0F8_{16}$	$0F9_{16}$	$0FA_{16}$	$0FB_{16}$	$0FC_{16}$	$0FD_{16}$	$0FE_{16}$	$0FF_{16}$	100_{16}	101_{16}	102_{16}	103_{16}	104_{16}	105_{16}	106_{16}	107_{16}
12	108_{16}	109_{16}	$10A_{16}$	$10B_{16}$	$10C_{16}$	$10D_{16}$	$10E_{16}$	$10F_{16}$	110_{16}	111_{16}	112_{16}	113_{16}	114_{16}	115_{16}	116_{16}	117_{16}	118_{16}	119_{16}	$11A_{16}$	$11B_{16}$	$11C_{16}$	$11D_{16}$	$11E_{16}$	$11F_{16}$

✻ The hexadecimal numbers in the boxes show the display RAM address.

Fig.10 Screen constitution

RAM Character CONSTITUTION

The dot lines and dot rows of the character RAM are determined from each address and bit of the character RAM . The RAM character constitution is shown in Figure 11.

Dot / Dot	1	2	3	4	5	6	7	8	9	10	11	12
1	FRn00B	FRn00A	FRn009	FRn008	FRn007	FRn006	FRn005	FRn004	FRn003	FRn002	FRn001	FRn000
2	FRn01B	FRn01A	FRn019	FRn018	FRn017	FRn016	FRn015	FRn014	FRn013	FRn012	FRn011	FRn010
3	FRn02B	FRn02A	FRn029	FRn028	FRn027	FRn026	FRn025	FRn024	FRn023	FRn022	FRn021	FRn020
4	FRn03B	FRn03A	FRn039	FRn038	FRn037	FRn036	FRn035	FRn034	FRn033	FRn032	FRn031	FRn030
5	FRn04B	FRn04A	FRn049	FRn048	FRn047	FRn046	FRn045	FRn044	FRn043	FRn042	FRn041	FRn040
6	FRn05B	FRn05A	FRn059	FRn058	FRn057	FRn056	FRn055	FRn054	FRn053	FRn052	FRn051	FRn050
7	FRn06B	FRn06A	FRn069	FRn068	FRn067	FRn066	FRn065	FRn064	FRn063	FRn062	FRn061	FRn060
8	FRn07B	FRn07A	FRn079	FRn078	FRn077	FRn076	FRn075	FRn074	FRn073	FRn072	FRn071	FRn070
9	FRn08B	FRn08A	FRn089	FRn088	FRn087	FRn086	FRn085	FRn084	FRn083	FRn082	FRn081	FRn080
10	FRn09B	FRn09A	FRn099	FRn098	FRn097	FRn096	FRn095	FRn094	FRn093	FRn092	FRn091	FRn090
11	FRn0AB	FRn0AA	FRn0A9	FRn0A8	FRn0A7	FRn0A6	FRn0A5	FRn0A4	FRn0A3	FRn0A2	FRn0A1	FRn0A0
12	FRn0BB	FRn0BA	FRn0B9	FRn0B8	FRn0B7	FRn0B6	FRn0B5	FRn0B4	FRn0B3	FRn0B2	FRn0B1	FRn0B0
13	FRn0CB	FRn0CA	FRn0C9	FRn0C8	FRn0C7	FRn0C6	FRn0C5	FRn0C4	FRn0C3	FRn0C2	FRn0C1	FRn0C0
14	FRn0DB	FRn0DA	FRn0D9	FRn0D8	FRn0D7	FRn0D6	FRn0D5	FRn0D4	FRn0D3	FRn0D2	FRn0D1	FRn0D0
15	FRn0EB	FRn0EA	FRn0E9	FRn0E8	FRn0E7	FRn0E6	FRn0E5	FRn0E4	FRn0E3	FRn0E2	FRn0E1	FRn0E0
16	FRn0FB	FRn0FA	FRn0F9	FRn0F8	FRn0F7	FRn0F6	FRn0F5	FRn0F4	FRn0F3	FRn0F2	FRn0F1	FRn0F0
17	FRn10B	FRn10A	FRn109	FRn108	FRn107	FRn106	FRn105	FRn104	FRn103	FRn102	FRn101	FRn100
18	FRn11B	FRn11A	FRn119	FRn118	FRn117	FRn116	FRn115	FRn114	FRn113	FRn112	FRn111	FRn110

✻ The number in the boxes show the bit address of the RAM character :n. ("n" is RAM number : 0 to 7)

Fig.11 RAM charcter consititution

Note. When the RAM character is used, it is necessary to clear all areas of the RAM character first.

DISPLAY RAM

Address 000_{16} to $11F_{16}$

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>C0</td><td>0
1</td><td rowspan="8">Set the displayed ROM character code.

*RAM character is selected using the 8 bits from C7 to C0.
When C7 to C0=(11111110_2) is set. And, RAM character code is set to R, G and B.

<table><tr><th>B</th><th>G</th><th>R</th><th>RAM character code</th></tr><tr><td>0</td><td>0</td><td>0</td><td>RAM character 0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>RAM character 1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>RAM character 2</td></tr><tr><td>0</td><td>1</td><td>1</td><td>RAM character 3</td></tr><tr><td>1</td><td>0</td><td>0</td><td>RAM character 4</td></tr><tr><td>1</td><td>0</td><td>1</td><td>RAM character 5</td></tr><tr><td>1</td><td>1</td><td>0</td><td>RAM character 6</td></tr><tr><td>1</td><td>1</td><td>1</td><td>RAM character 7</td></tr></table></td><td rowspan="8">Set display character</td></tr>
<tr><td>1</td><td>C1</td><td>0
1</td></tr>
<tr><td>2</td><td>C2</td><td>0
1</td></tr>
<tr><td>3</td><td>C3</td><td>0
1</td></tr>
<tr><td>4</td><td>C4</td><td>0
1</td></tr>
<tr><td>5</td><td>C5</td><td>0
1</td></tr>
<tr><td>6</td><td>C6</td><td>0
1</td></tr>
<tr><td>7</td><td>C7</td><td>0
1</td></tr>
<tr><td>8</td><td>R</td><td>0
1</td><td rowspan="3"><table><tr><th>B</th><th>G</th><th>R</th><th>Color</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr><tr><td>1</td><td>1</td><td>1</td><td>White</td></tr></table></td><td rowspan="3">Set character color (character unit)
* When set C7 to C0= (11111110_2), can be set RAM character code.</td></tr>
<tr><td>9</td><td>G</td><td>0
1</td></tr>
<tr><td>A</td><td>B</td><td>0
1</td></tr>
<tr><td>B</td><td>BLINK</td><td>0</td><td>Do not blink.</td><td rowspan="2">Set blinking
See register BLINK2 to BLINK0 (address129_{16})</td></tr>
<tr><td></td><td></td><td>1</td><td>Blinking</td></tr>
<tr><td>C</td><td>BR</td><td>0
1</td><td rowspan="4"><table><tr><th>BB</th><th>BG</th><th>BR</th><th>Color</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr><tr><td>1</td><td>1</td><td>1</td><td>White</td></tr></table></td><td rowspan="4">Set character background color. (character unit)
*When set C7 to C0=(11111110_2) and register RBLK0 (address124_{16})= “1”, set coloring prohibition color.
Moreover, when the blink is set, the parts other than the color set by this register are blinks.
See DISPLAY FORM 2.</td></tr>
<tr><td>D</td><td>BG</td><td>0
1</td></tr>
<tr><td>E</td><td>BB</td><td>0
1</td></tr>
</table>

Note. The display RAM is undefined state at the $\overline{AC}$ pin.

REGISTERS DESCRIPTION

(1) Address 120_{16}

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>DIV0</td><td>⓪
1</td><td rowspan="11">Set division value (multiply value) of horizontal oscillation frequency.

$N1 = \sum_{n=0}^{10} (DIVn \times 2^n)$

N1 : division value (multiply value)</td><td rowspan="11">Set display frequency by division value (multiply value) setting.
For details, see REGISTER SUPPLEMENTARY DESCRIPTION (1).

Also, set the display frequency range by registers DIVS0, DIVS1, DIVS2, RSEL0 and RSEL1(address 121_{16}) in accordance with the display frequency.

Any of this settings above is required only when EXCK1 = 0, EXCK0 = 1 and EXCK1 = 1, EXCK0 = 1.</td></tr>
<tr><td>1</td><td>DIV1</td><td>⓪
1</td></tr>
<tr><td>2</td><td>DIV2</td><td>⓪
1</td></tr>
<tr><td>3</td><td>DIV3</td><td>⓪
1</td></tr>
<tr><td>4</td><td>DIV4</td><td>⓪
1</td></tr>
<tr><td>5</td><td>DIV5</td><td>⓪
1</td></tr>
<tr><td>6</td><td>DIV6</td><td>⓪
1</td></tr>
<tr><td>7</td><td>DIV7</td><td>⓪
1</td></tr>
<tr><td>8</td><td>DIV8</td><td>⓪
1</td></tr>
<tr><td>9</td><td>DIV9</td><td>⓪
1</td></tr>
<tr><td>A</td><td>DIV10</td><td>⓪
1</td></tr>
<tr><td>B</td><td>TEST10</td><td>⓪</td><td>It should be fixed to "0".</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>C</td><td>SPACE0</td><td>⓪
1</td><td rowspan="3">SPACE 2 1 0 | Number of Lines and Space <(S) represents space>
0 0 0 | 12
0 0 1 | 1 (S) 10 (S) 1
0 1 0 | 2 (S) 8 (S) 2
0 1 1 | 3 (S) 6 (S) 3
1 0 0 | 4 (S) 4 (S) 4
1 0 1 | 5 (S) 2 (S) 5
1 1 0 | 6 (S) 6
1 1 1 | 6 (S)(S) 6
(S) represents one line worth of space</td><td rowspan="3">Leave one line worth of space in the vertical direction.
For example, 6 (S) 6 indicates two sets of 6 lines with a line of spaces between lines 6 and 7.
A line is 18 × N horizontal scan lines.
N is determined by the character size in the vertical direction</td></tr>
<tr><td>D</td><td>SPACE1</td><td>⓪
1</td></tr>
<tr><td>E</td><td>SPACE2</td><td>⓪
1</td></tr>
</table>

Note. The mark ◯ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

(2) Address 121_{16}

DA	Register	Contents		Remarks
		Status	Function	
0	PTC0	⓪	P0 output (port P0).	P0 pin output control.
		1	BLNK0 output.	
1	PTC1	⓪	P1 output (port P1).	P1 pin output control.
		1	R signal output.	
2	PTC2	⓪	P2 output (port P2).	P2 pin output control.
		1	Can not be used.	
3	PTC3	⓪	P3 output (port P3).	P3 pin output control.
		1	G signal output.	
4	PTC4	⓪	P4 output (port P4).	P4 pin output control.
		1	Can not be used.	
5	PTC5	⓪	P5 output (port P5).	P5 pin output control.
		1	B signal output.	
6	PTC6	⓪	P6 output (port P6).	P6 pin output control.
		1	Can not be used.	
7	PTC7	⓪	P7 output (port P7).	P7 pin output control.
		1	Can not be used.	
8	DIVS0	⓪	For setting, see REGISTER SUPPLEMENTARY DESCRIPTION (2).	Set display frequency range.
		1		
9	DIVS1	⓪		
		1		
A	DIVS2	⓪		
		1		
B	RSEL0	⓪		
		1		
C	RSEL1	⓪		
		1		
D	EXCK0	⓪	<table><tr><th>EXCK1</th><th>EXCK0</th><th>Display clock input</th></tr><tr><td>0</td><td>0</td><td>External synchronous (external clock)</td></tr><tr><td>0</td><td>1</td><td>Internal synchronous</td></tr><tr><td>1</td><td>0</td><td>Do not set</td></tr><tr><td>1</td><td>1</td><td>External synchronous (internal clock)</td></tr></table>	Display clock setting See REGISTER SUPPLEMENTARY DESCRIPTION (1)
		1		
E	EXCK1	⓪		
		1		

Note. The mark ◯ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

(3) Address 122_{16}

DA	Register	Contents		Remarks
		Status	Function	
0	PTD0	⓪	"L" output or negative polarity output (BLNK0 output).	P0 pin data control.
		1	"H" output or positive polarity output (BLNK0 output).	
1	PTD1	⓪	"L" output or negative polarity output (R signal output).	P1 pin data control.
		1	"H" output or positive polarity output (R signal output).	
2	PTD2	⓪	"L" output.	P2 pin data control.
		1	"H" output.	
3	PTD3	⓪	"L" output or negative polarity output (G signal output).	P3 pin data control.
		1	"H" output or positive polarity output (G signal output).	
4	PTD4	⓪	"L" output.	P4 pin data control.
		1	"H" output.	
5	PTD5	⓪	"L" output or negative polarity output (B signal output).	P5 pin data control.
		1	"H" output or positive polarity output (B signal output).	
6	PTD6	⓪	"L" output.	P6 pin data control.
		1	"H" output.	
7	PTD7	⓪	"L" output.	P7 pin data control.
		1	"H" output.	
8	TEST11	⓪	Can not be used.	
		1	It should be fixed to "1".	
9	TEST12	⓪	It should be fixed to "0".	
		1	Can not be used.	
A	TEST13	⓪	It should be fixed to "0".	
		1	Can not be used.	
B	TEST14	⓪	It should be fixed to "0".	
		1	Can not be used.	
C	TEST15	⓪	It should be fixed to "0".	
		1	Can not be used.	
D	TEST16	⓪	It should be fixed to "0".	
		1	Can not be used.	
E	TEST17	⓪	It should be fixed to "0".	
		1	Can not be used.	

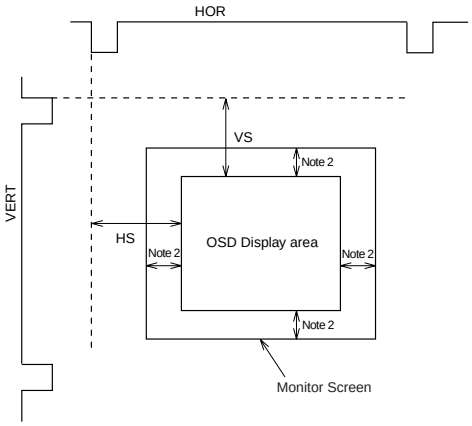
Note. The mark ◯ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

(4) Address 123_{16}

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>HP0</td><td>0</td><td rowspan="11">If HS is the horizontal display start location,
$HS = T \times (\sum_{n=0}^{10} 2^n NP_n + m)$
T: Period of display frequency

2007 settings are possible.

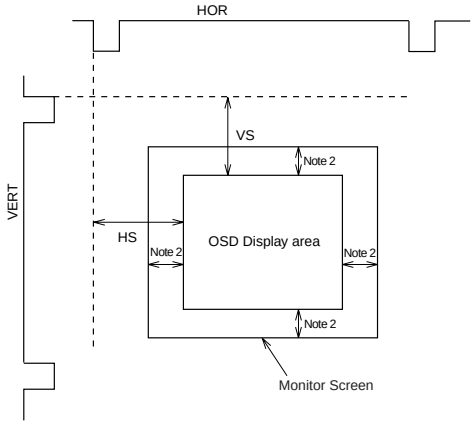
m : offset value differ for the setting of the register EXCK0 and EXCK1. It shown below.

<table><tr><td>EXCK1</td><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><td>EXCK0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>m</td><td>13</td><td>13</td><td>Do not set</td><td>19</td></tr></table>
  </td><td rowspan="11">Horizontal display start location is specified using the 11 bits from HP10 to HP0. HP10 to HP0 = (000000000002) and (000001001112) setting is forbidden.

HS*(shown left) shows horizontal display start location this is register B/$\overline{F}$ (address 12916) = "0" is set.</td></tr>
<tr><td>1</td><td>HP1</td><td>0</td></tr>
<tr><td>2</td><td>HP2</td><td>0</td></tr>
<tr><td>3</td><td>HP3</td><td>0</td></tr>
<tr><td>4</td><td>HP4</td><td>0</td></tr>
<tr><td>5</td><td>HP5</td><td>0</td></tr>
<tr><td>6</td><td>HP6</td><td>0</td></tr>
<tr><td>7</td><td>HP7</td><td>0</td></tr>
<tr><td>8</td><td>HP8</td><td>0</td></tr>
<tr><td>9</td><td>HP9</td><td>0</td></tr>
<tr><td>A</td><td>HP10</td><td>0</td></tr>
<tr><td>B</td><td>TEST0</td><td>0</td><td>It should be fixed to "0".</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>C</td><td>TEST1</td><td>0</td><td>It should be fixed to "0".</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>D</td><td>TEST2</td><td>0</td><td>It should be fixed to "0".</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>E</td><td>TEST3</td><td>0</td><td>It should be fixed to "0".</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
</table>

Notes 1. The mark ○ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.
2. Set up the horizontal and vertical display start location so that display range may not exceed it.
Set the character code "FF_{16}" (blank without background) for the display RAM of the part which the display range exceeds.

(5) Address 124_{16}

DA	Register	Contents		Remarks
		Status	Function	
0	VP0	⓪	If VS is the vertical display start location, $VS = H \times \sum_{n=0}^{10} 2^n VP_n$ T: Cycle with the horizonal synchronizing pulse 2047 settings are possible.  	The vertical start location is specified using the 11 bits from VP10 to VP0. VP10 to VP0 = (00000000000_2) setting is forbidden. HS*(shown left) shows horizontal display start location this is register B/$\overline{F}$ (address 129_{16}) = "0" is set.
		1		
1	VP1	⓪		
		1		
2	VP2	⓪		
		1		
3	VP3	⓪		
		1		
4	VP4	⓪		
		1		
5	VP5	⓪		
		1		
6	VP6	⓪		
		1		
7	VP7	⓪		
		1		
8	VP8	⓪		
		1		
9	VP9	⓪		
		1		
A	VP10	⓪		
		1		
B	TEST18	⓪	It should be fixed to "0".	
		1	Can not be used.	
C	TEST19	⓪	It should be fixed to "0".	
		1	Can not be used.	
D	RBLK0	⓪	Matrix-outline size.	Sets the blanking mode of RAM character. See DISPLAY FORM 2.
		1	Charcter size. (Note 3)	
E	TEST20	⓪	It should be fixed to "0".	
		1	Can not be used.	

Notes 1. The mark ◯ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.
2. Set up the horizontal and vertical display start location so that display range may not exceed it.
Set the character code "FF_{16}" (blank without background) for the display RAM of the part which the display range exceeds.
3. The part of the appointed color by BR, BG and BB of the display RAM changes that the blanking is "OFF".

(6) Address 125_{16}

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>DSP0</td><td>⓪</td><td rowspan="13">The display modes of display screen inside n+1 line by DSPn (n=0 to 11)

The display mode decided by the combination with registers BLK1 and BLK0 (address 129_{16}).
Settings are given below.

<table><tr><th>BLK1</th><th>BLK0</th><th>DSPn="0"</th><th>DSPn="1"</th></tr><tr><td>0</td><td>0</td><td>Matrix-outline border</td><td>Matrix-outline</td></tr><tr><td>0</td><td>1</td><td>Character</td><td>Border</td></tr><tr><td>1</td><td>0</td><td>Border</td><td>Matrix-outline</td></tr><tr><td>1</td><td>1</td><td>Matrix-outline</td><td>Charcter</td></tr></table>(At register BCOL="0")

For detail, see DISPLAY FORM 1 (1).</td><td>Sets the display mode of line 1.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>1</td><td>DSP1</td><td>⓪</td><td>Sets the display mode of line 2.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>2</td><td>DSP2</td><td>⓪</td><td>Sets the display mode of line 3.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>3</td><td>DSP3</td><td>⓪</td><td>Sets the display mode of line 4.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>4</td><td>DSP4</td><td>⓪</td><td>Sets the display mode of line 5.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>5</td><td>DSP5</td><td>⓪</td><td>Sets the display mode of line 6.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>6</td><td>DSP6</td><td>⓪</td><td>Sets the display mode of line 7.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>7</td><td>DSP7</td><td>⓪</td><td>Sets the display mode of line 8.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>8</td><td>DSP8</td><td>⓪</td><td>Sets the display mode of line 9.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>9</td><td>DSP9</td><td>⓪</td><td>Sets the display mode of line 10.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>A</td><td>DSP10</td><td>⓪</td><td>Sets the display mode of line 11.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>B</td><td>DSP11</td><td>⓪</td><td>Sets the display mode of line 12.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>C</td><td>TEST21</td><td>⓪</td><td>It should be fixed to "0".</td><td></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td><td></td></tr>
<tr><td>D</td><td>TEST22</td><td>⓪</td><td>It should be fixed to "0".</td><td></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td><td></td></tr>
<tr><td>E</td><td>TEST23</td><td>⓪</td><td>It should be fixed to "0".</td><td></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td><td></td></tr>
</table>

Note. The mark ◯ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

(7) Address 126_{16}

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td rowspan="2">LIN2</td><td>(0)</td><td rowspan="10">The vertical dot size for line n in the character dot lines (18 vertical lines) is set using LINn (n = 2 to 17).

Dot size can be selected between 2 types for each dot line.

For dot size, see the below registers. Line 1 and lines 2 to 12 can be set independent of one another.

<table><tr><th></th><th>LINn = "0"</th><th>LINn = "1"</th></tr><tr><td>1st line</td><td>Refer to VSZ1L0 and VSZ1L1</td><td>Refer to VSZ1H0 and VSZ1H1</td></tr><tr><td>2nd to 12th line</td><td>Refer to VSZ2L0 and VSZ2L1</td><td>Refer to VSZ2H0 and VSZ2H1</td></tr></table></td><td>Character size setting in the vertical direction for the 2nd line.</td></tr>
<tr><td>1</td><td>1</td><td>Character size setting in the vertical direction for the 3rd line.</td></tr>
<tr><td>2</td><td rowspan="2">LIN3</td><td>(0)</td><td>Character size setting in the vertical direction for the 4th line.</td></tr>
<tr><td>3</td><td>1</td><td>Character size setting in the vertical direction for the 5th line.</td></tr>
<tr><td>4</td><td rowspan="2">LIN4</td><td>(0)</td><td>Character size setting in the vertical direction for the 6th line.</td></tr>
<tr><td>5</td><td>1</td><td>Character size setting in the vertical direction for the 7th line.</td></tr>
<tr><td>6</td><td rowspan="2">LIN5</td><td>(0)</td><td>Character size setting in the vertical direction for the 8th line.</td></tr>
<tr><td>7</td><td>1</td><td>Character size setting in the vertical direction for the 9th line.</td></tr>
<tr><td>8</td><td rowspan="2">LIN6</td><td>(0)</td><td rowspan="2">H: Cycle with the horizontal synchronizing pulse
<table><tr><th>V1SZ1</th><th>V1SZ0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="2">Character size setting in the vertical direction for the 1st line.
(display monitor 1 to 12 line)</td></tr>
<tr><td>9</td><td>1</td></tr>
<tr><td>A</td><td rowspan="2">LIN7</td><td>(0)</td><td rowspan="2">H: Cycle with the horizontal synchronizing pulse
<table><tr><th>VSZ1L1</th><th>VSZ1L0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="2">Character size setting in the vertical direction (display monitor 1 line) at "0" state in register LIN2 to LIN17 (address 126_{16}, 127_{16}).</td></tr>
<tr><td>B</td><td>1</td></tr>
<tr><td>C</td><td rowspan="2">LIN8</td><td>(0)</td><td rowspan="2">H: Cycle with the horizontal synchronizing pulse
<table><tr><th>VSZ1H1</th><th>VSZ1H0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="2">Character size setting in the vertical direction (display monitor 1 line) at "1" state in register LIN2 to LIN17 (address 126_{16}, 127_{16}).</td></tr>
<tr><td>D</td><td>1</td></tr>
<tr><td>E</td><td rowspan="2">TEST24</td><td>(0)</td><td>It should be fixed to "0".</td><td rowspan="2"></td></tr>
<tr><td></td><td>1</td><td>Can not be used.</td></tr>
</table>

Note. The mark ◯ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

(8) Address 127_{16}

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>LIN10</td><td>⓪</td><td rowspan="14">The vertical dot size for line n in the character dot lines (18 vertical lines) is set using LINn (n = 2 to 17).

Dot size can be selected between 2 types for each dot line.

For dot size, see the below registers. Line 1 and lines 2 to 12 can be set independent of one another.

<table><tr><th></th><th>LINn = "0"</th><th>LINn = "1"</th></tr><tr><td>1st line</td><td>Refer to VSZ1L0 and VSZ1L1</td><td>Refer to VSZ1H0 and VSZ1H1</td></tr><tr><td>2nd to 12th line</td><td>Refer to VSZ2L0 and VSZ2L1</td><td>Refer to VSZ2H0 and VSZ2H1</td></tr></table></td><td>Character size setting in the vertical direction for the 10th line.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>1</td><td>LIN11</td><td>⓪</td><td>Character size setting in the vertical direction for the 11th line.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>2</td><td>LIN12</td><td>⓪</td><td>Character size setting in the vertical direction for the 12th line.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>3</td><td>LIN13</td><td>⓪</td><td>Character size setting in the vertical direction for the 13th line.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>4</td><td>LIN14</td><td>⓪</td><td>Character size setting in the vertical direction for the 14th line.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>5</td><td>LIN15</td><td>⓪</td><td>Character size setting in the vertical direction for the 15th line.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>6</td><td>LIN16</td><td>⓪</td><td>Character size setting in the vertical direction for the 16th line.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>7</td><td>LIN17</td><td>⓪</td><td>Character size setting in the vertical direction for the 17th line.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>8</td><td>V18SZ0</td><td>⓪</td><td rowspan="2">H: Cycle with the horizontal synchronizing pulse
<table><tr><th>V18SZ1</th><th>V18SZ0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="2">Character size setting in the vertical direction for the 18th line.
(display monitor 1 to 12 line)</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>9</td><td>V18SZ1</td><td>⓪</td><td rowspan="2">Character size setting in the vertical direction for the 19th line.
(display monitor 1 to 12 line)</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>A</td><td>VSZ2L0</td><td>⓪</td><td rowspan="2">H: Cycle with the horizontal synchronizing pulse
<table><tr><th>VSZ2L1</th><th>VSZ2L0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="2">Character size setting in the vertical direction (display monitor for 2 to 12 line) at "0" state in register LIN2 to LIN17 (address 126_{16}, 127_{16}).</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>B</td><td>VSZ2L1</td><td>⓪</td><td rowspan="2">Character size setting in the vertical direction (display monitor for 2 to 12 line) at "0" state in register LIN2 to LIN17 (address 126_{16}, 127_{16}).</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>C</td><td>VSZ2H0</td><td>⓪</td><td rowspan="2">H: Cycle with the horizontal synchronizing pulse
<table><tr><th>VSZ2H1</th><th>VSZ2H0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>1</td><td>1</td><td>2H/dot</td></tr><tr><td>0</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="2">Character size setting in the vertical direction (display monitor for 2 to12 line) at "1" state in register LIN2 to LIN17(address 126_{16}, 127_{16}).</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>D</td><td>VSZ2H1</td><td>⓪</td><td rowspan="2">Character size setting in the vertical direction (display monitor for 2 to12 line) at "1" state in register LIN2 to LIN17(address 126_{16}, 127_{16}).</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>E</td><td>TEST25</td><td>⓪</td><td>It should be fixed to "0".</td><td></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td><td></td></tr>
</table>

Note. The mark ◯ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

(9) Address 128_{16}

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">RR</td><td>0</td><td rowspan="9"><table><tr><th>RB</th><th>RG</th><th>RR</th><th>Color</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr><tr><td>1</td><td>1</td><td>1</td><td>White</td></tr></table></td><td rowspan="9">Sets the raster color of all blankings.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">RG</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">RB</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">FR</td><td>0</td><td rowspan="9"><table><tr><th>FB</th><th>FG</th><th>FR</th><th>Color</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr><tr><td>1</td><td>1</td><td>1</td><td>White</td></tr></table></td><td rowspan="9">Set the blanking color of the Border size, or the shadow size.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">FG</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">FB</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">TEST26</td><td>0</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">TEST27</td><td>0</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">8</td><td rowspan="2">TEST28</td><td>0</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">9</td><td rowspan="2">BETA14</td><td>0</td><td>Matrix-outline display (12 × 18 dot)</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Matrix-outline display (14 × 18 dot)</td></tr>
<tr><td rowspan="2">A</td><td rowspan="2">HSZ10</td><td>0</td><td rowspan="3"><table><tr><th>HSZ10</th><th>Horizontal direction size</th></tr><tr><td>0</td><td>1T/dot</td></tr><tr><td>1</td><td>2T/dot</td></tr></table></td><td rowspan="3">Charcter size setting in the horizontal direction for the first line.
T: Display frequency cycle</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">B</td><td rowspan="2">TEST31</td><td>0</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">C</td><td rowspan="2">HSZ20</td><td>0</td><td rowspan="3"><table><tr><th>HSZ20</th><th>Horizontal direction size</th></tr><tr><td>0</td><td>1T/dot</td></tr><tr><td>1</td><td>2T/dot</td></tr></table></td><td rowspan="3">Charcter size setting in the horizontal direction for the 2nd line to 12th line.
T: Display frequency cycle</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">D</td><td rowspan="2">TEST32</td><td>0</td><td>It should be fixed to "0".</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td rowspan="2">E</td><td rowspan="2">TEST29</td><td>0</td><td>It should be fixed to "0".</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
</table>

Note. The mark ◯ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

(10) Address 129_{16}

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">BCOL</td><td>(0)</td><td>Blanking of BLK0, BLK1</td><td rowspan="2">Sets all raster blanking</td></tr>
<tr><td>1</td><td>All raster blanking</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">B/$\overline{F}$</td><td>(0)</td><td>Synchronize with the leading edge of horizontal synchronization.</td><td rowspan="2">Synchronize with the front porch or back porch of the horizontal synchronization signal.</td></tr>
<tr><td>1</td><td>Synchronize with the trailing edge of horizontal synchronization.</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">VMASK</td><td>(0)</td><td>Do not mask by VERT input signal</td><td rowspan="2">Set mask at phase comparison operating.</td></tr>
<tr><td>1</td><td>Mask by VERT input signal</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">POLV</td><td>(0)</td><td>VERT pin is negative polarity</td><td rowspan="2">Set VERT pin polarity.</td></tr>
<tr><td>1</td><td>VERT pin is positive polarity</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">POLH</td><td>(0)</td><td>HOR pin is negative polarity</td><td rowspan="2">Set HOR pin polarity.</td></tr>
<tr><td>1</td><td>HOR pin is positive polarity</td></tr>
<tr><td rowspan="4">5</td><td rowspan="4">BLK0</td><td>(0)</td><td rowspan="4"><table><tr><th>BLK1</th><th>BLK0</th><th>Blanking mode</th></tr><tr><td>0</td><td>0</td><td>Matrix-outline size</td></tr><tr><td>0</td><td>1</td><td>Character size</td></tr><tr><td>1</td><td>0</td><td>Border size</td></tr><tr><td>1</td><td>1</td><td>Matrix-outline size</td></tr></table></td><td rowspan="4">Set blanking mode.
See DISPLAY FORM 1 (1).</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">BLK1</td><td>(0)</td></tr>
<tr><td>1</td><td>(When DSPn (address 125_{16}) = "0")</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">SYAD</td><td>(0)</td><td>Border display of character</td><td rowspan="2">See DISPLAY FORM 1 (2).</td></tr>
<tr><td>1</td><td>Shadow display of character</td></tr>
<tr><td rowspan="2">8</td><td rowspan="2">RAMERS</td><td>(0)</td><td>RAM not erased</td><td rowspan="2">When register RAMERS is set to "1", do not stop the display clock. There is no need to reset because there is no register for this bit.</td></tr>
<tr><td>1</td><td>RAM erased</td></tr>
<tr><td rowspan="2">9</td><td rowspan="2">STOP</td><td>(0)</td><td>Oscillation of clock for display</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Stop the oscillation of clock for display</td></tr>
<tr><td rowspan="2">A</td><td rowspan="2">DSPON</td><td>(0)</td><td>Display OFF</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Display ON</td></tr>
<tr><td rowspan="4">B</td><td rowspan="4">BLINK0</td><td>(0)</td><td rowspan="4"><table><tr><th>BLINK1</th><th>BLINK0</th><th>Duty</th></tr><tr><td>0</td><td>0</td><td>Blinking OFF</td></tr><tr><td>0</td><td>1</td><td>25%</td></tr><tr><td>1</td><td>0</td><td>50%</td></tr><tr><td>1</td><td>1</td><td>75%</td></tr></table></td><td rowspan="4">Set blinking duty ratio.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">C</td><td rowspan="2">BLINK1</td><td>(0)</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">D</td><td rowspan="2">BLINK2</td><td>(0)</td><td>Divided into 64 of vertical synchronous signal</td><td rowspan="2">Set blinking frequency.</td></tr>
<tr><td>1</td><td>Divided into 32 of vertical synchronous signal</td></tr>
<tr><td rowspan="2">E</td><td rowspan="2">TEST30</td><td>(0)</td><td>It should be fixed to "0".</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
</table>

Note. The mark ◯ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

REGISTER SUPPLEMENTARY DESCRIPTION

(1) Setting external clock input and display frequency mode

Setting external clock input and display frequency mode (by use of EXCK0, EXCK1 (121_{16}), and DIV10 to DIV0 (120_{16}) as explained here following.

(a) When (EXCK1, EXCK0) = (0, 0) .....External clock mode 1

Fosc = 6.3 to 80 MHz (V_{DD} = 4.75 to 5.25 V)

Fosc = 6.3 to 40 MHz (V_{DD} = 2.50 to 3.50 V)

Input from the TCK pin a constant-period continuous external clock that synchronizes with the horizontal synchronous signal. And input from HOR pin a constant period continuous horizontal synchronous signal.

Never stop inputting the clock while displaying.

Do not have to set a display frequency because the clock just as it is entered from outside is used as the display clock.

(b) When (EXCK1, EXCK0) = (0, 1) .....Internal clock mode

Fosc = 20 to 110 MHz (V_{DD} = 4.75 to 5.25 V)

Clock input from the TCK pin is unnecessary. The multiply clock of the internally generated horizontal synchronous signal is used as the display clock.

The display frequency is set by setting the multiply value of the horizontal synchronous frequency (of the display frequency) in DIV10 to DIV0 (address 120_{16}). Also, set the display frequency range. (See the next page.)

Display frequency is calculated using the below expression.

Display frequency = Horizontal synchronous frequency x Multiply value

(c) When (EXCK1, EXCK0) = (1, 0) ..... Setting disabled

(d) When (EXCK1, EXCK0) = (1, 1) .....External clock mode 2

Fosc = 20 to 110 MHz (V_{DD} = 4.75 to 5.25 V)

Input from the TCK pin a constant-period continuous external clock that synchronizes with the horizontal synchronous signal. And input from HOR pin a constant-period continuous horizontal synchronous signal.

Never stop inputting the clock while displaying.

An internal clock which is in sync with the external input clock is used as the display clock.

Because the display frequency equals the external clock frequency, set N1 (division value) that satisfies the below expressions to DIV10 to DIV0 (address 120_{16}) for make the display frequency is equal to the external clock frequency.

N1 = external clock frequency / horizontal synchronous frequency

$$N1 = \sum_{n=0}^{10} 2^n DIV_n$$

Also, set the display frequency range. (See the next page.)

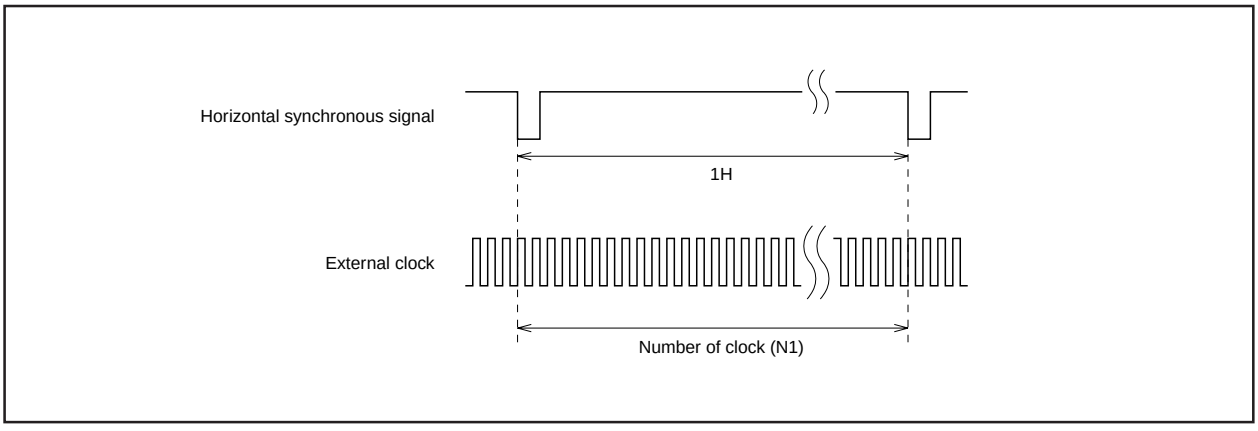


Fig. 12 Example of external clock input

(2) To set display frequency range

Whenever setting display frequency (when EXCK1 = "0", EXCK0 = "1", or EXCK1 = "1", EXCK0 = "1"), always set the display frequency range in accordance with the display frequency. This range is set from DIVS0, DIVS1, DIVS2, RSEL0 and RSEL1 (address 121_{16}). Frequency ranges are given here below.

RSEL1	RSEL0	DIVS2	DIVS1	DIVS0	Display frequency range MHz
1	1	0	0	0	100.0 to 110.0
1	0	0	0	0	–
0	1	0	0	0	92.0 to 100.0
0	0	0	0	0	73.0 to 92.0
1	1	0	0	1	66.5 to 73.0
1	0	0	0	1	–
0	1	0	0	1	61.0 to 66.5
0	0	0	0	1	49.0 to 61.0
1	1	0	1	0	–
1	0	0	1	0	–
0	1	0	1	0	45.5 to 49.0
0	0	0	1	0	36.5 to 45.5
1	1	0	1	1	33.5 to 36.5
1	0	0	1	1	–
0	1	0	1	1	30.5 to 33.5
0	0	0	1	1	24.5 to 30.5
1	1	1	0	0	–
1	0	1	0	0	–
0	1	1	0	0	23.0 to 24.5
0	0	1	0	0	20.0 to 23.0

(3) Notes on setting display frequency

To change external clock (display) frequency or horizontal synchronization frequency, always use the following procedures.

To set EXCK1 = "0", EXCK0 = "1"

(a) Turn the display OFF. … DSPON (address 129_{16}) = "0"
(b) Set the display frequency. … Set from DIV10 to DIV0(address 120_{16}) , DIVS0, DIVS1, DIVS2, RSEL0 and RSEL1 (address 121_{16}).
(c) Wait 20 ms while the horizontal synchronization signal is being input.
(d) Turn the display ON. … DSPON (address 129_{16}) = "1"

To set EXCK1 = "1", EXCK0 = "1"

(a) Turn the display OFF. … DSPON (address 129_{16}) = "0"
(b) Set the display frequency. … Set from DIV10 to DIV0(address 120_{16}) , DIVS0, DIVS1, DIVS2, RSEL0 and RSEL1 (address 121_{16}).
(c) Wait 20 ms while the horizontal synchronization signal and external clock are being input.
(d) Turn the display ON. … DSPON (address 129_{16}) = "1"

DISPLAY FORM 1

M35075-XXXFP has the following four display forms.

(1) ROM character blanking mode

Character size

: Blanking same as the character size.

Border size

: Blanking the background as a size from character.

Matrix-outline size

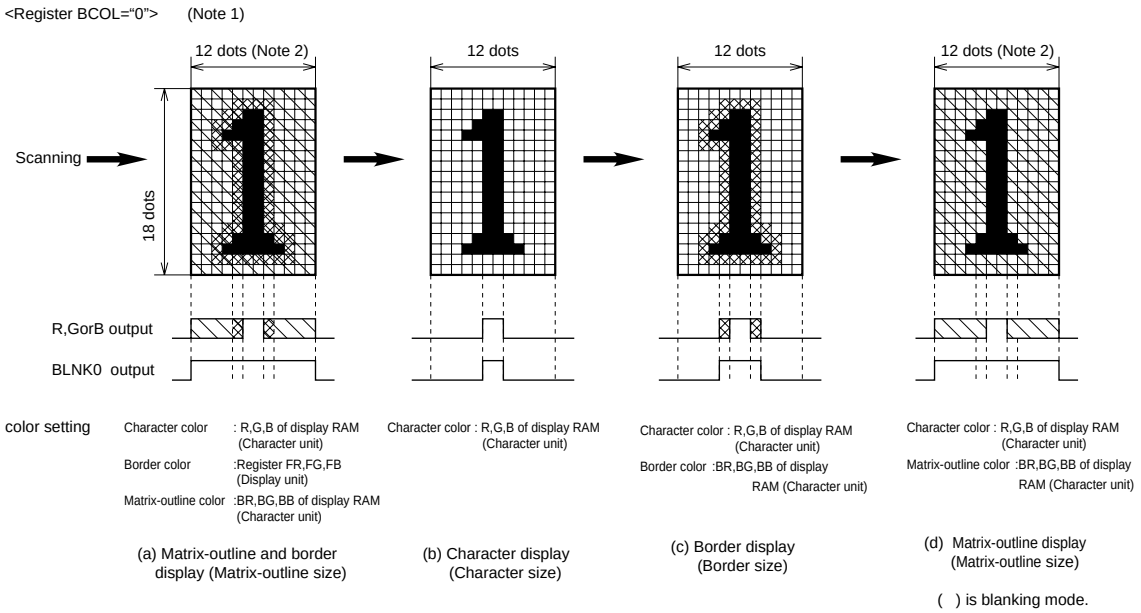
: Blanking the background 12 × 18 dot.

All blanking size

: When set register BCOL to "1", all raster area is blanking.

The display mode and blanking mode can be set line-by-line, as follows, from registers BCOL, BLK1, BLK0 (address 129_{16}), DSP0 to DSP11 (address 125_{16}).

BCOL	BLK1	BLK0	Line of DSPn = "0"		Line of DSPn = "1"	
			Display mode	Blanking mode	Display mode	Blanking mode
0	0	0	Matrix-outline border display	Matrix-outline size	Matrix-outline display	Matrix-outline size
	0	1	Character display	Character size	Border display	Border size
	1	0	Border display	Border size	Matrix-outline display	Matrix-outlinesize
	1	1	Matrix-outline display	Matrix-outline size	Character display	Character size
1	0	0	Matrix-outline border display	All blanking size	Matrix-outline display	All blanking size
	0	1	Character display		Border display	
	1	0	Border display		Matrix-outline display	
	1	1	Matrix-outline display		Character display	



Note 1. When register BCOL is set to "1", the raster range of the display modes set respectively by BLK1 and BLK0 are colored by registers RR, RG, and RB (address 128_{16}). And the blanking mode is set all blanking size (all raster size) regardless of the BLK1 and BLK0 settings.

Note 2. The horizontal size of the full matrix-outline size can be set to 14 dots by register BETA14 (address 128_{16}). BLNK0 can also be output at 14 dots.

Fig. 13 Display form

(2) Shadow display

When border display mode, if set SYAD (address 129_{16}) = "0" to "1", it change to shadow display mode.

Border and shadow display are shown below.

Set shadow display color by BR, BG and BB of display RAM or by register FR, FG and FB.

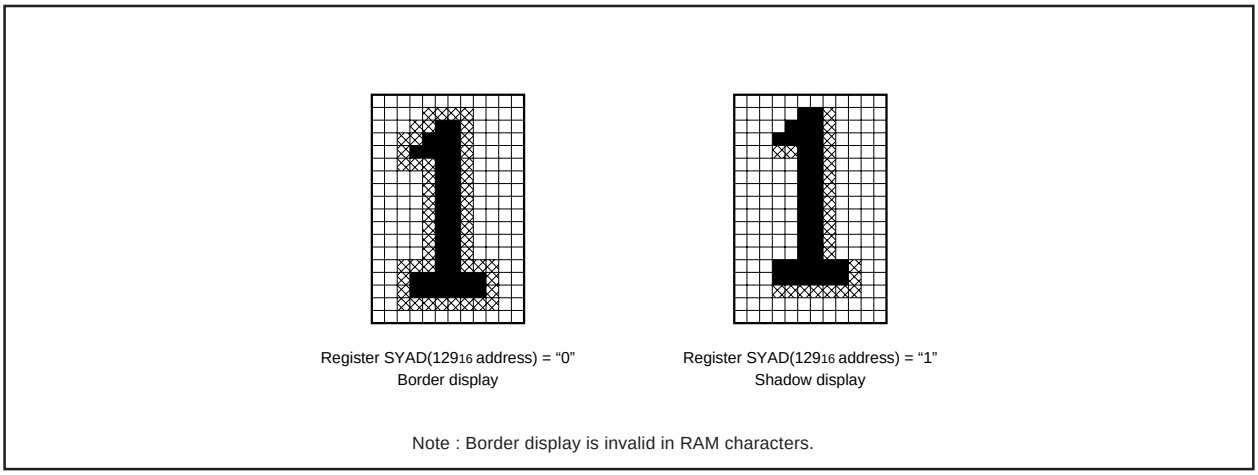


Fig.14 Border and shadow display

DISPLAY FORM 2

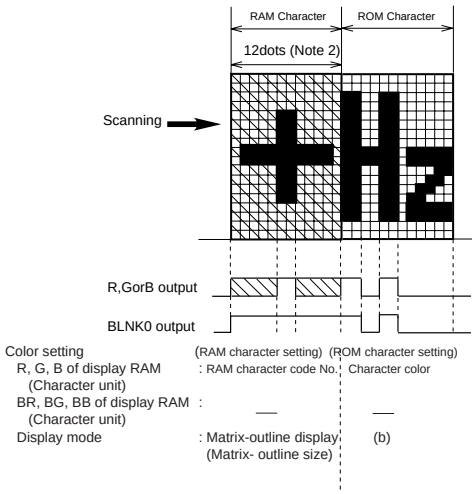
This IC can display both ROM character and RAM character at the same time. The display form is shown in Figure 15 and 16.

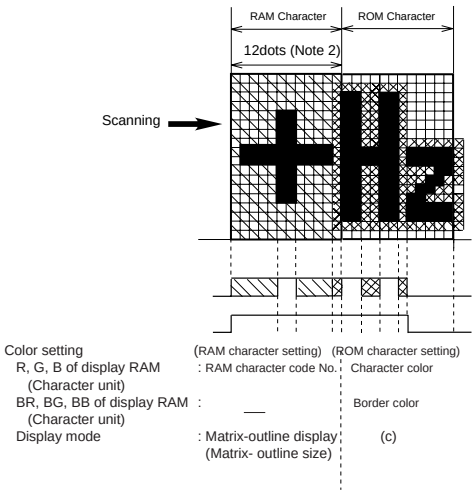
(1) RAM character blanking mode

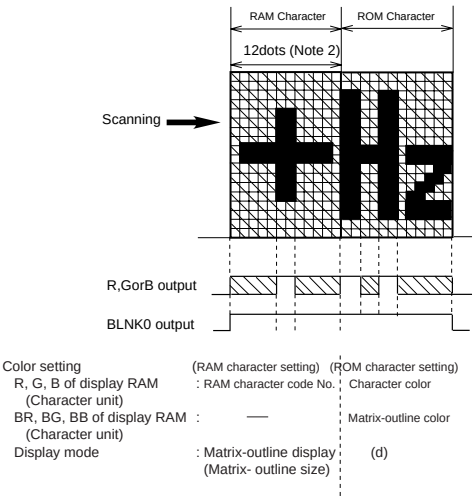
BCOL	RBLK0	Display mode	Blanking mode
0	0	Matrix-outline display	Matrix-outline size
	1	Character display (Note1)	Character size (Note2)
1	0	Matrix-outline display	All blanking size
	1	Character display (Note1)	All blanking size

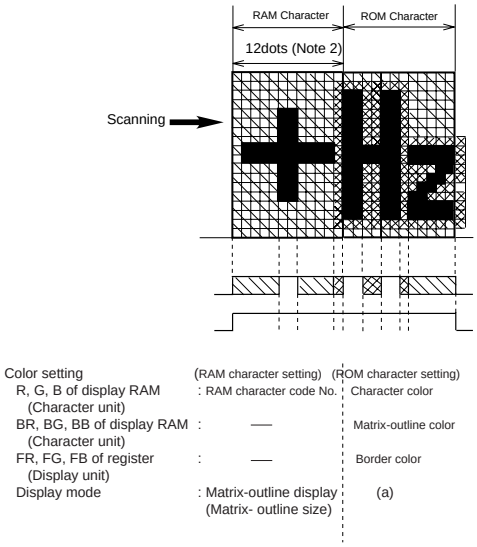
Note1: The part of the appointed color by BR, BG and BB of the display RAM changes that is not coloring.
Note2: The part of the appointed color by BR, BG and BB of the display RAM changes that the blanking is "OFF"

< Regiser BCOL = “0”, RBLK0 = “0”> (Note 1)







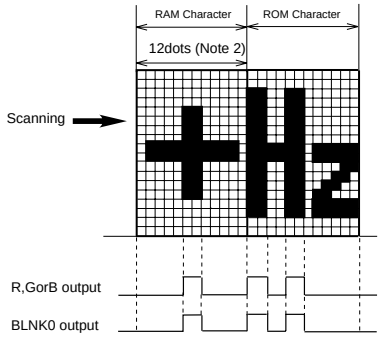


( ) is blanking mode.
Refer to DISPLAY FORM 1 about (a)-(d).

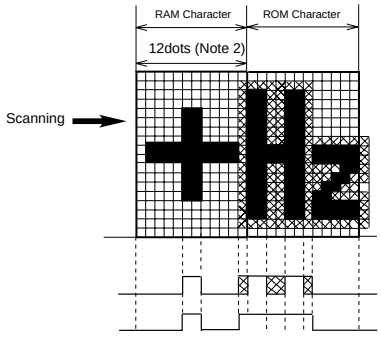
Fig.15 Display form1

Continue to Next

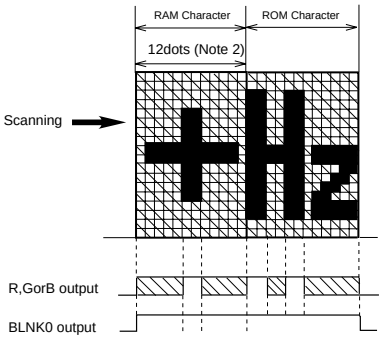
< Register BCOL = “0”, RBLK0 = “1”> (Note 1)



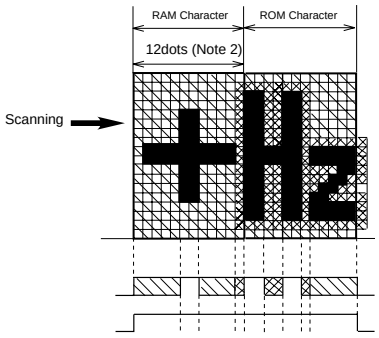
Color setting	(RAM character setting)	(ROM character setting)
R, G, B of display RAM (Character unit)	: RAM character code No.	Character color
BR, BG, BB of display RAM (Character unit)	: Coloring prohibition color	—
Display mode	: Character display (Character size)	(b)



Color setting	(RAM character setting)	(ROM character setting)
R, G, B of display RAM (Character unit)	: RAM character code No.	Character color
BR, BG, BB of display RAM (Character unit)	: Coloring prohibition color	Border color
Display mode	: Character display (Character size)	(c)



Color setting	(RAM character setting)	(ROM character setting)
R, G, B of display RAM (Character unit)	: RAM character code No.	Character color
BR, BG, BB of display RAM (Character unit)	: — (Note 3)	Matrix-outline color
Display mode	: Matrix-outline display (Matrix-outline size) (Note 3)	(d)



Color setting	(RAM character setting)	(ROM character setting)
R, G, B of display RAM (Character unit)	: RAM character code No.	Character color
BR, BG, BB of display RAM (Character unit)	: — (Note 3)	Matrix-outline color
FR, FG, FB of register (Display unit)	: —	Border color
Display mode	: Matrix-outline display (Matrix-outline size) (Note 3)	(a)

( ) is blanking mode.
Refer to DISPLAY FORM 1 about (a)-(d).

Note 1 : When register BCOL = "1", the raster range of the display modes set respectively by RBLK0 is colored by register RR, RG and RB (address 128_{16}) . And the blanking mode is set all blanking size (all raster size) independent of the RBLK0 settings.
Note 2 : The horizontal size of the full matrix-outline size can be set to 14 dots by register BETA14 (address 128_{16}). BLNK0 can also be output at 14 dots.
Note 3 : When display mode (setting by register BLK1, BLK0, DSPn) is Matrix-outline display or Matrix-outline border display, register RBLK0= "1" setting (coloring prohibition color setting) is invalid.

Fig. 16 Display form2

Example of setting RAM character data

For example : RAM character 0

Example of setting the RED bit code data

Address	DAF	DAE (BS)	DAD (GS)	DAC (RS)	DAB (1)	DAA (2)	DA9 (3)	DA8 (4)	DA7 (5)	DA6 (6)	DA5 (7)	DA4 (8)	DA3 (9)	DA2 (10)	DA1 (11)	DA0 (12)
(1)200$_{16}$	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
(2)201$_{16}$	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
(3)202$_{16}$	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
(4)203$_{16}$	0	0	0	1	0	0	1	1	1	1	1	1	1	1	0	0
(5)204$_{16}$	0	0	0	1	0	0	1	1	1	1	1	1	1	1	0	0
(6)205$_{16}$	0	0	0	1	0	0	1	1	1	1	1	1	1	1	0	0
(7)206$_{16}$	0	0	0	1	0	0	1	1	1	1	1	1	1	1	0	0
(8)207$_{16}$	0	0	0	1	0	0	1	1	1	1	1	1	1	1	0	0
(9)208$_{16}$	0	0	0	1	0	0	1	1	1	1	1	1	1	1	0	0
(10)209$_{16}$	0	0	0	1	0	0	1	1	1	1	1	1	1	1	0	0
(11)20A$_{16}$	0	0	0	1	0	0	1	1	1	1	1	1	1	1	0	0
(12)20B$_{16}$	0	0	0	1	0	0	1	1	1	1	1	1	1	1	0	0
(13)20C$_{16}$	0	0	0	1	0	0	1	1	1	1	1	1	1	1	0	0
(14)20D$_{16}$	0	0	0	1	0	0	1	1	1	1	1	1	1	1	0	0
(15)20E$_{16}$	0	0	0	1	0	0	1	1	1	1	1	1	1	1	0	0
(16)20F$_{16}$	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
(17)210$_{16}$	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
(18)211$_{16}$	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
212$_{16}$ ⋮ 21F$_{16}$	Can not used															

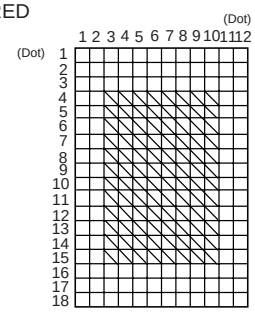
Example of setting the GREEN bit code data

Address	DAF	DAE (BS)	DAD (GS)	DAC (RS)	DAB (1)	DAA (2)	DA9 (3)	DA8 (4)	DA7 (5)	DA6 (6)	DA5 (7)	DA4 (8)	DA3 (9)	DA2 (10)	DA1 (11)	DA0 (12)
(1)200$_{16}$	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
(2)201$_{16}$	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
(3)202$_{16}$	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	0
(4)203$_{16}$	0	0	1	0	0	1	0	0	0	0	0	0	0	0	1	0
(5)204$_{16}$	0	0	1	0	0	1	0	0	1	1	1	1	0	0	1	0
(6)205$_{16}$	0	0	1	0	0	1	0	1	0	0	0	0	1	0	1	0
(7)206$_{16}$	0	0	1	0	0	1	0	1	0	0	0	0	1	0	1	0
(8)207$_{16}$	0	0	1	0	0	1	0	1	0	0	0	0	0	0	1	0
(9)208$_{16}$	0	0	1	0	0	1	0	1	0	0	1	1	1	0	1	0
(10)209$_{16}$	0	0	1	0	0	1	0	1	0	0	0	0	1	0	1	0
(11)20A$_{16}$	0	0	1	0	0	1	0	1	0	0	0	0	1	0	1	0
(12)20B$_{16}$	0	0	1	0	0	1	0	1	0	0	0	1	1	0	1	0
(13)20C$_{16}$	0	0	1	0	0	1	0	0	1	1	1	0	1	0	1	0
(14)20D$_{16}$	0	0	1	0	0	1	0	0	0	0	0	0	0	0	1	0
(15)20E$_{16}$	0	0	1	0	0	1	0	0	0	0	0	0	0	0	1	0
(16)20F$_{16}$	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	0
(17)210$_{16}$	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
(18)211$_{16}$	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
212$_{16}$ ⋮ 21F$_{16}$	Can not used															

Example of setting the GREEN bit code data

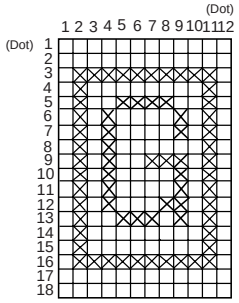
Address	DAF	DAE (BS)	DAD (GS)	DAC (RS)	DAB (1)	DAA (2)	DA9 (3)	DA8 (4)	DA7 (5)	DA6 (6)	DA5 (7)	DA4 (8)	DA3 (9)	DA2 (10)	DA1 (11)	DA0 (12)
(1)200$_{16}$	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1
(2)201$_{16}$	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1
(3)202$_{16}$	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1
(4)203$_{16}$	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1
(5)204$_{16}$	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1
(6)205$_{16}$	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1
(7)206$_{16}$	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1
(8)207$_{16}$	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1
(9)208$_{16}$	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1
(10)209$_{16}$	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1
(11)20A$_{16}$	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1
(12)20B$_{16}$	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1
(13)20C$_{16}$	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1
(14)20D$_{16}$	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1
(15)20E$_{16}$	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1
(16)20F$_{16}$	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1
(17)210$_{16}$	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1
(18)211$_{16}$	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1
212$_{16}$ ⋮ 21F$_{16}$	Can not used															

RED

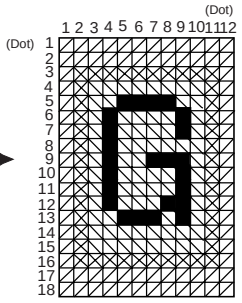


+

GREEN

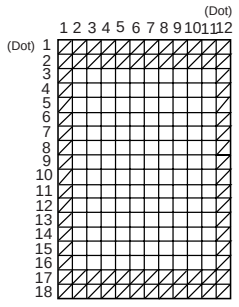


(R+G+B display image)



+

BLUE



Note 1 : After clearing or setting all character RAM areas, and use the RAM characters.

Note 2 : The RAM character's dots are set RED, GREEN and BLUE data, which are controlled by BS, GS and RS bit. (Can be set at same time)

Fig.17 Setting of the data of RAM character

CHARACTER FONT

Images are composed on a 12 × 18 dot matrix, and characters can be linked vertically and horizontally with other characters to allow the display the continuous symbols.
Character code FF_{16} is fixed as a blank without background. Therefore, cannot register a character font in this code.

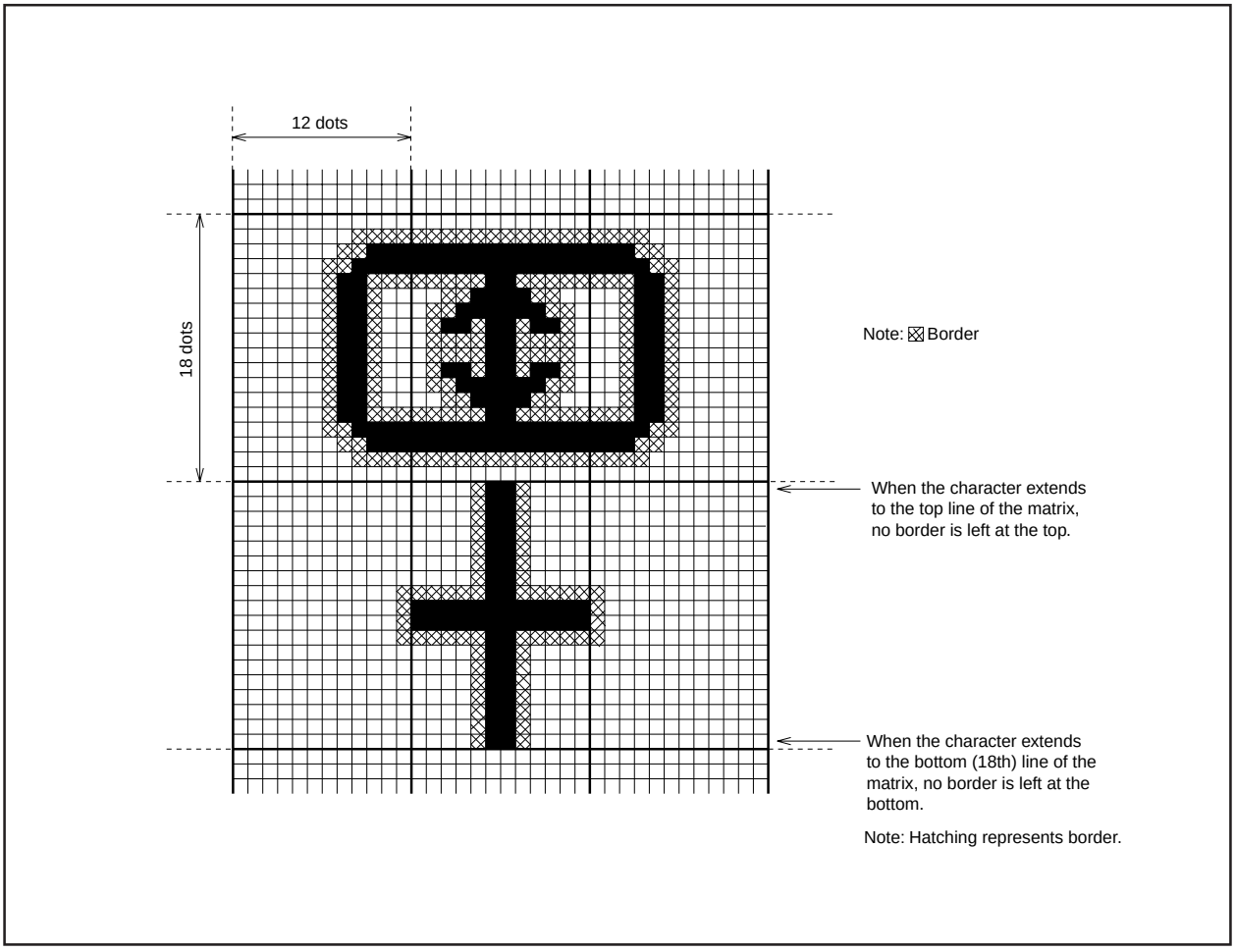


Fig.18 Example of border display

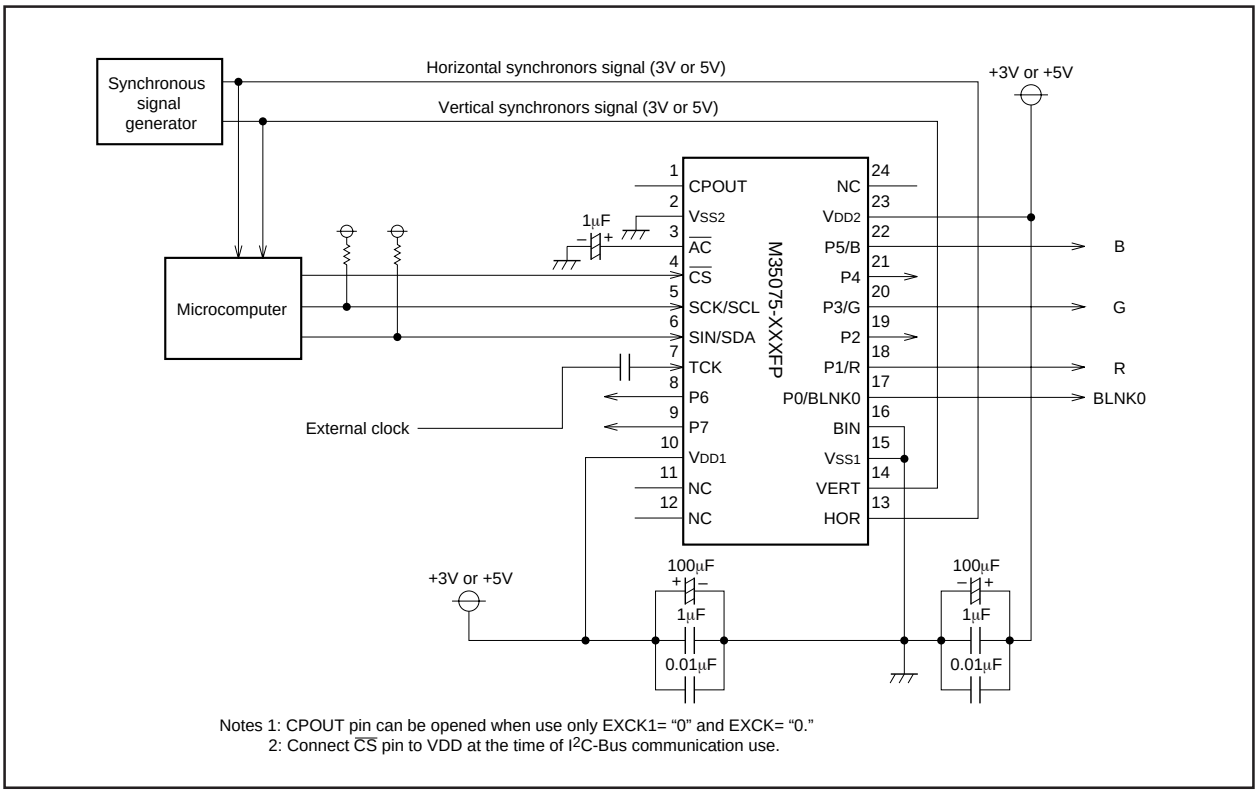
DATA INPUT EXAMPLE

Data of display RAM and display control registers can be set by the I²C-BUS serial input function. Example of data setting is shown in Figure 19 (at EXCK0 = "1", EXCK1 = "0" setting).

Address/data	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	Remarks
	200 m sec hold																System set up (Note 3)
Address 120₁₆	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	Address setting
Data 120₁₆	0	0	0	0	0	DIV10	DIV9	DIV8	DIV7	DIV6	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0	Frequency value setting
Data 121₁₆	0	0	1	RSEL1	RSEL0	DIVS2	DIVS1	DIVS0	1	1	1	0	1	0	1	1	Frequency range setting
Data 122₁₆	0	0	0	0	0	0	0	1	1	1	1	0	1	0	1	1	Output setting
Data 123₁₆	0	0	0	0	0	HP10	HP9	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	Horizontal display location setting
Data 124₁₆	0	0	0	0	0	VP10	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	Vertical display location setting
Data 125₁₆	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Display form setting
Data 126₁₆	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Character size setting
Data 127₁₆	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Character size setting
Data 128₁₆	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Color, character size setting
Data 129₁₆	0	0	0	0	0	0	0	0	0	0	0	POLH	POLV	0	0	0	Display OFF
	20 m sec hold																Be stable/Waiting time
Address 200₁₆	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	Address setting
Data 200₁₆	0	0	0	1	FR000B	FR000A	FR0009	FR0008	FR0007	FR0006	FR0005	FR0004	FR0003	FR0002	FR0001	FR0000	RED•bit code setting
⋮	⋮	Bit color			Bit code/RED												
Data 2F1₁₆	0	0	0	1	FR711B	FR711A	FR7119	FR7118	FR7117	FR7116	FR7115	FR7114	FR7113	FR7112	FR7111	FR7110	
Address 200₁₆	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	Address setting
Data 200₁₆	0	0	1	0	FR000B	FR000A	FR0009	FR0008	FR0007	FR0006	FR0005	FR0004	FR0003	FR0002	FR0001	FR0000	GREEN•bit code setting
⋮	⋮	Bit color			Bit code/GREEN												
Data 2F1₁₆	0	0	1	0	FR711B	FR711A	FR7119	FR7118	FR7117	FR7116	FR7115	FR7114	FR7113	FR7112	FR7111	FR7110	
Address 200₁₆	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	Address setting
Data 200₁₆	0	1	0	0	FR000B	FR000A	FR0009	FR0008	FR0007	FR0006	FR0005	FR0004	FR0003	FR0002	FR0001	FR0000	BLUE•bit code setting
⋮	⋮	Bit color			Bit code/BLUE												
Data 2F1₁₆	0	1	0	0	FR711B	FR711A	FR7119	FR7118	FR7117	FR7116	FR7115	FR7114	FR7113	FR7112	FR7111	FR7110	
Address000₁₆	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Address setting
Data 000₁₆	0	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0	Character setting
⋮	⋮	Background coloring			Blink-ing	Character color			Character code								
Data 11F₁₆	0	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0	
Address 129₁₆	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	1	Address setting
Data 129₁₆	0	0	0	0	0	1	0	0	0	1	1	POLH	POLV	0	0	0	Display ON (Note 2)

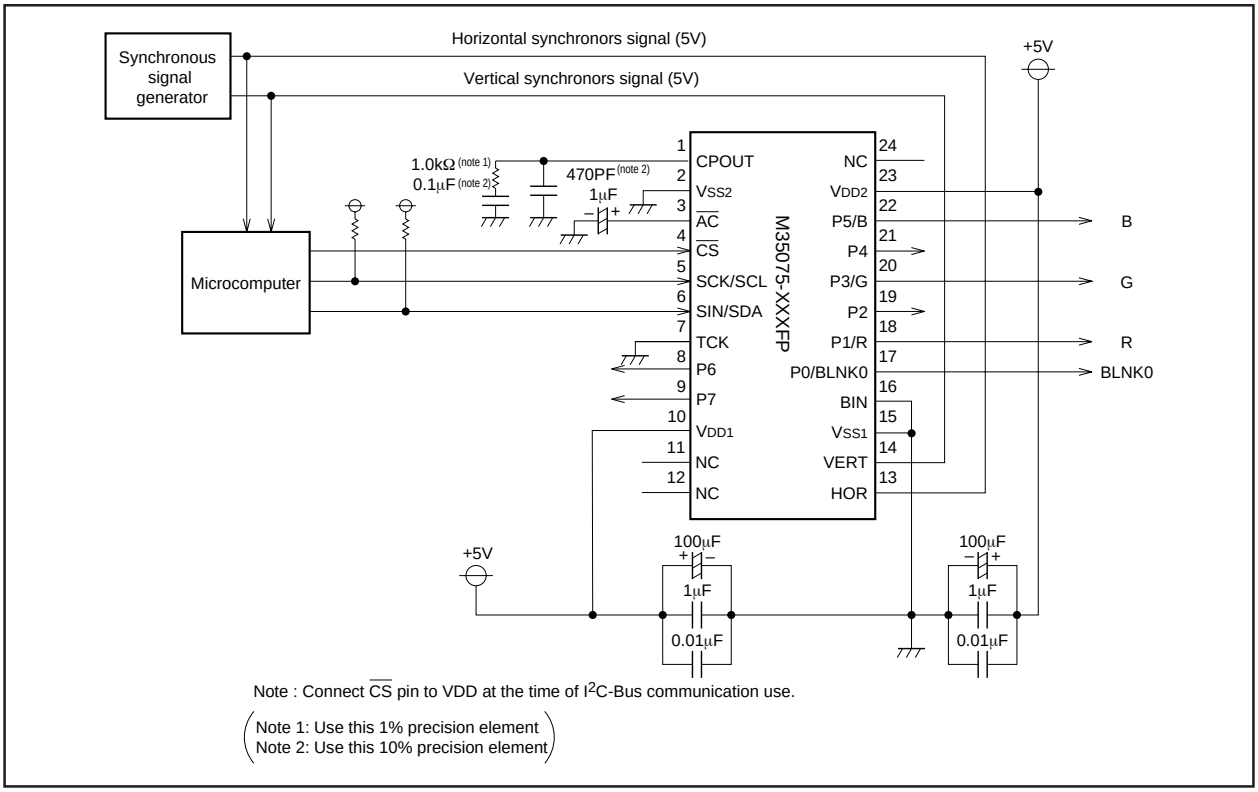
Notes 1 : Input a continuous clock of constant period from the TCK pin. Also, input a horizontal synchronous signal into the HOR pin and a vertical synchronous signal into the VERT pin.
2 : Matrix-outline display in this data.
3 : Secure the waiting time of 200ms after releasing $\overline{AC}$, and set data from setting the display frequency (setting of the register).
4 : Set data to Display RAM and Display character RAM at internal clock (display clock) is stabilized.

Fig. 19 Example of data setting



Notes 1: CPOUT pin can be opened when use only EXCK1= "0" and EXCK= "0."
2: Connect $\overline{CS}$ pin to VDD at the time of I²C-Bus communication use.

Fig.20 Example of the M35075-XXXFP peripheral circuit (Internal synchronous. At EXCK1 = "0", EXCK0 = "0")



Note : Connect $\overline{CS}$ pin to VDD at the time of I²C-Bus communication use.

(Note 1: Use this 1% precision element
Note 2: Use this 10% precision element)

Fig.21 Example of the M35075-XXXFP peripheral circuit (External synchronous. At EXCK1 = "0", EXCK0 = "1")

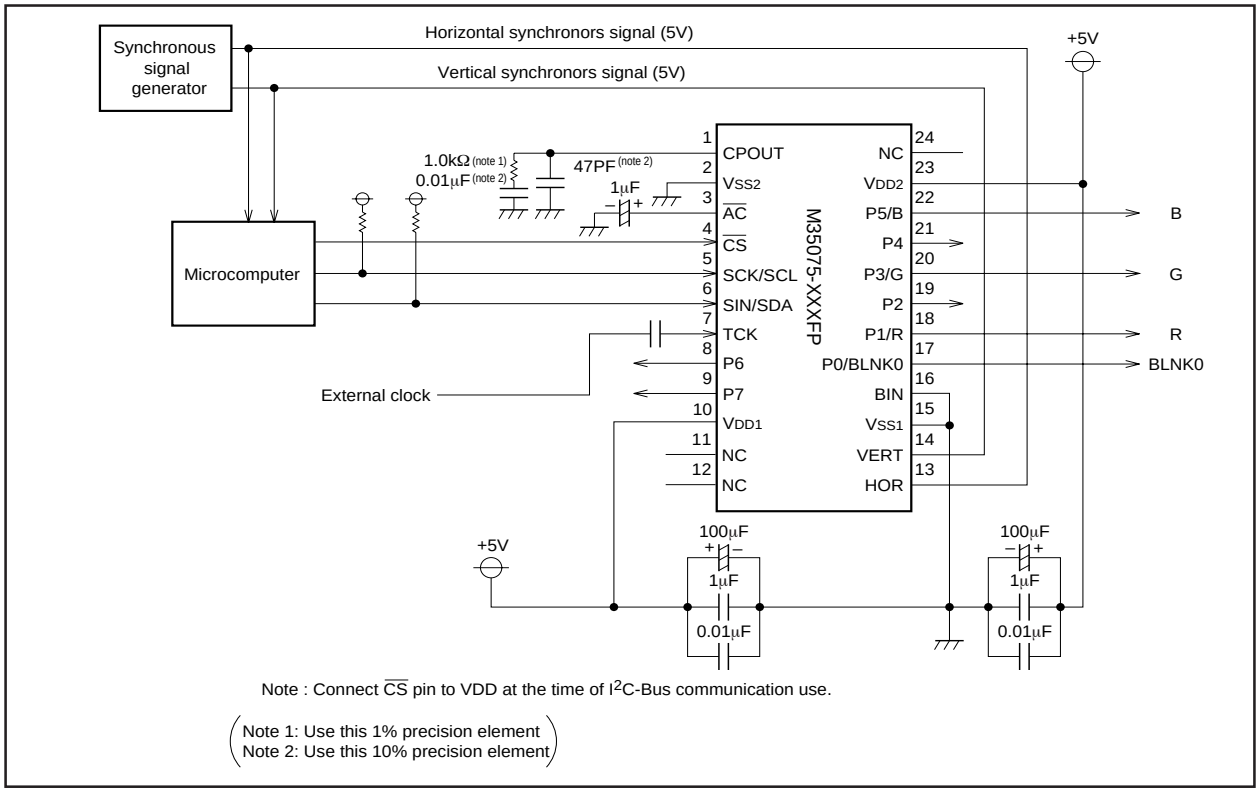


Fig.22 Example of the M35075-XXXFP peripheral circuit (External clock mode 2. At EXCK1 = "1", EXCK0 = "1")

DATA INPUT 1

(1) The16-bit communication function

(a)Serial data should be input with the LSB first.

(b)The address consists of 16 bits.

(c)The data consists of 16 bits.

(d)The 16 bits in the SCK after the $\overline{CS}$ signal has fallen are the address, and for succeeding input data, the address is incremented every 16 bits. Therefore, it is not necessary to in put the address from the second data.

Note. Stop the input to SCK pin and fix it to “H” at $\overline{CS}$ pin “H” level.

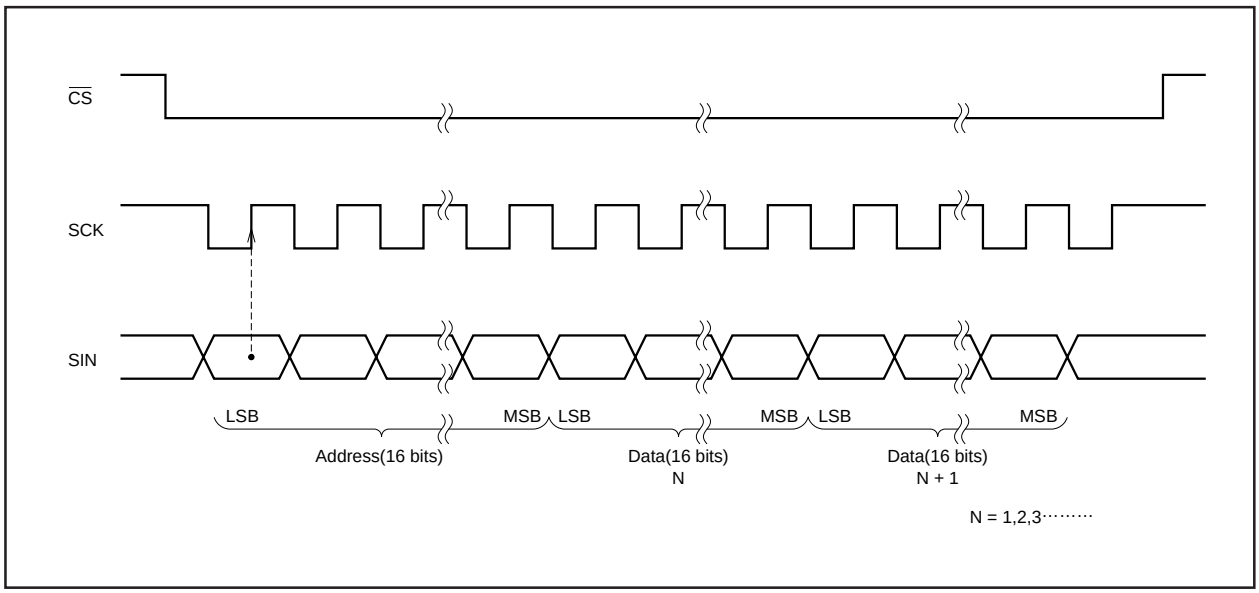


Fig.23 Serial input timing

(2)Timing requirements
Data input

Symbol	Parameter	Limits			Unit	Remarks
		Min.	Typ.	Max.		
$t_{w(SCK)}$	SCK width	200	—	—	ns	See Figure 24
$t_{su(\overline{CS})}$	$\overline{CS}$ setup time	200	—	—	ns	
$t_{h(\overline{CS})}$	$\overline{CS}$ hold time	2	—	—	µs	
$t_{su(SIN)}$	SIN setup time	200	—	—	ns	
$t_{h(SIN)}$	SIN hold time	200	—	—	ns	
t_{word}	1 word writing time	10	—	—	µs	

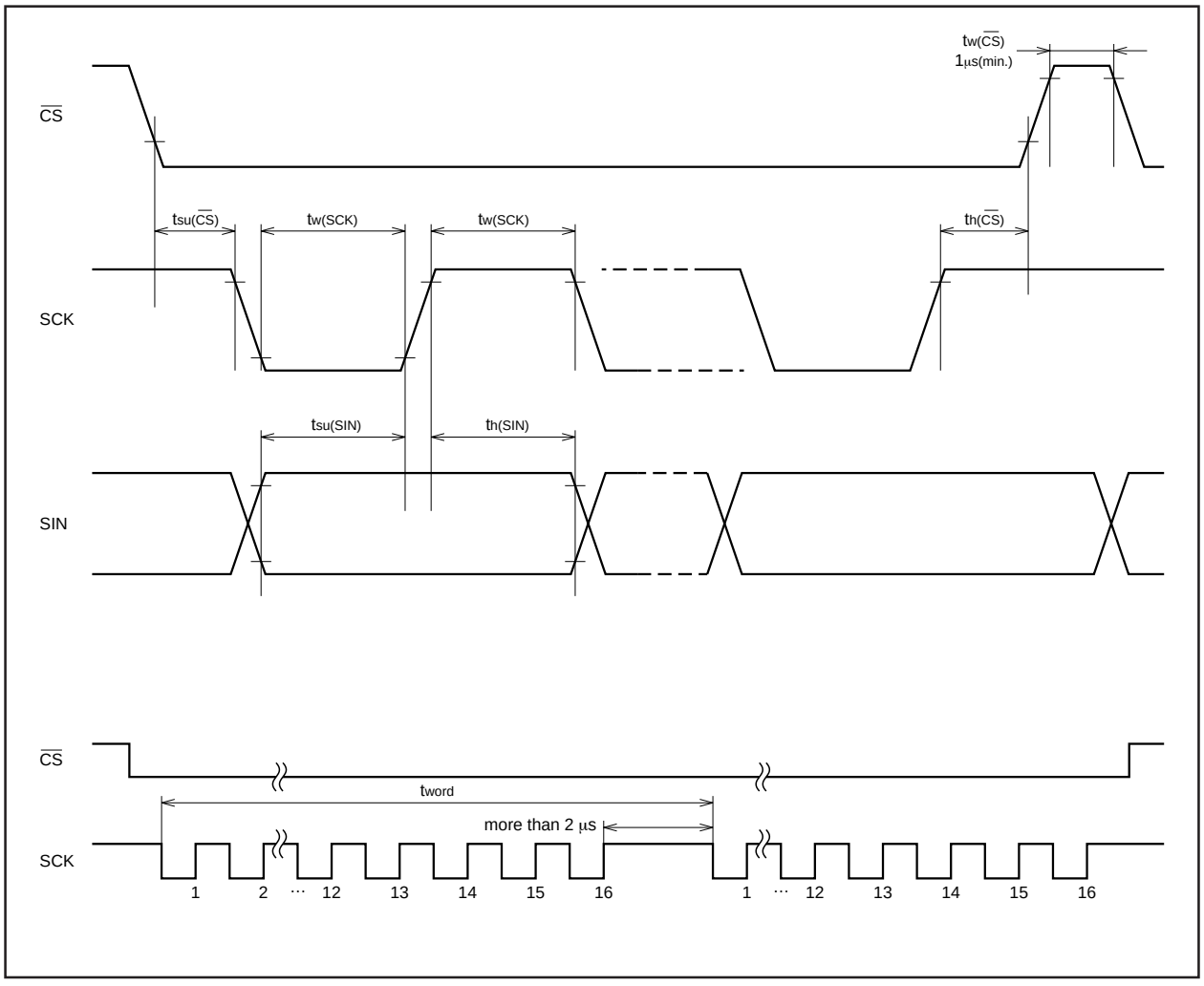


Fig. 24 Serial input timing requirements

DATA INPUT 2

(1) I²C-Bus communication function

This IC has a built-in data transmission interface which utilizes 2 unidirectional buses. In communications, this IC functions as a slave reception device.

Must connect $\overline{CS}$ pin to "H" at the time of I²C-Bus communication use.

The IC is synchronized with the serial clock (SCL) sent from the master device and receives the data (SDA).

Communications are controlled from the start/stop states.

Also, always in put the control byte after attaining the start state.

The below chart shows the start/stop state and control byte configuration.

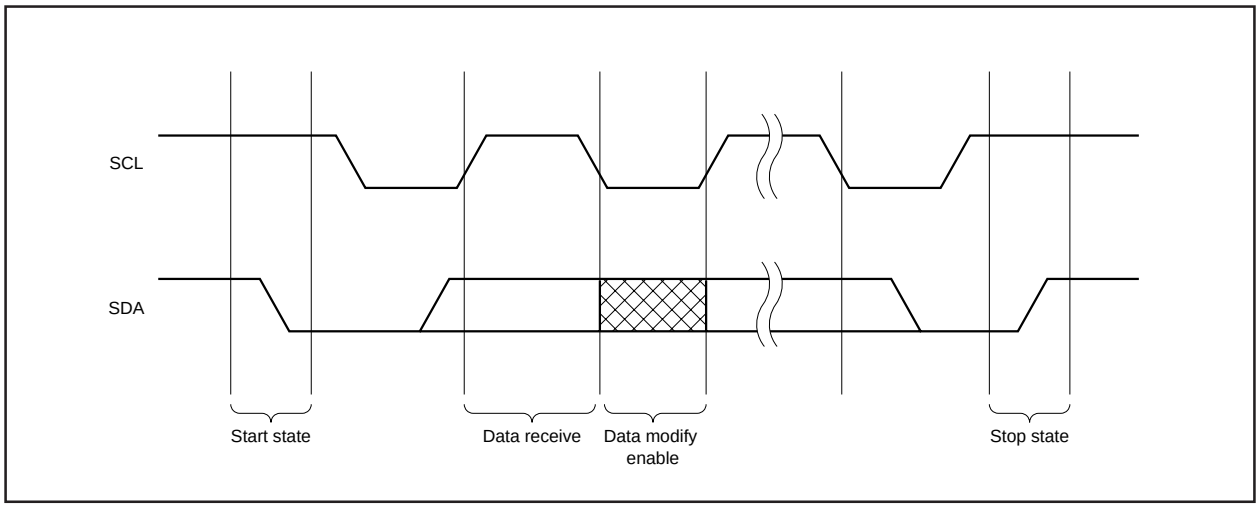


Fig.25 Start state / Stop state

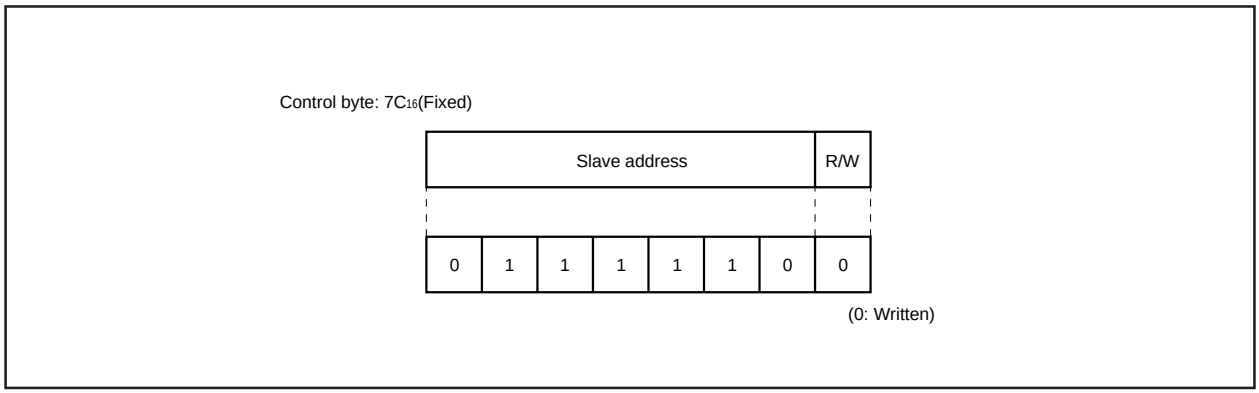


Fig.26 Control byte configuration

(2) Data input (Sequence)

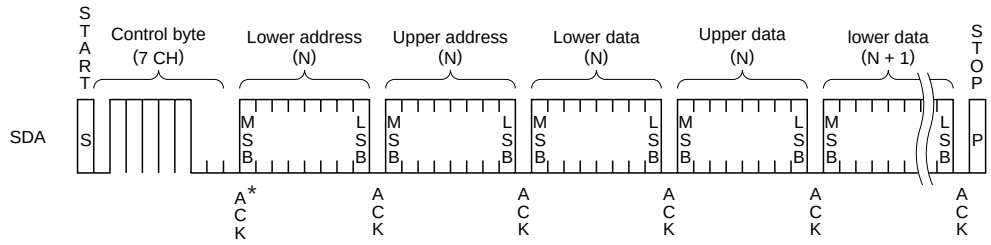
(a) Addresses are consists of 16 bits.

(b) Data is consists of 16 bits.

(c) Addresses and data are communicated in 8-bit units. Input the lower 8 bits before the upper 8 bits. Make input from the MSB side.

(d) After the start state has been attained and the control byte (7CH) received, the next 16 bits (2 bytes) are for inputting the address. Addresses are increased in increments for every 16 bits (2 bytes) of data input thereafter. As a result, it is not necessary to input the address from the second data.

Note:During external synchronous , do not stop the external clock input from the TCK pin while inputting data.



ACK* (Acknowledge) : Output the acknowledge signal whenever one byte input after the start state. Output the acknowledge signal and recieve the data thereafter when match the slave address (7CH).

Fig.27 Data input sequence

(2) Timing requirements
Data input

Symbol	Parameter	Limits				Unit	Remarks
		Typ. mode		High-speed mode			
		Min.	Max.	Min.	Max.		
f_{CLK}	Clock frequency	0	100	0	400	KHz	
t_{HIGH}	HIGH period of Clock	4000	–	600	–	ns	
t_{LOW}	LOW period of Clock	4700	–	1300	–	ns	
t_R	SDA & SCL rise time	–	1000	20+(Note) 0.1C_B	300	ns	
t_F	SDA & SCL fall time	–	300	20+(Note) 0.1C_B	300	ns	
t_{HD} : STA	Hold time at START status	4000	–	600	–	ns	
t_{SU} : STA	Set up time at START status	4700	–	600	–	ns	Only at START state repeating generation
t_{HD} : DAT	Data input hold time	0	–	0	–	ns	
t_{SU} : DAT	Data input setup time	250	–	100	–	ns	
t_{SU} : STO	Set up time at STOP state	4000	–	600	–	ns	
t_{BUF}	Bus release time	4700	–	1300	–	ns	Time must be released bus before next transmission
t_{SP}	Input filter / spike suppress (SDA & SCL pin)	N/A	N/A	0	50	ns	

Note. CB = total capacitance of 1 bus line.

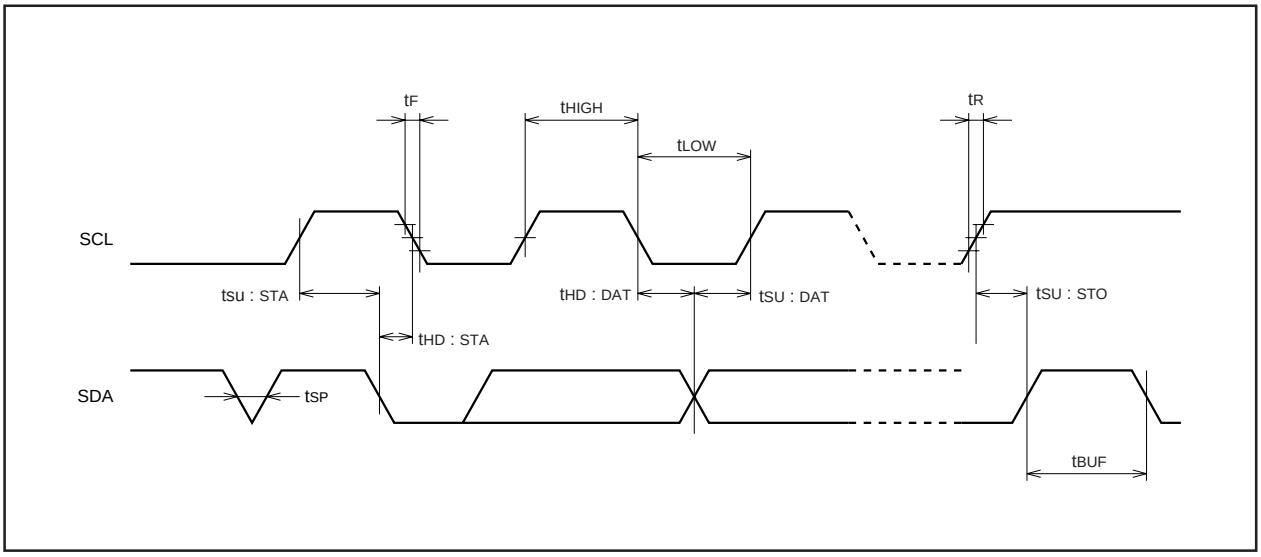


Fig.28 Data input timing

ABSOLUTE MAXIMUM RATINGS (V_{DD} = 5.00V, Ta = –20 to +85°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Supply voltage	With respect to V_{SS}.	–0.3 to +6.0	V
V_I	Input voltage		V_{SS} –0.3 ≤ V_I ≤ V_{DD} +0.3	V
V_O	Output voltage		V_{SS} ≤ V_O ≤ V_{DD}	V
P_d	Power dissipation	Ta = +25 °C	+300	mW
T_{opr}	Operating temperature		–20 to +85	°C
T_{stg}	Storage temperature		–40 to +125	°C

RECOMMENDED OPERATING CONDITIONS (V_{DD} = 5.00V, Ta = –20 to +85°C, unless otherwise noted)

Symbol	Parameter			Limits			Unit
				Min.	Typ.	Max.	
V_{DD}	Supply voltage	5V		4.75	5.0	5.25	V
		3V		2.50	3.0	3.50	V
V_{IH}	"H" level input voltage	$\overline{AC}$, $\overline{CS}$, HOR, VERT		0.8V_{DD}	V_{DD}	V_{DD}	V
		SCK/SCL, SIN/SDA		0.7V_{DD}	V_{DD}	V_{DD}	V
V_{IL}	"L" level input voltage	$\overline{AC}$, $\overline{CS}$, HOR, VERT		0	0	0.2V_{DD}	V
		SCK/SCL, SIN/SDA		0	0	0.3V_{DD}	V
F_{OSC}	Oscillating frequency for display	External clock mode 1	V_{DD} = 4.75 to 5.25 V	6.3	—	80.0	MHz
			V_{DD} = 2.50 to 3.50 V	6.3	—	40.0	MHz
		External clock mode 2	V_{DD} = 4.75 to 5.25 V	20.0	—	110.0	MHz
		Internal clock mode	V_{DD} = 4.75 to 5.25 V	20.0	—	110.0	MHz
H.sync	Horizontal synchronous signal input frequeney		V_{DD} = 4.75 to 5.25 V	15.0	—	130.0	kHz
			V_{DD} = 2.50 to 3.50 V	15.0	—	60.0	kHz

ELECTRICAL CHARACTERISTICS 1 (V_{DD} = 5.00V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{DD}	Supply voltage		Ta = –20 to +85°C	4.75	5.0	5.25	V
I_{DD}	Supply current		V_{DD} = 5.00V	—	40	60	mA
V_{OH}	"H" level output voltage	P0 to P7 (Note1)	V_{DD} = 4.75V, I_{OH} = -0.4mA	3.5	—	—	V
		CPOUT	V_{DD} = 4.75V, I_{OH} = -0.05mA				
V_{OL}	"L" level output voltage	P0 to P7 (Note2)	V_{DD} = 4.75V, I_{OL} = 0.4mA	—	—	0.4	V
		CPOUT	V_{DD} = 4.75V, I_{OL} = 0.05mA				
		SIN/SDA	V_{DD} = 4.75V, I_{OL} = 3.0mA				
R_I	Pull-up resistance $\overline{AC}$, $\overline{CS}$		V_{DD} = 5.00V	10	30	100	kΩ
V_{TCK}	External clock input width		4.75V ≤ V_{DD} ≤ 5.25V	0.6V_{DD}	—	0.9V_{DD}	V

Notes 1. The current from the IC must not exceed – 0.4 mA/port at any of the port pins (P0 to P7).
2. The current flowing into the IC must not exceed 0.4 mA/port at any of port pins (P0 to P7).

ELECTRICAL CHARACTERISTICS 2 V_{DD}=3V (V_{DD} = 3.00V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply voltage	Ta = –20 to +85°C	2.50	3.00	3.50	V
I_{DD}	Supply current	V_{DD} = 3.00V	—	20	30	mA
V_{OH}	"H" level output voltage P0 to P7 (Note1)	V_{DD} = 2.70V, I_{OH} = -0.1mA	2.30	—	—	V
V_{OL}	"L" level output voltage P0 to P7 (Note2)	V_{DD} = 2.70V, I_{OH} = 0.1mA	—	—	0.4	V
R_I	Pull-up resistance $\overline{AC}$, $\overline{CS}$	V_{DD} = 3.00V	30	—	150	kΩ
V_{TCK}	External clock input width	2.50V ≤ V_{DD} ≤ 3.50V	0.9V_{DD}	—	V_{DD}	V

Notes 1. The current from the IC must not exceed – 0.1 mA/port at any of the port pins (P0 to P7).
2. The current flowing into the IC must not exceed 0.1 mA/port at any of port pins (P0 to P7).

NOTE FOR SUPPLYING POWER

(1)Timing of power supplying to $\overline{AC}$ pin

The internal circuit of M35075-XXXFP is reset when the level of the auto clear input pin $\overline{AC}$ is "L". This pin in hysteresis input with the pull-up resistor.

The timing about power supplying of $\overline{AC}$ pin is shown in Figure 29.

After supplying the power (V_{DD} and V_{SS}) to M35075-XXXFP and the supply voltage becomes more than 0.8 × V_{DD}, it needs to keep V_{IL} time; tw of the $\overline{AC}$ pin for more than 1ms.

Start inputting from microcomputer after $\overline{AC}$ pin supply voltage becomes more than 0.8 × V_{DD} and keeping 200ms wait time.

(2)Timing of power supplying to V_{DD1} and V_{DD2}.

Supply power to V_{DD1} and V_{DD2} at the same time.

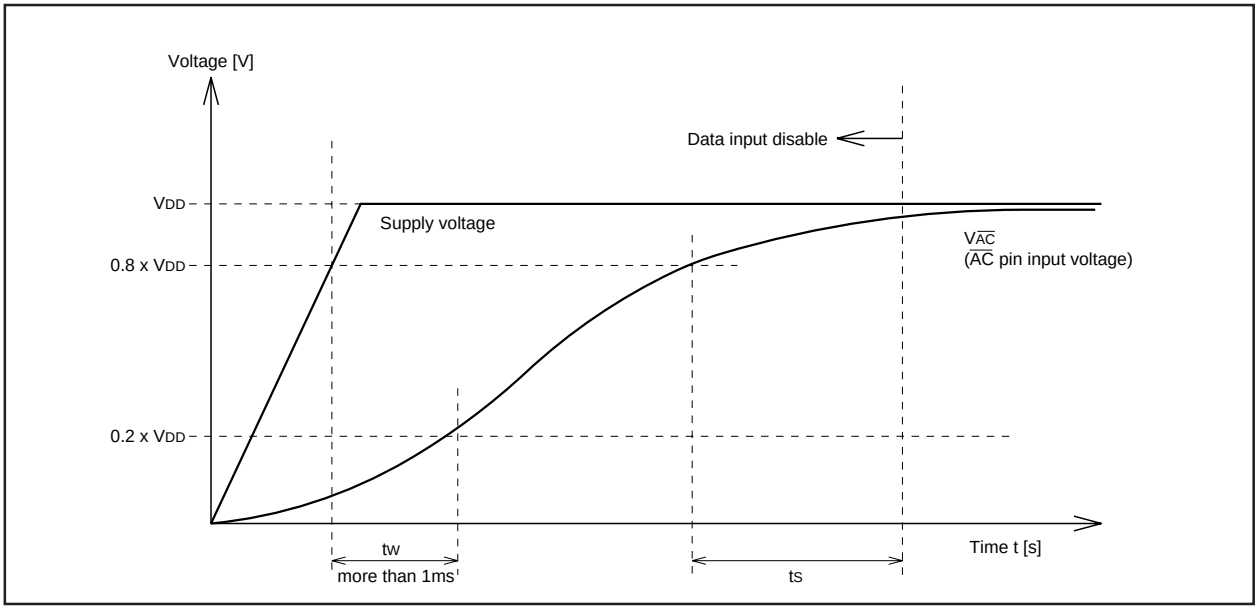


Fig.29 Timing of power supplying to $\overline{AC}$ pin

PRECAUTION FOR USE

Notes on noise and latch-up

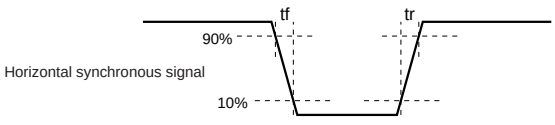
In order to avoid noise and latch-up, connect a bypass capacitor (≈0.1µF) directly between the V_{DD1} pin and V_{SS1} pin, and the V_{DD2} pin and V_{SS2} pin using a heavy wire.

Note for waveform timing of the horizontal signals to the HOR pin

Set horizontal synchronous signal edge* waveform timing to under 5ns and input to HOR pin.

Set only the side which set by B/$\overline{F}$ register waveform timing under 5ns and input to HOR pin.

*: Set front porch edge or back porch edge by B/$\overline{F}$ register.



DATA REQUIRED FOR MASK ROM ORDERING

Please send the following data for mask orders.

(1) M35075-XXXFP mask ROM order confirmation form

(2) 24P2Q mark specification form

(3) ROM data : EPROMs or floppy disks

*In the case of EPROMs, thres sets of EPROMs are required per pattern.

*In the case of floppy disks, 3.5-inch 2HD disk (1BM format) is required per pattern.

STANDARD ROM TYPE : M35075-001FP

M35075-001FP is a standard ROM type of M35075-XXXFP.
The character patterns are fixed to the contents of Figure 30 to 33.

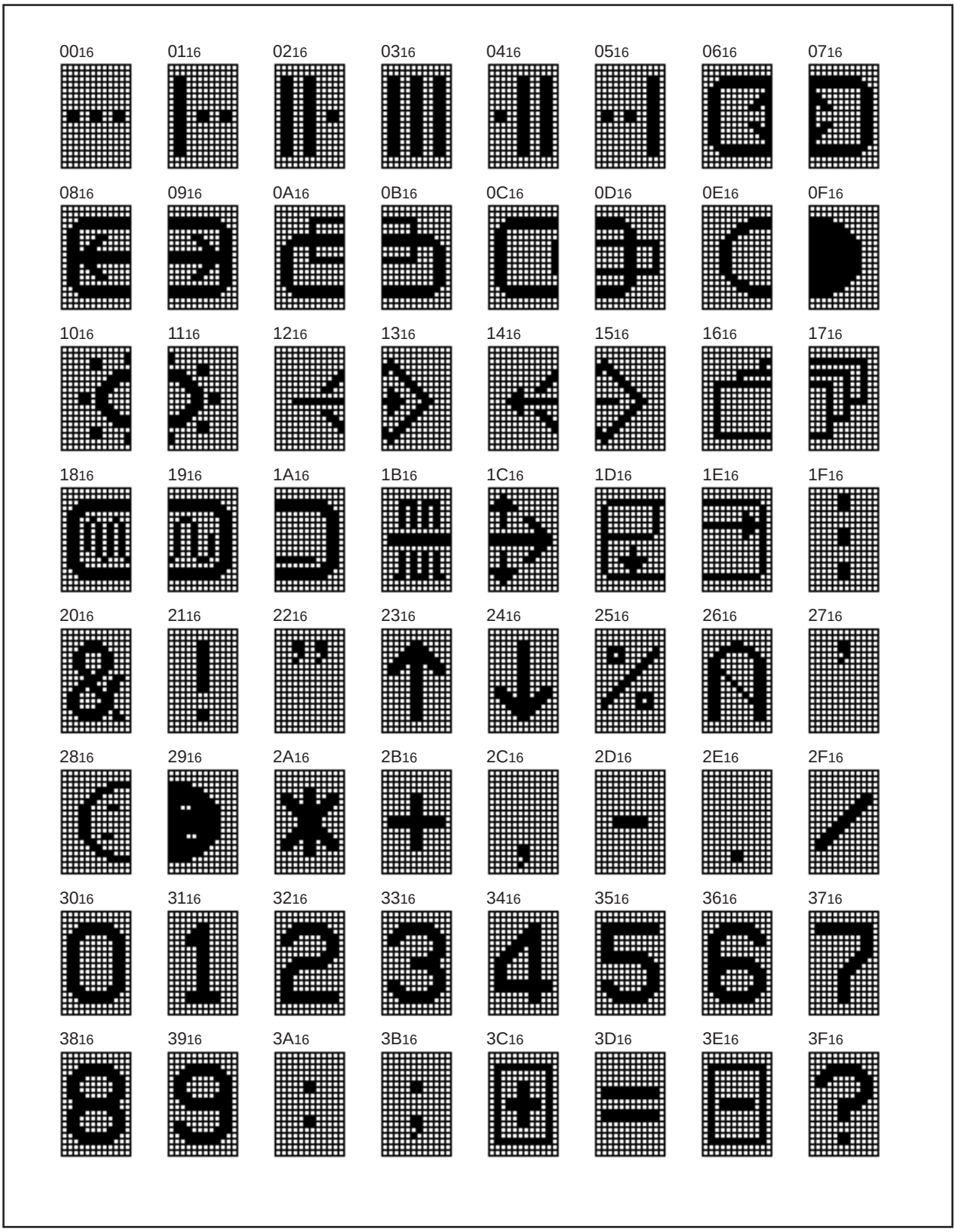


Fig.30 M35075-001FP character patterns (1)

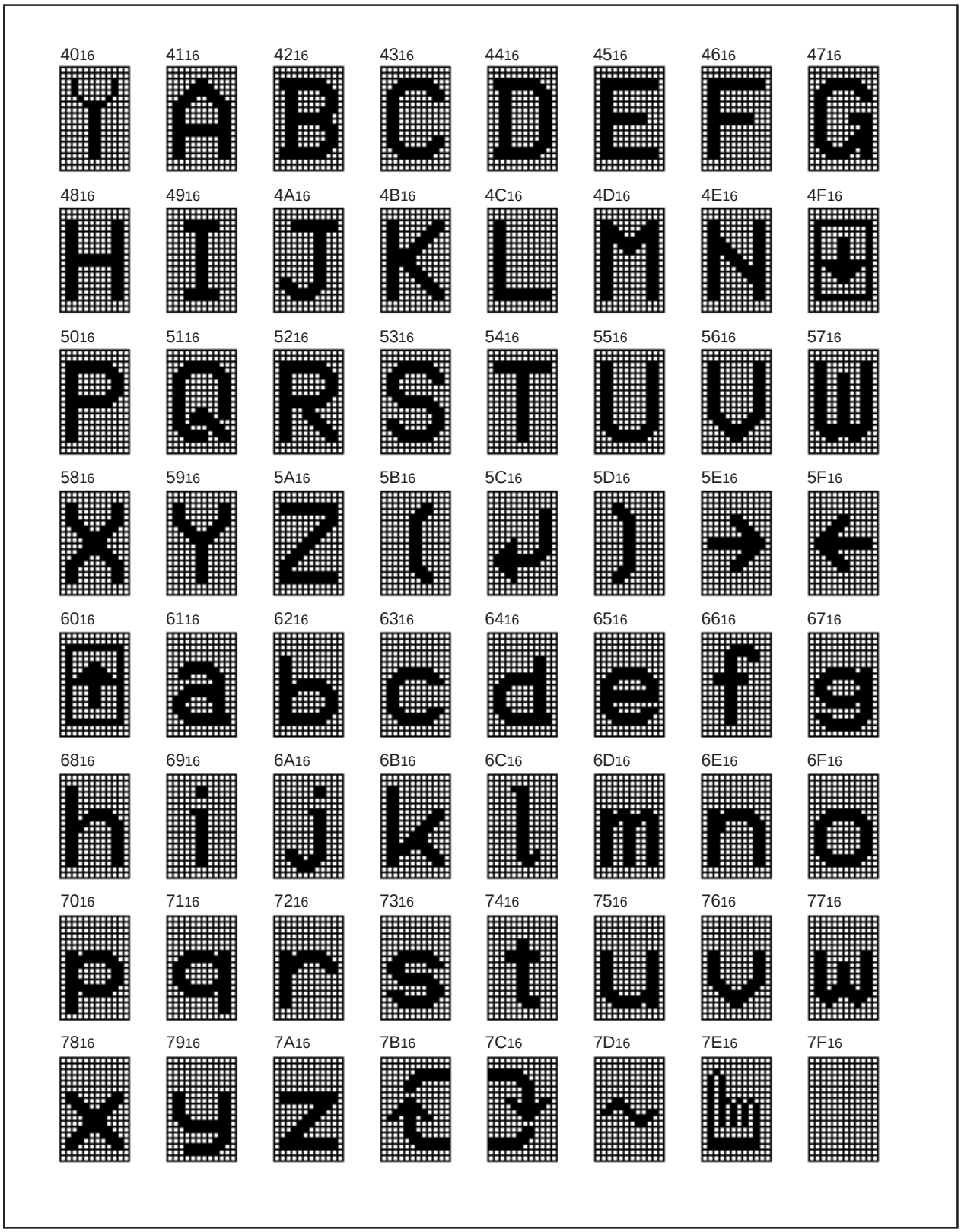


Fig.31 M35075-001FP character patterns (2)

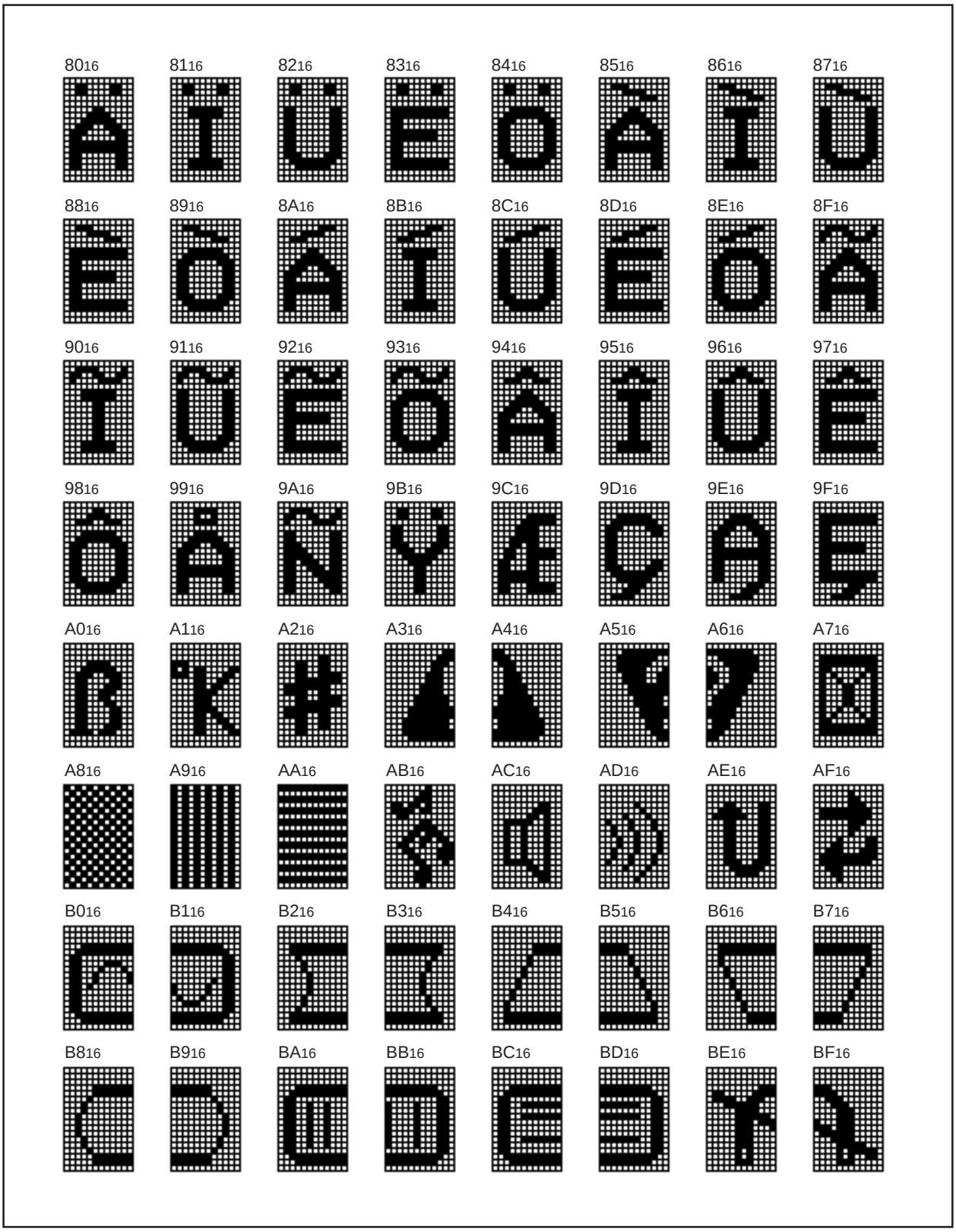


Fig.32 M35075-001FP character patterns (3)

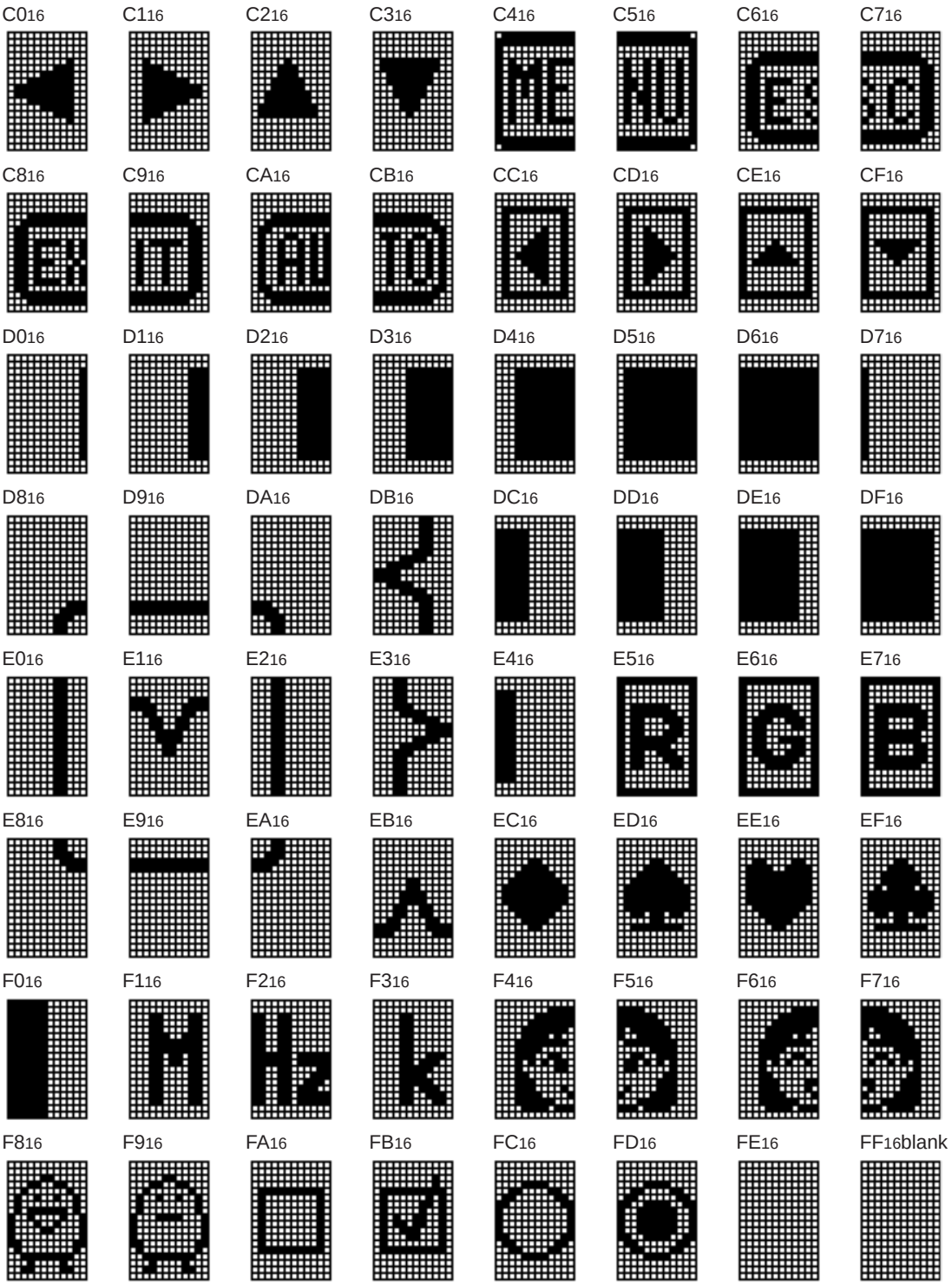
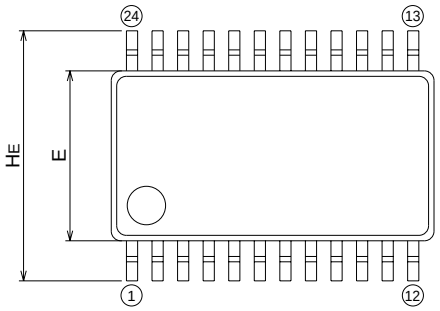


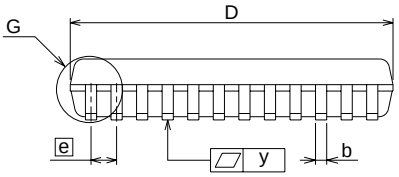
Fig.33 M35075-001FP character patterns (4)

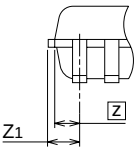
PACKAGE OUTLINE

24P2Q-A (MMP) **Plastic 24pin 300mil SSOP**

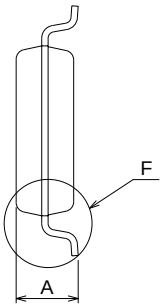
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP24-P-300-0.80	–	0.2	Cu Alloy

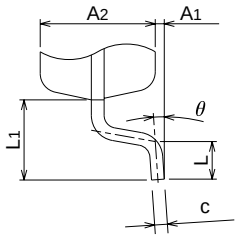




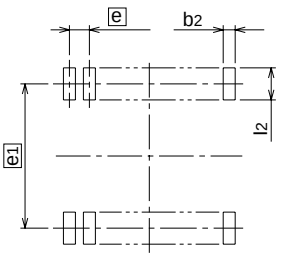


Detail G





Detail F



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	2.1
A_1	0	0.1	0.2
A_2	–	1.8	–
b	0.3	0.35	0.45
c	0.18	0.2	0.25
D	10.0	10.1	10.2
E	5.2	5.3	5.4
e	–	0.8	–
H_E	7.5	7.8	8.1
L	0.4	0.6	0.8
L_1	–	1.25	–
z	–	0.65	–
Z_1	–	–	0.8
y	–	–	0.1
θ	0°	–	8°
b_2	–	0. 5	–
e_1	–	7.62	–
l_2	1.27	–	–

REVISION HISTORY	M35075-XXXFP

Rev.	Date	Description	
		Page	Summary
1.00	Mar 01, 2002	-	First edition issued
1.10	Feb 13, 2006	P36	"RECOMMENDED OPERATING CONDITIONS" and "ELECTRICAL CHARACTERISTICS 1" are changed.
		P37	"ELECTRICAL CHARACTERISTICS 2" is changed.