SIEMENS

SMPS - IC with SIPMOS Driver Output

TDA 4918
TDA 4919

Bipolar IC

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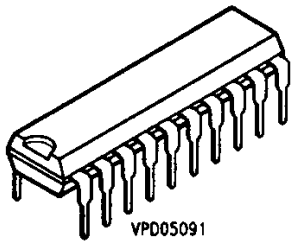
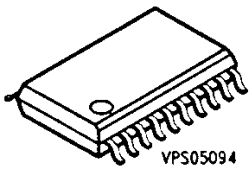
Features

- Switching frequency up to 300 kHz (TDA 4919) or 150 kHz (TDA 4918)
- Push-pull output driver with + 700 mA/– 500 mA
- Separate GND for the driver outputs
- Feed-forward control
- Soft start
- Hysteresis adjustable at overvoltage and undervoltage comparator
- Current-saving starting circuit
- Current mode and voltage mode operation are possible



P-DIP-20-1

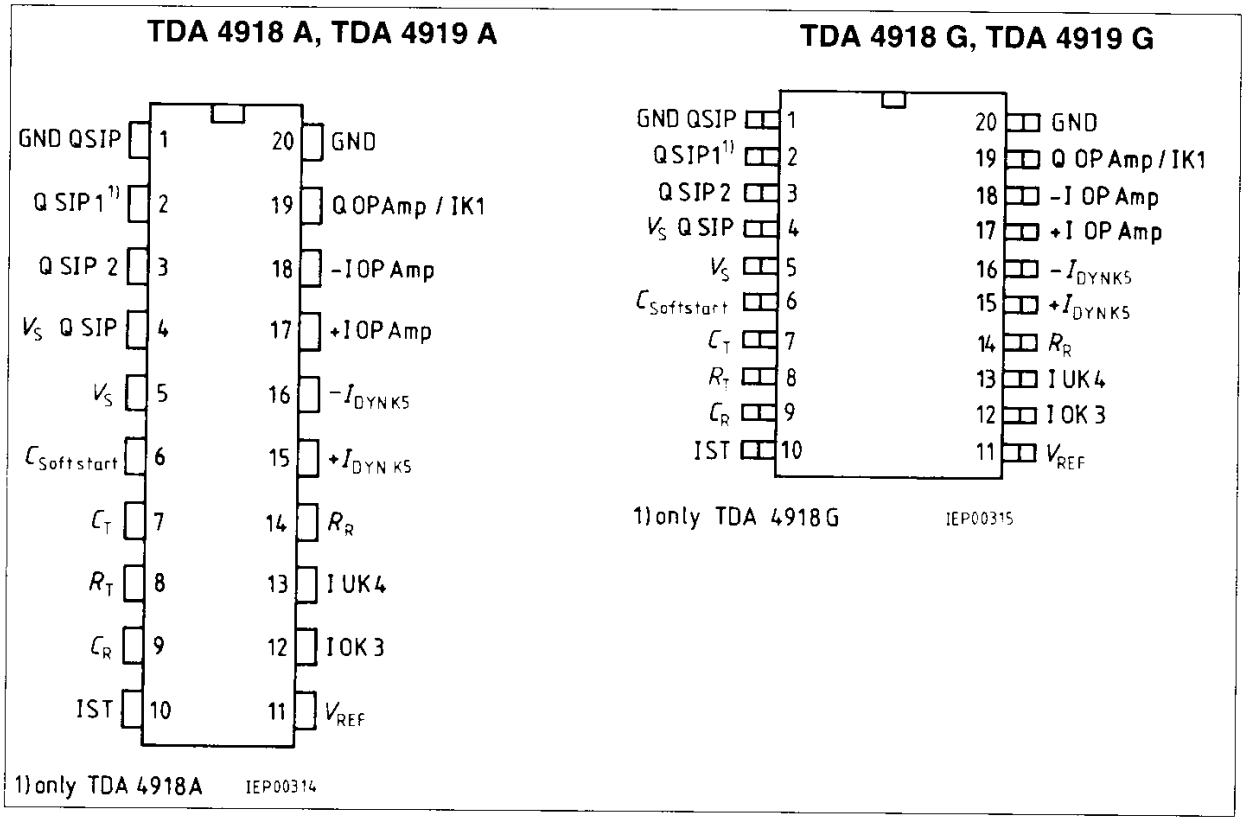


P-DSO-20-1

	Type	Ordering Code	Package
S	TDA 4918 A	Q67000-A8021	P-DIP-20-1
S	TDA 4918 G	Q67000-A8142	P-DSO-20-1 (SMD)
S	TDA 4919 A	Q67000-A8143	P-DIP-20-1
S	TDA 4919 G	Q67000-A8018	P-DSO-20-1 (SMD)

Functional Description

The versatile switch-mode power supply ICs for the direct control of SIPMOS power transistors comprise digital and analog functions. These functions are required for the design of high-quality flyback and forward converters during single-phase and push-pull operation in normal, half-bridge and full-bridge configurations. The ICs can also be used for transformerless voltage multipliers and speed-controlled motors. Malfunctions in the electrical operation of the switch-mode power supply are recognized by on-chip comparators which activate protective functions. The TDA 4918 has two driver outputs for push-pull switch-mode power supplies, as well as single-phase SMPS with a duty cycle limitation of 50 %. The TDA 4919 with a driver output is suitable for single-ended SMPS with duty cycles of up to 100% approximately.



Pin Configuration
(top view)

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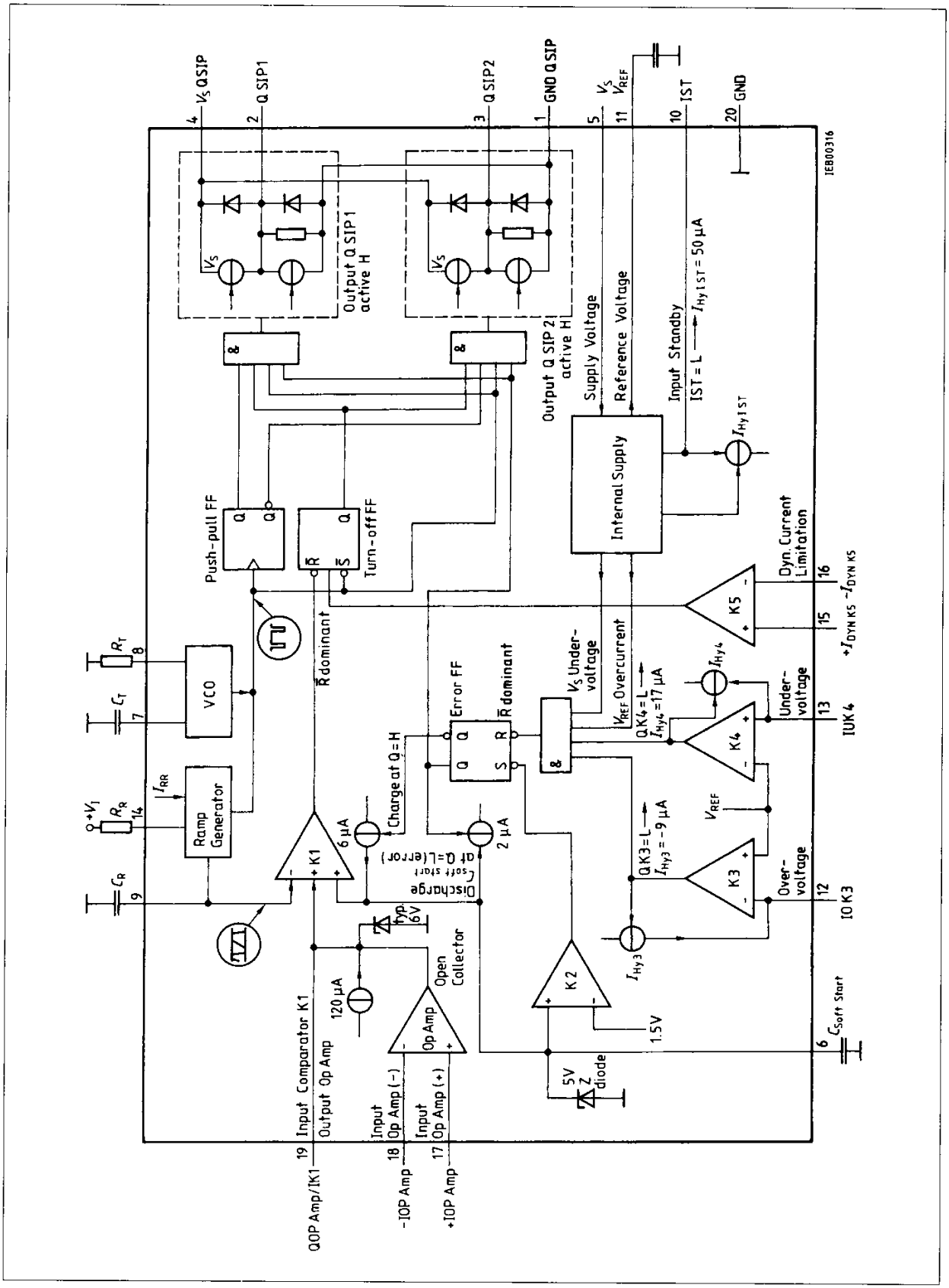
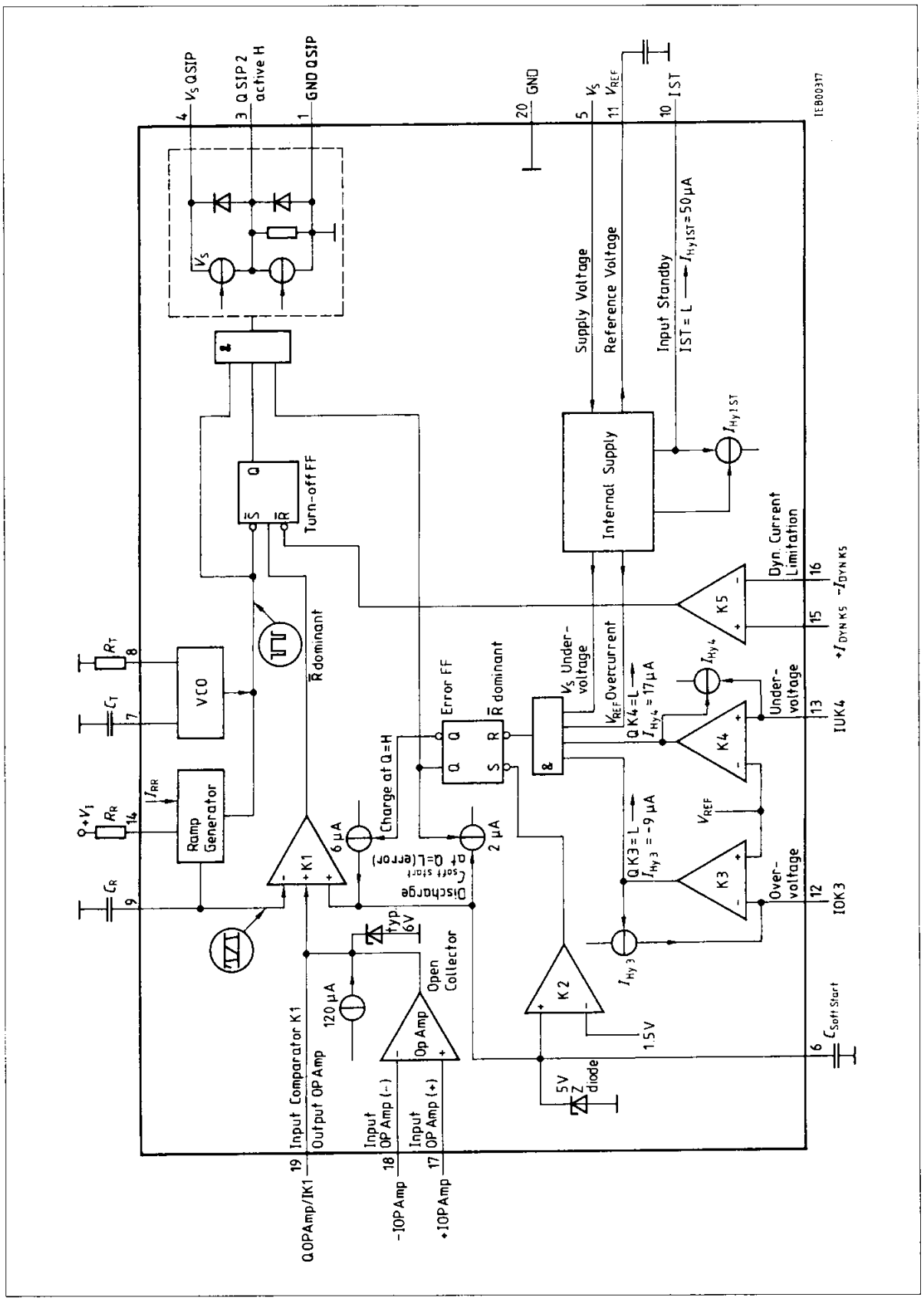
Pin Definitions and Functions

Pin	Symbol	Function
1	GND Q SIP	Ground driver
2	Q SIP1	SIPMOS driver 1 (only TDA 4918)
3	Q SIP2	SIPMOS driver 2
4	V_S QSIP	Supply voltage driver
5	V_S	Supply voltage
6	$C_{soft\ start}$	Soft start
7	C_T	Frequency generator
8	R_T	Frequency generator
9	C_R	Ramp generator
10	I ST	Input standby
11	V_{REF}	Reference voltage
12	I OK3	Input overvoltage
13	I UK4	Input undervoltage
14	R_R	Ramp generator
15	$+ I_{DYN\ K5}$	Dyn. current limitation
16	$- I_{DYN\ K5}$	Dyn. current limitation
17	I Op Amp (+)	Input operational amplifier
18	I Op Amp (–)	Input operational amplifier
19	Q Op Amp/IK1	Output operational amplifier Q Op Amp / input comparator
20	GND	Ground



Block Diagram (TDA 4918)



Block Diagram (TDA 4919)

Functional Description

The various functional units of the component and their interaction are described in the following.

Supply Voltage V_S

The IC enables the two outputs not before the turn-on threshold ($V_{S\,ON}$) at V_S is exceeded. The duty cycle (active time/disable time) at the enabled outputs can then rise from zero to the value set with K1 in the time specified by the soft start.

An undervoltage at the standby input causes the current consumption I_S to remain at the very low standby current level independent of the voltage V_S.

Voltage Controlled Oscillator (VCO)

The VCO is connected with the capacitor C_T and the resistor R_T. The charge current at C_T flows continuously and is set with resistor R_T. The discharge current is active during the discharge of C_T and is set internally.

In the typical mode of operation the duration of the rising edge is considerably greater than that of the falling edge. During the falling edge the VCO passes a trigger signal to the ramp generator thus discharging the ramp generator capacitance. Additionally, the trigger signal is routed to other parts of the IC.

Ramp Generator

The ramp generator is triggered by the VCO and TDA 4919 operates at the same frequency as the VCO. The duration of the ramp generator falling edge must be shorter than the VCO fall time. Only then do the ramp generator upper and lower switching levels reach their rated values.

To control the pulse width at the output, the voltage of the ramp generator rising edge is compared with an externally adjustable dc voltage at comparator K1. The slope of the rising edge is adjusted via the current by means of R_R. This provides the possibility of an additional superimposed control of the output duty cycle. This control capability (feed-forward control) permits the compensation of known interference (e.g. input voltage ripple). A superimposed load current control **(current mode control)** however, can also be implemented.

Push-Pull Flipflop (only TDA 4918)

The push-pull flipflop is switched by the falling edge of the VCO. This ensures that only one output of the two SIPMOS driver outputs is enabled at a time.

Comparator K1 (Duty Cycle Control)

The two plus inputs of the comparator are switched such that the lower plus level is always compared with the level of the minus input. As soon as the voltage of the rising sawtooth edge (minus input) exceeds the lower level of the two plus inputs, the currently active output is disabled via the turn-off flipflop. The "high"-duration of the respectively active output can thus be infinitely varied. As the frequency remains constant, this process corresponds to a change in duty cycle.

Operational Amplifier (Op Amp)

The op amp is a high quality operational amplifier. It can be used in the control circuit to transmit the amplified variations of the voltage to be regulated to the free plus input of comparator K1. A voltage change is thus converted to a duty cycle change.

Turn-OFF Flipflop

The falling edge of the VCO causes a pulse at the turn-off flipflop set input. It can, however, only be actually set if no reset signal is pending. With the turn-OFF flipflop set, the outputs are enabled. Upon an error signal from K5 or upon a turn-off signal from K1 the flipflop disables the outputs.

Z-Diode

The Z-diode limits the voltage at capacitor $C_{\text{soft start}}$ to a maximum of 5 V. The ramp generator voltage can reach 5.5 V. For an appropriate slope of the rising ramp generator edge, the duty cycle can be limited to a desired maximum value. This can be a possible advantage in flyback converter operation.

Comparator K2

The comparator has its switching threshold at 1.5 V at the plus input, and with its output it sets the error flipflop if the voltage at capacitor $C_{\text{soft start}}$ is below 1.5 V. The error flipflop, however, will only accept the set pulse if no reset pulse (error) is pending. This prevents a restart of the outputs as long as an error signal is pending.

Soft Start

The lower of the two voltages at the K1 plus inputs - compared with the ramp generator voltage - is a measure for the duty cycle at the output. At component turn-on, the voltage at capacitor $C_{\text{soft start}}$ is equal to 0. As long as no error exists, the capacitor will be charged to the maximum value of 5 V with a current of 6 µA.

In the case of an error, $C_{\text{soft start}}$ is discharged with a current of 2 µA. The currently active output, however, is immediately disabled by the error flipflop. Below a charge voltage of 1.5 V, a set signal is pending at the error flipflop and the outputs are enabled if no reset signal is pending at the same time. As the minimum ramp generator voltage, however, is 1.8 V, the duty cycle at the outputs is actually only increased slowly and continuously after the voltage at $C_{\text{soft start}}$ exceeds 1.8 V.

Error Flipflop

Error signals, routed to the error flipflop reset input, cause an immediate disabling of the outputs (low), and after elimination of the error, a restart of the outputs by soft start.

Comparators K3 (Overvoltage), K4 (Undervoltage), V_{REF} Overcurrent, V_S Undervoltage

These are error detectors that on error cause the error flipflop to immediately disable the outputs. After elimination of the error, the duty cycle is raised again using the soft start. Upon overvoltage, a current is impressed at the inputs of K3 and K4, that can be used to enable an adjustable hysteresis or a holding function. The value of the hysteresis is derived from the internal resistance of the external control source and the current impressed internally at the input of K3 or K4. In the undervoltage case, the set current flows at K4 into the component in the technical direction of current flow, with overvoltage at K3 out of the component.

Comparator K5 (Dynamic Current Limiter)

K5 serves to recognize overcurrents at the switching transistors. Both inputs of the comparator are externally accessible. After elimination of the error, the outputs are enabled with the VCO trigger pulse at the turn-off flipflop. The delay time between occurrence of an error and disabling of the outputs is only 250 ns.

Standby Input (I ST)

This input switches voltage and current hysteresis. The voltage levels for switching from standby to active operation can be set with an external voltage divider between V_S - standby input - ground.

In standby mode the component has a much lower current consumption compared to active operation. The outputs are then active low.

Should the component be operated by means of feedback supply from the switch-mode power supply, the starting phase can optimally be dimensioned.

Reference Voltage (V_{REF})

The reference voltage source is a highly constant source with regard to its temperature behavior. It can be used for the external wiring of the op amp, the error comparators, the ramp generator, or other external components. The voltage source is short-circuit proof to ground.

SIPMOS Driver Outputs (Q SIP)

TDA 4918

The two outputs operate in the push-pull mode. They are active high. The duration during which one of the outputs is active, can be varied infinitely. The duration of the falling edge at the frequency generator is equal to the minimum duration during which both outputs are simultaneously low.

TDA 4919

The output is active high. The duration during which the output is active can be varied infinitely. The duration of the falling edge at the frequency generator is equal to the minimum duration during which the output is low (dead time).

The output drivers are designed as a push-pull stage. The output current is internally limited to the specified values.

A 10 kΩ resistor is connected between the output and ground. This resistor holds the SIPMOS transistor reliably disabled during standby operation (undervoltage at pin I St).

Output Q SIP is connected with the supply voltage $V_{S\,Q\,SIP}$ and with ground via diodes.

The diode connected to V_S routes the capacitive shift currents from the SIPMOS transistor gate to the filter capacitor at V_S during turning on the SMPS supply voltage. The voltage at V_S can reach approximately 2.3 V without the SIPMOS transistor being turned on.

The diode connected to ground connects negative voltages at Q SIP to – 0.7 V. This provides an unimpeded flow off of capacitive currents occurring during voltage breakdown at the SIPMOS transistor drain connection.

For supply voltages starting at approx. 2 V, both outputs are active low in the disabled state. The function of the diode connected to V_S is then taken over by the pull-down source.

The maximum output voltage is limited by the respectively lowest value of V_S, $V_{S\,Q\,SIP}$ or an internal Z-diode. The internal Z-diode limits the voltage at Q SIP to typ. 20 V.

Absolute Maximum Ratings

T_A = – 40 to 85 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_{SQSIP}, V_S	– 0.3	33	V
Inputs Op Amp, K3, K5, I ST	V_I	– 0.3	33	V
Input K4	V_I	– 0.3	V_S	V
Frequency Generator (VCO)				
Voltage at R_T; C_T	V_{CT}, V_{RT}	– 0.3	6	V
Current at C_T	I_{CT}		3	mA
V_{CT} > 6 V				
Ramp Generator				
C_R input	V_{CR}	– 0.3	6	V
R_R input	I_{RR}	0	3	mA
Reference voltage	V_{REF}	– 0.3	6	V
Output Op Amp	$V_{Q\ op\ amp}$	– 0.3	6	V
$V_{Q\ op\ amp}$ > 6 V	$I_{Q\ op\ amp}$		2	mA
Driver output Q SIP [1]	$V_{Q\ SIP}$	– 0.3	$V_{S\ QSIP}$	V
Q SIP clamp diodes	$I_{Q\ SIP}$	– 100	100	mA
$V_{Q\ SIP} > V_S$ or $V_{Q\ SIP} < -0.3$ V				
Soft start	$V_{C\ soft\ start}$	– 0.3	6	V
$V_{C\ soft\ start}$ > 6 V	$I_{C\ soft\ start}$	0	100	µA
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	– 65	125	°C
Thermal resistance				
system - air P-DIP-20	$R_{th\ SA}$		60	K/W
P-DSO-20	$R_{th\ SA}$		90	K/W

The characteristics refer to both the pins connected to ground.

[1] With this, the max. power dissipation or junction temperature must be taken into account!

Operating Range

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_S $V_{SQ\ SIP}$	$V_{S\ ON}$ [1]	30 30	V V
Frequency generator (VCO) Ramp generator	f_{VCO} f_R		300 300	kHz kHz
Ambient temperature	T_A	– 40	85	°C
Ground QSIP	$V_{GNDQ\ SIP}$	– 0.3	0.5	V

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Characteristics

$V_{SON} < V_S < 30\,V$ [2], $T_A = -40$ to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current consumption without load at V_{REF} Q op amp, Q SIP 1/2	I_S	6		18	mA	$C_T = 1$ nF frequency generator with 100 kHz outputs active
Standby operation	I_{ST}			3.5	mA	$V_S = 20$ V

Hysteresis at V_S

Turn-on threshold for V_S rising	V_{SH}			9.6	V	$V_{IST} \geq V_{ISTH}$
Turn-off threshold for V_S falling	V_{SL}	7.8			V	

The characteristics refer to both the pins connected to ground.

1) For V_{SON} values refer to characteristic data.

2) $V_{S\ ON}$ means that $V_{S\ HIGH}$ has been exceeded, while $V_{S\ LOW}$ has not yet been undercut.

Characteristics (cont'd)
$V_{SON} < V_S < 30\,V$ [1], $T_A = -40$ to $85\,^{\circ}C$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Reference						
Voltage	V_{REF}	2.475	2.5	2.525	V	$I_{REF} = 1\,mA$ $T_A = 25\,^{\circ}C$ $V_S = 15\,V$
Load current	$-I_{REF}$	0		3	mA	
Voltage change Voltage change	ΔV_{REF} ΔV_{REF}			10 3	mV mV	$I_{REF} = 1\,mA \pm 20\%$ $V_S = 15\,V \pm 20\%$
Temperature response	$\Delta V_{REF}/\Delta T\Delta$	-0.3		0.3	mV/K	
Response threshold for V_{REF} overcurrent	$-I_{REF\,O}$	4	7	10	mA	
Frequency Generator (VCO)						
Frequency range	f_{VCO}			300	kHz	
Frequency change Tolerance	$\Delta f/f_{VCO}$ $\Delta f/f_{VCO}$	-7		1 7	% %	$V_S = 15\,V \pm 20\%$ $C_T = 1\,nF$ $f_{VCO} = 100\,kHz$; $T_A = 25\,^{\circ}C$
Charge current for C_T (perm.) = current at pin R_T Discharge current for C_T	 $-I_{RT}$ I_{dch}	 0	 2	 1	 mA mA	 $I_{RT} = V_{REF/RT}$ internally fixed
C_T range		0.47		68	nF [2]	
Dead time	T_t		350 400	450 500	ns ns [2]	$C_T = 470\,pF$, $f_{VCO} = 100\,kHz$ $C_T = 470\,pF$, $f_{VCO} = 300\,kHz$

1) $V_{S\,ON}$ means that $V_{S\,HIGH}$ has been exceeded, while $V_{S\,LOW}$ has not yet been undercut.
2) The time of the falling edge (fall time) is proportional to C_T, if the discharge current largely exceeds the charge current. The fall time is proportional to the minimum dead time at the outputs.

Characteristics (cont'd)
$V_{SON} < V_S < 30$ V [1], $T_A = -40$ to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Ramp Generator						
Frequency range	f_R			300	kHz	
Maximum voltage at C_R Minimum voltage at C_R	V_{CRH} V_{CRL}	5.4 1.65	6.1 1.8	6.7 1.95	V V	
Charge current for C_R (perm) = current at pin R_R Discharge current for C_R	 I_{ch} I_{dch}	 0 1.3	 2	 1 2.7	 mA mA	 V_{RR} approx. 0.7 V internally fixed
Ratio $I_{RR}/I_{CR\,charge}$		0.95		1.1		$I_{RR} = 0.5$ mA
Capacitance	C_R	100			pF	
Duty cycle (active time/ period at output)	 t_V		 5/20			
Temperature coefficient of duty cycle	 T_C		 0.2		 %/K	
Comparator K1						
Input current	$-I_{K1}$			2	µA	
Common-mode input voltage range	 V_{IC}	 0		 V_{CRH}	 V	
Turn-OFF delay time	t			500	ns [2]	Rated load 3 nF at Q SIP

1) $V_{S\,ON}$ means that V_{SHGH} has been exceeded, while $V_{S\,LOW}$ has not yet been undercut.
2) Step function $V_{REF} = -100$ mV ⌐► $V_{REF} = +100$ mV (for transit time from input comparator to Q SIP)

Characteristics (cont'd)
$V_{SON} < V_S < 30$ V [1], $T_A = -40$ to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Operational Amplifier						
Open-loop voltage gain	G_{V0}	60	80		dB	
Input offset voltage	V_{IO}	– 10		10	mV	Pin 19 n.c.
Input current	$-I_{I\,op\,amp}$			2	µA	
Common-mode input voltage range	V_{IC}	0		4	V	
Output current	$I_{Q\,op\,amp}$	0		2	mA	
Output voltage range	V_Q	0.5		$V_{CR\,H}$	V	0 mA < I_Q < 2 mA
Transition frequency Transition phase	f_T ϕ_T		3 120		mHz deg.	
Temperature coefficient of V_{IO}	TC	– 30		30	µV/K	Pin 19 n.c.; V_{IC} = 3 V
Source current at Q Op Amp	$I_{op\,amp}$	70	100	130	µA	0.5 V < V_Q < $V_{CR\,H}$
Soft Start						
Charge current for $C_{soft\,start}$ Discharge current for $C_{soft\,start}$	I_{ch} I_{dch}	4 1	6 2	8 3.2	µA µA	
Upper limiting voltage Switching voltage of K2	V_{lim} V_{K2}	4.4 1.3	4.8 1.5	5.0 1.7	V V	

[1] $V_{S\,ON}$ means that $V_{S\,HIGH}$ has been exceeded, while $V_{S\,LOW}$ has not yet been undercut.

Characteristics (cont'd)
$V_{SON} < V_S < 30$ V [1], $T_A = -40$ to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Dynamic Current Limitation K5						
Input current Input offset voltage	$-I_{IDYN}$ V_{IO}	– 10		2 10	µA mV	
Common-mode input voltage range	V_{IC}	0		$V_S - 3$	V	
Turn-OFF delay time	t		250	400	ns [2]	Rated load 3 nF at QSIP
Undervoltage K4						
Input current at K4	$-I_{IK4}$			0.2	µA	
Switching voltage at K4	V_{sw}	V_{REF} – 0.01		V_{REF} + 0.01	V	
Hysteresis current	$I_{Hy\,4\,H}$ $I_{Hy\,4\,L}$	11	17	22 0.1	µA µA	$V_{(+K4)} < V_{sw}$ $V_{(+K4)} > V_{sw}$
Turn-OFF delay time	t			3	µs [2]	
Overvoltage K3						
Input current	$-I_{IK3}$			0.2	µA	
Switching voltage	V_{sw}	V_{REF} – 0.01		V_{REF} + 0.01	V	
Turn-OFF delay time	t			3	µs [2]	
Hysteresis current	$-I_{Hy\,3\,H}$ $-I_{Hy\,3\,L}$	6	9	12 0.1	µA µA	$V_{(-K6)} > V_{sw}$ $V_{(-K6)} < V_{sw}$

1) $V_{S\,ON}$ means that $V_{S\,HIGH}$ has been exceeded, while $V_{S\,LOW}$ has not yet been undercut.
2) Step function $V_{REF} = -100$ mV ⌐► $V_{REF} = +100$ mV (for transit time from input comparator to Q SIP)

Characteristics (cont'd)
$V_{SON} < V_S < 40$ V [1], $T_A = -40$ to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output Driver QSIP 1/2						
H-output voltage	V_{QH}	$V_S - 3$			V	$I_{Q\,SIP} = -250$ mA; $V_S = V_{S\,Q\,SIP}$
L-output voltage	V_{QL}			2.1	V	$I_{Q\,SIP} = +250$ mA; $V_S = V_{S\,Q\,SIP}$
	V_{QL}			1.4	V	$I_{Q\,SIP} = +10$ mA; $V_S = V_{S\,Q\,SIP}$
Output current	$I_{Q\,SIP}$	500	700		mA [2]	$C_{Q\,SIP} = 10$ nF; $V_S = V_{S\,Q\,SIP} = 20$ V
	$-I_{Q\,SIP}$	300	500		mA [2]	
	$I_{Q\,SIP}$		600		mA [2]	$C_{Q\,SIP} = 10$ nF; $V_S = V_{S\,Q\,SIP} = 15$ V
	$-I_{Q\,SIP}$		500		mA [2]	
	$I_{Q\,SIP}$		400		mA [2]	$C_{Q\,SIP} = 10$ nF; $V_S = V_{S\,Q\,SIP} = 10$ V
	$-I_{Q\,SIP}$		400		mA [2]	
Input Standby IST						
Turn-ON threshold for V_{IST} rising	$V_{IST\,H}$	6.1	6.8	7.5	V	$V_S > V_{S\,ON}$; $T_A = 25$ °C
Temperature response	$\Delta V_{IST\,H}/\Delta T$		-0.023		%/K	
Turn-OFF threshold for V_{IST} falling	$V_{IST\,H}$	5.5	6.1	6.7	V	
Temperature response	$\Delta V_{IST\,L}/\Delta T$		0.047		%/K	
Hysteresis current	$-I_{Hy\,IST\,H}$			2	µA	$V_{IST} > V_{IST\,H}$
	$I_{Hy\,IST\,L}$	35	50	65	µA	$V_{IST\,L} \le V_{IST} \le V_{IST\,H}$; $T_A = 25$ °C
Temperature response	$\Delta I_{Hy\,IST}/\Delta T$		0.01		%/K	

[1] $V_{S\,ON}$ means that $V_{S\,HIGH}$ has been exceeded, while $V_{S\,LOW}$ has not yet been undercut.
[2] Dynamic maximum current during rising or falling edge.

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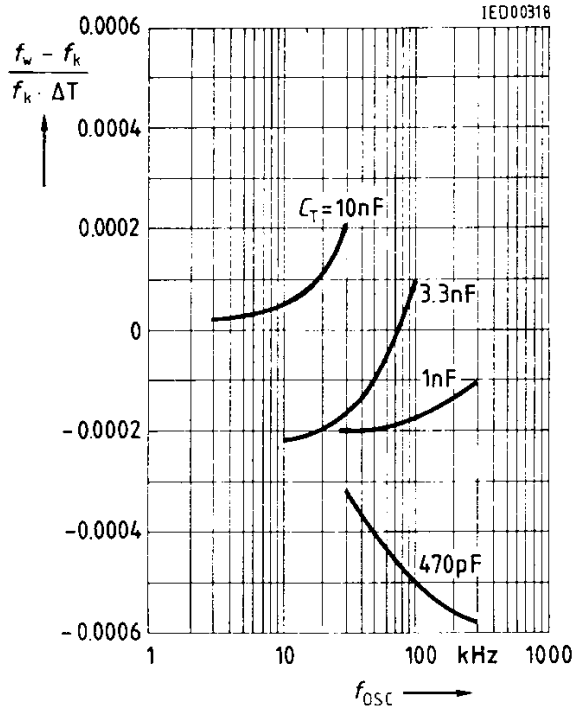
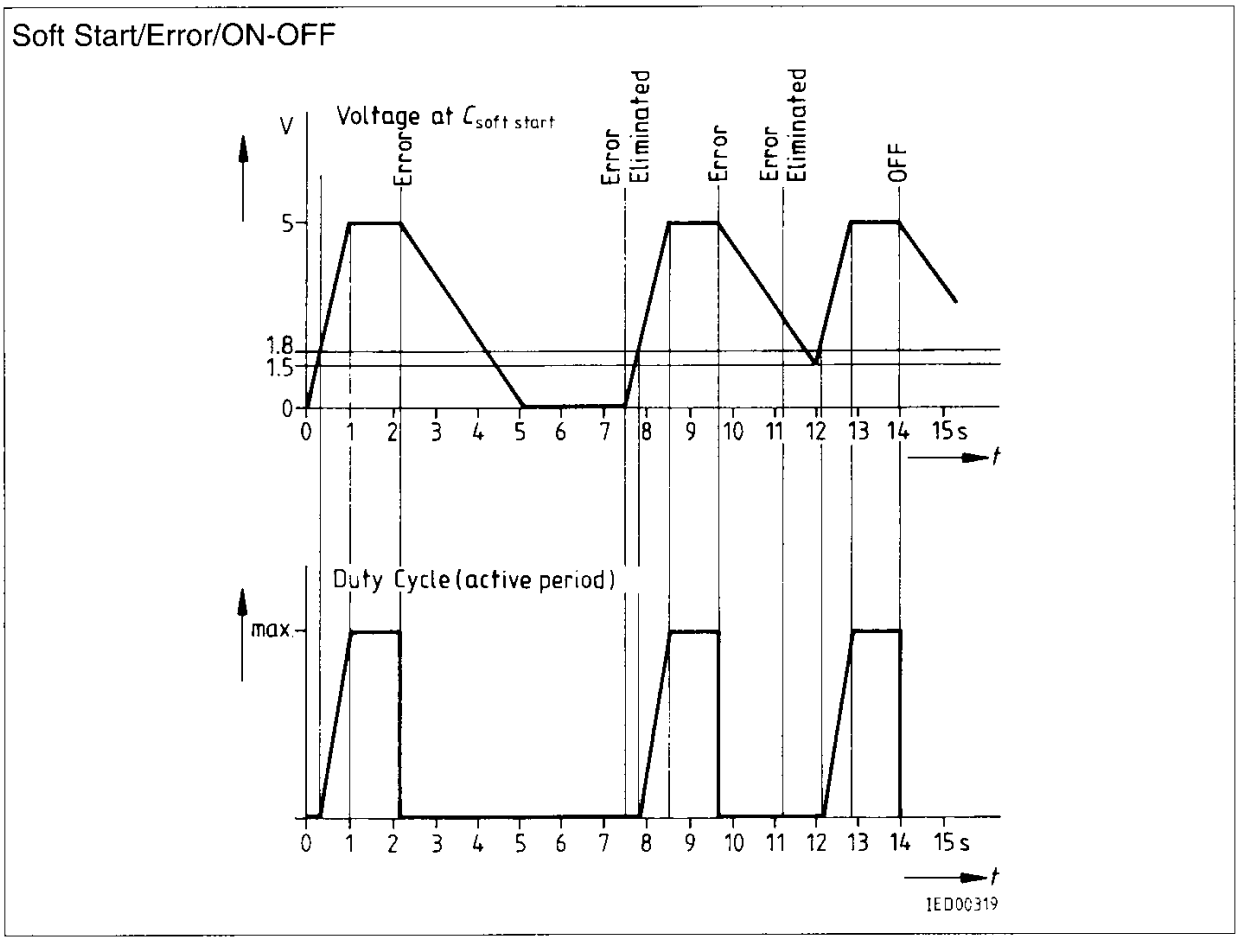
Diagrams

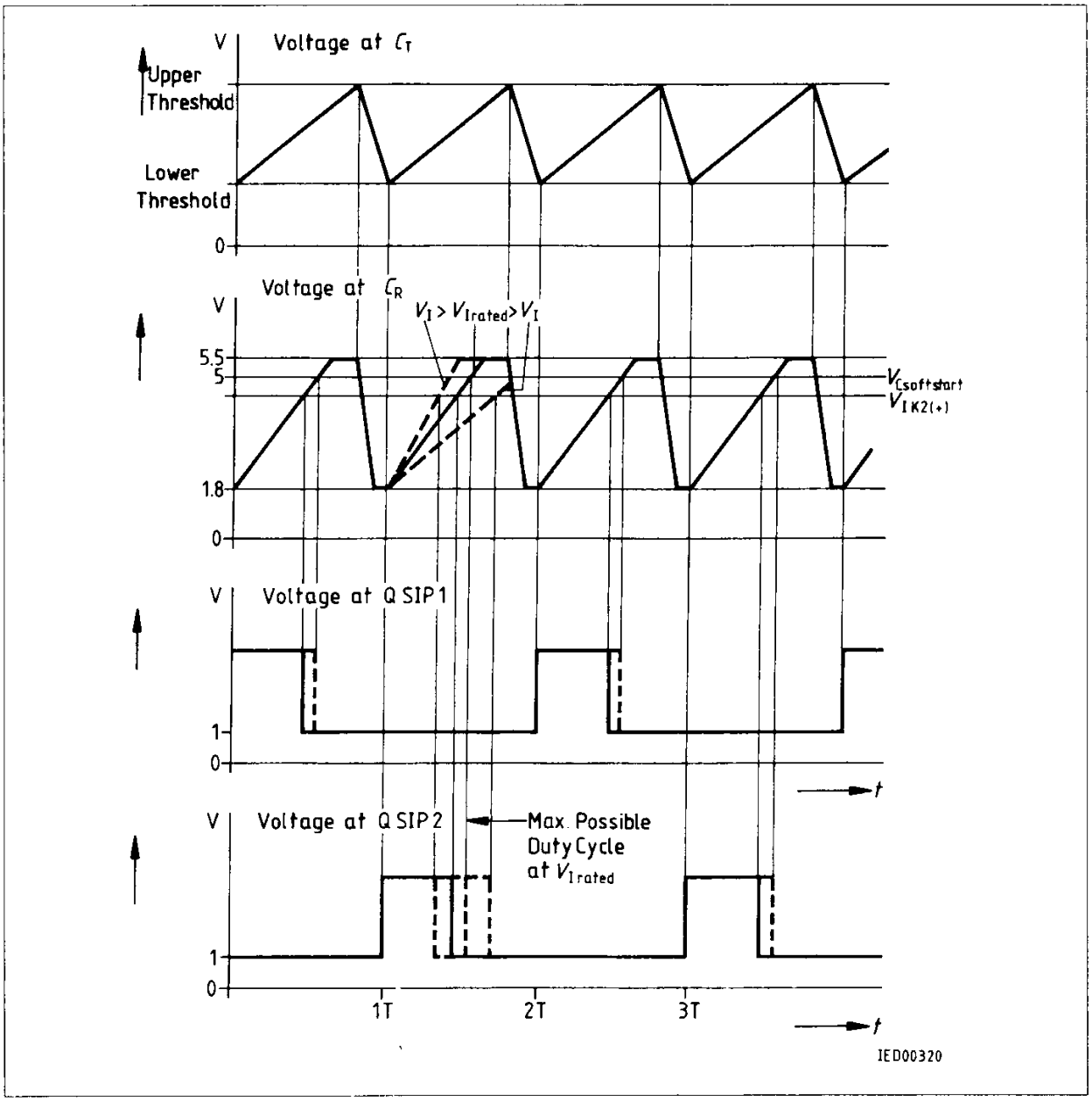
Typical temperature dependance of the frequency generator at different C_T values.



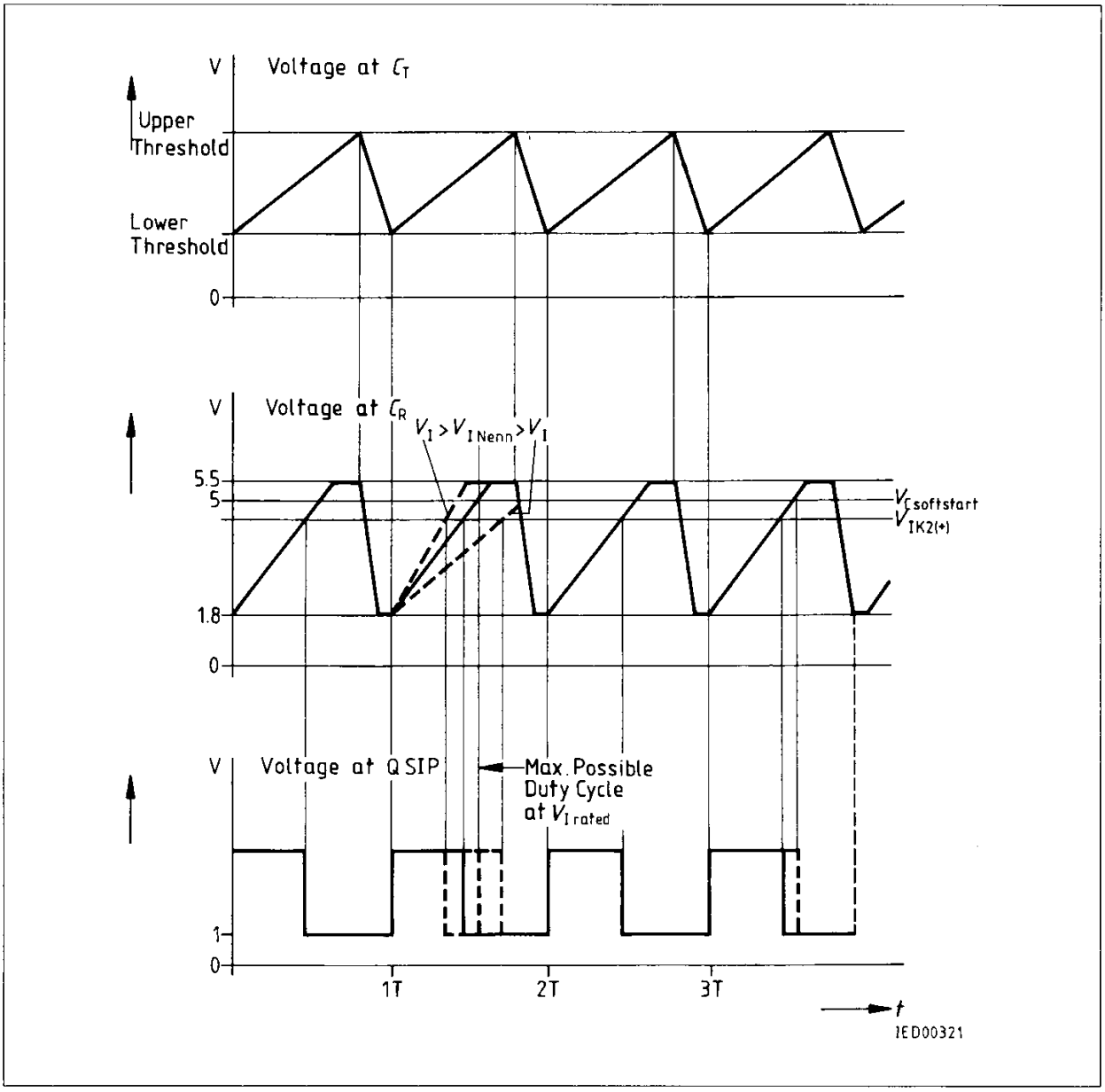
f_k = Frequency at room temperature
f_w = Frequency at thermal increase



Pulse Diagram



Pulse Diagram (TDA 4918)



Pulse Diagram (TDA 4919)

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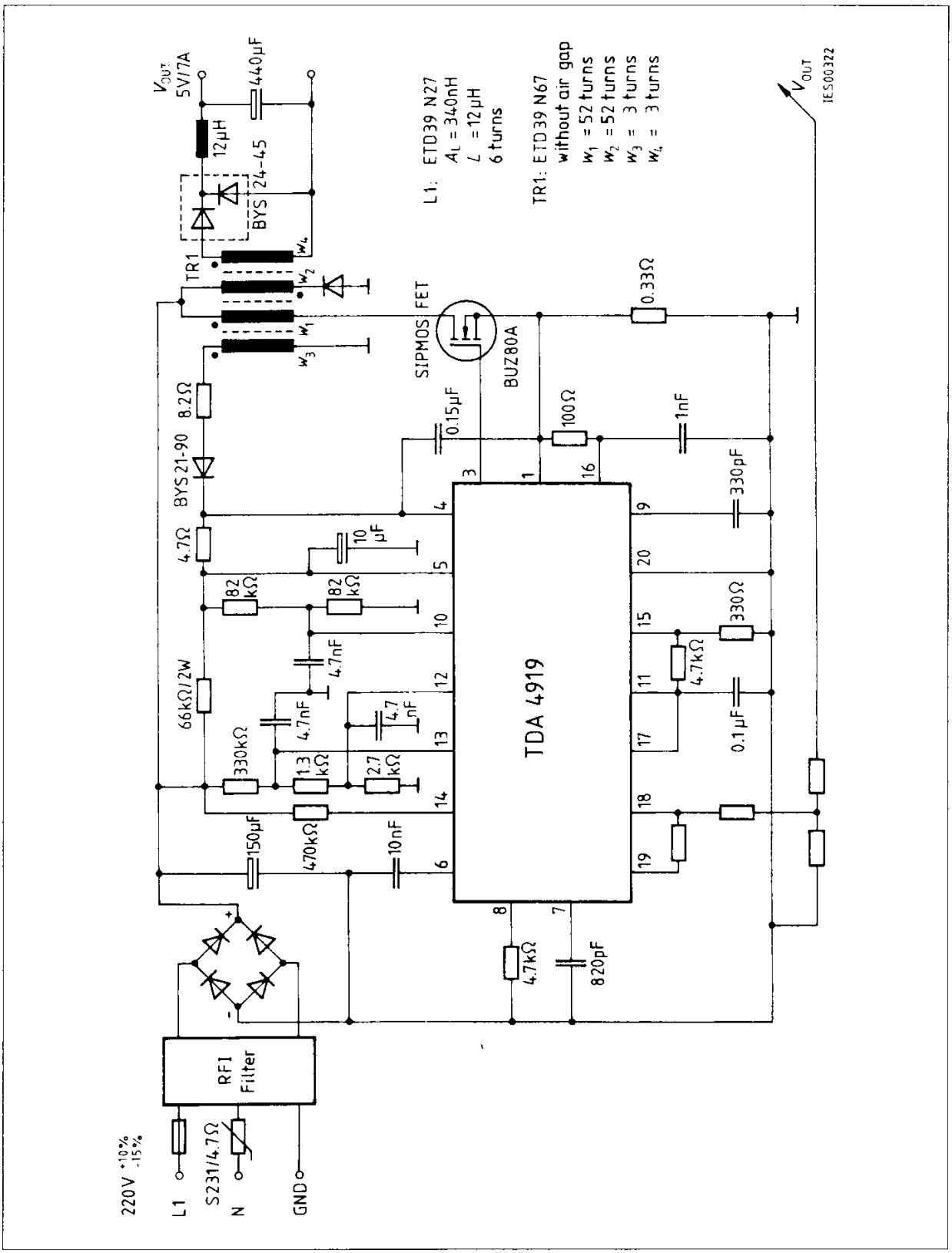

Application Circuit (TDA 4919)