SMALL SIGNAL COMBINATION IC FOR COLOUR TV

GENERAL DESCRIPTION

The TDA4505 is a TV sub-system circuit, for colour television receivers. For a complete colour television receiver only a tuner, a colour decoder and output stages are required.

Features

- Vision IF amplifier with synchronous demodulator
- Tuner AGC (negative going control voltage with increasing signal)
- AGC detector suited for negative modulation
- AFC circuit
- Video preamplifier
- Sound IF amplifier, demodulator and preamplifier
- DC volume control or separate supply for starting the oscillator
- Horizontal synchronization circuit with two control loops
- Vertical synchronization (divider system) and sawtooth generation with automatic amplitude adjustment for 50 or 60 Hz mode
- Transmitter identification (mute)
- Three level sandcastle pulse generation

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 7)	V_{7-6}	9,5	12	13,2	V
Supply current (pin 7)	I_7	–	135	–	mA
Supply current (pin 11)	I_{11}	–	6	8,5	mA
Operating ambient temperature range	T_{amb}	–25	–	+ 65	°C
Storage temperature range	T_{stg}	–25	–	+ 150	°C
Total power dissipation	P_{tot}	–	–	2,3	W

PACKAGE OUTLINE

28-lead DIL; plastic (with internal heat spreader) (SOT117).

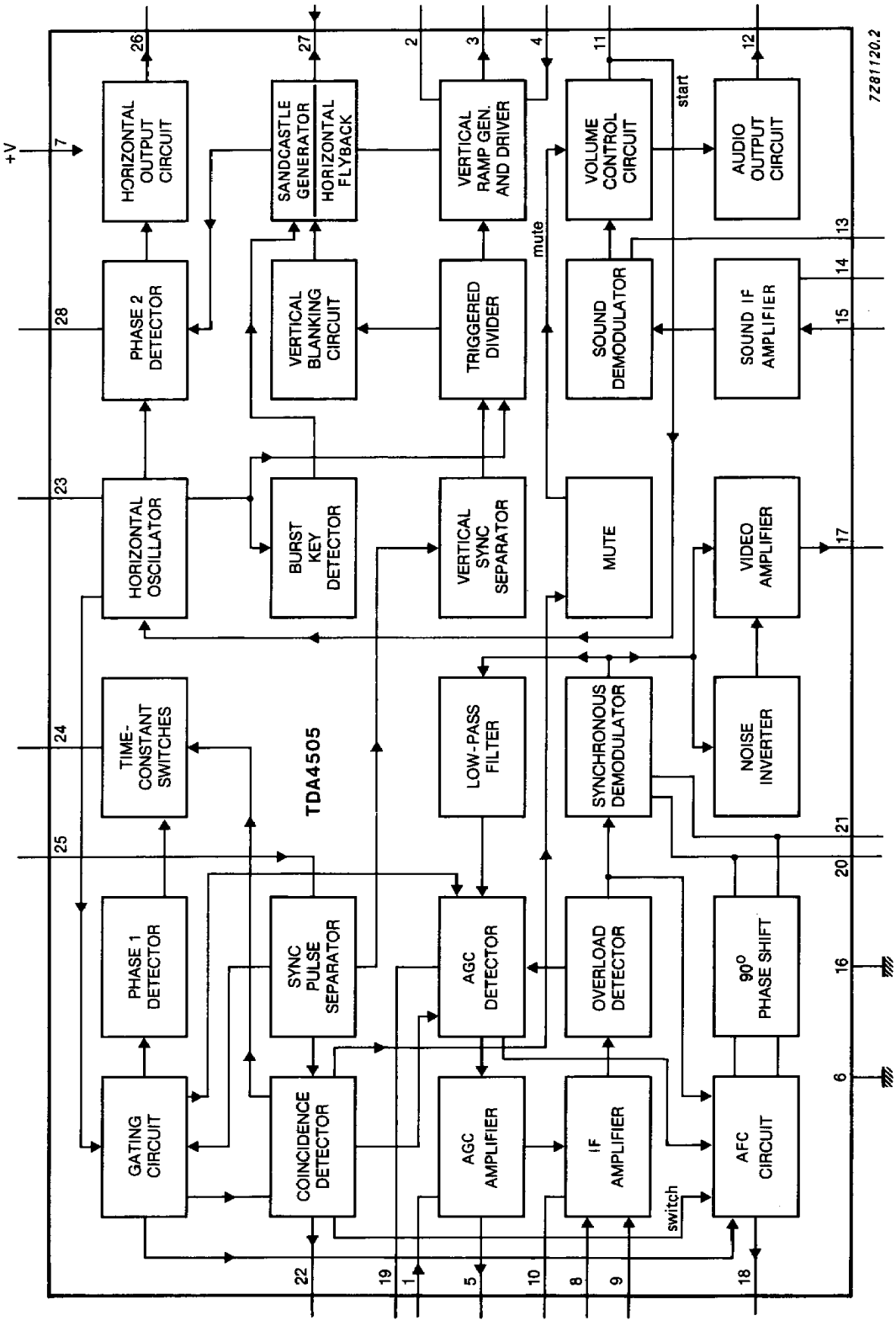


Fig. 1 Block diagram.

PINNING

1. AGC take over
2. Vertical ramp generator
3. Vertical drive
4. Vertical feedback
5. Tuner AGC
6. Ground
7. Supply
8. Vision IF input
9. Vision IF input
10. Decoupling capacitor
11. Volume control/start horizontal oscillator
12. Audio output
13. Sound demodulator
14. Sound IF decoupling
15. Sound IF input
16. Ground
17. Video output
18. AFC output
19. AGC detection
20. Synchronous demodulator
21. Synchronous demodulator
22. Coincidence detector decoupling
23. Horizontal oscillator
24. Phase 1 detector
25. Sync separator
26. Horizontal drive
27. Sandcastle output/flyback input
28. Phase 2 detector

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

IF amplifier, demodulator and AFC

The IF amplifier has a symmetrical input (pins 8 and 9). The synchronous demodulator and the AFC circuit share an external reference tuned circuit (pins 20 and 21). An internal RC-network provides the necessary phase-shift for AFC operation. The AFC circuit is gated by an internally generated gating pulse. As a result the AFC output voltage contains no video information. The AFC circuit provides a control voltage output with a swing greater than 10 V at pin 18.

AGC circuit

Gating of the AGC detector is performed to reduce sensitivity of the IF amplifier to external electrical noise. The AGC time constant is provided by an RC-circuit connected to pin 19. The point of tuner take-over is preset by the voltage level at pin 1.

Video amplifier

The signal through the video amplifier comprises video and sound information.

Sound circuit and horizontal oscillator starting function

The input to the sound IF amplifier is obtained by a bandpass filter coupling from the video output (pin 17). The sound is demodulated and passed via a dual-function volume control stage to the audio output amplifier. The volume control function is obtained by connecting a variable resistor (4,7 kΩ) between pin 11 and ground, or by supplying pin 11 with a variable voltage. Sound output is suppressed by an internal mute signal when no TV signal is identified.

DC volume control/Horizontal oscillator start

The circuit can be used with a DC volume control or with a starting possibility of the horizontal oscillator. The operation depends on the application. When during switch-on no current is supplied to pin 11 this pin will act as volume control. When a current of 6 mA is supplied to pin 11 the volume control is set to a fixed output signal and the IC will generate drive pulses for the horizontal deflection. The main supply of the IC can then be derived from the horizontal deflection.

FUNCTIONAL DESCRIPTION (continued)

Horizontal synchronization

The video input signal (positive video) is connected to pin 25.
The horizontal synchronization has two control loops. This has been introduced to generate a sand-castle pulse. Using the oscillator sawtooth facilitates accurate timing of the burst key pulse. Therefore, the phase of this sawtooth must have a fixed relationship to the sync pulse, which is achieved by use of a second loop.

Horizontal phase detector

The circuit has the following operating conditions.

(a) Strong input signal, synchronized or not synchronized.
(The input signal condition is obtained from the AGC-circuit, the in-sync./out-of-sync from the coincidence detector). In this condition the time constant is optimal for VCR-playback i.e.; fast time constant during the vertical retrace (to be able to correct head-errors of the VCR) and such a time constant during scan that fluctuations of the sync. are corrected. The phase detector is not gated.

(b) Weak signal.
In this condition the time constant is doubled compared to condition (a). Also the phase detector is gated when the oscillator is synchronized. This ensures a stable display which is not disturbed by the noise in the video signal.

(c) Not synchronized (weak signal).
In this condition the time constant during scan and vertical retrace are the same as during scan in condition (a).

Vertical sync pulse

The vertical sync pulse integrator will not be disturbed when the vertical sync pulses have a width of only 10 μs with a separation of 22 μs. This type of vertical sync pulses are generated by video tapes with anti-copy guard.

Vertical divider system

The TDA4505 embodies a synchronized divider system for generating the vertical sawtooth at pin 2.
The divider system has an internal frequency doubling circuit, which allows the horizontal oscillator to operate at its normal line frequency. One line period equals 2 clock pulses.
Use of the divider system avoids the requirement for vertical frequency adjustment. The divider has a discriminator window for automatic switching from 60 Hz to 50 Hz mode. When the trigger pulse comes before line 576 the 60 Hz mode is selected, otherwise the 50 Hz mode is selected.
The divider system operates with 2 different divider reset windows for maximum interference/disturbance protection.
The windows are activated via an up/down counter.
The counter increases its counter value by 1 each time the separated vertical sync pulse is within the search window. When not within the search window this value is decreased by 1.
The operating modes of the divider system are as follows.

Mode A

Large (search) window (divider ratio between 488 and 722)

This mode is valid for the following conditions:

- Divider is looking for a new transmitter
- Divider ratio found – not within the narrow window limits
- Non-standard TV-signal condition detected while a double or enlarged vertical sync pulse is found after the internally generated anti-topflutter pulse has ended. This means a vertical sync pulse width > 8 clock pulses (50 Hz); > 10 clock pulses (60 Hz)
  Usually this mode is activated for video tape recorders operating in the feature trick mode
- Up/down counter value of the divider system operating in the narrow window mode drops below count 10

Mode B

Narrow window (divider ratio between 522 to 528; 60 Hz or 622 to 628; 50 Hz)

The divider system switches over to this mode when the up/down counter has reached its maximum value of 15 approved vertical sync pulses. When the divider operates in this mode and a vertical sync pulse is missing within the window, the divider is reset at the end of the window and the counter value is decreased by 1. At a counter value below 10 the divider system switches over the large window mode. The divider system also generates an anti-topflutter pulse which inhibits the Phase 1 detector during the vertical sync pulse. The pulse width is dependent on the divider mode. In Mode A the start is generated by reset of the divider. In Mode B the anti-topflutter pulse starts at the beginning of the first equalizing pulse.
The anti-topflutter pulse ends at count 10 for the 50 Hz mode and count 12 for the 60 Hz mode.
The vertical blanking pulse is also generated via the divider system. The start is by reset of the divider while the blanking pulse width is 34 (17 lines) for the 60 Hz mode and at count 42 (21 lines) for the 50 Hz mode. The vertical blanking pulse at the sandcastle output (pin 27) is generated by adding the anti-topflutter pulse to the blanking pulse. Thus the vertical blanking pulse starts at the beginning of the first equalizing pulse when the divider operates in Mode B. The length of the vertical blanking in this condition is 21 lines in the 60 Hz mode and 25 lines in the 50 Hz mode.

DEVELOPMENT DATA

Application when external video signals require synchronization

The input to the sync separator is externally available via pin 25. For normal application the video output signal at pin 17 is AC coupled to this input as shown in Fig. 10. It is possible to interrupt this connection and drive the sync separator from other sources such as:

- a teletext decoder in serial mode
- an external audio signal via a peritelevision connector

When a teletext decoder is applied the IF amplifier and synchronization circuit are operating in the same phase which allows various connections between the two parts (i.e. AGC gating) can remain active. When external signals are applied to the sync separator the connections between the two parts must be interrupted. This can be achieved by connecting pin 22 to ground, which results in the following conditions:

- AGC detector is not gated
- AFC circuit is active
- Mute circuit not active – sound channel remains switched on
- Phase detector 1 has an optimal time constant for external video sources

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 7)	$V_P = V_{7-6}$	–	13,2	V
Total power dissipation	P_{tot}	–	2,3	W
Operating ambient temperature range	T_{amb}	–25	+ 65	°C
Storage temperature range	T_{stg}	–25	+ 150	°C

CHARACTERISTICS

$V_P = V_{7-6} = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 7)		V_{7-6}	9,5	12	13,2	V
Supply current (pin 7)		I_7	–	135	–	mA
Supply current (pin 11) for horizontal oscillator start	note 1	I_{11}	–	6	8,5	mA
Vision IF amplifier (pins 8 and 9)						
Input sensitivity at 38,9 MHz	on-set AGC	V_{8-9}	60	130	180	μA
Input sensitivity at 45,75 MHz	on-set AGC	V_{8-9}	–	140	–	μA
Differential input resistance (pin 8 to 9)		R_{8-9}	800	1300	1800	Ω
Differential input capacitance (pin 8 to 9)		C_{8-9}	–	5	–	pF
Gain control range		G_{8-9}	–	63	–	dB
Maximum input signal		V_{8-9}	50	180	–	mV
Expansion of output signal for 40 dB variation of input signal with V_{8-9} at 300 μV, 0 dB)		ΔV_{17-6}	–	1	–	dB
Video amplifier						
Measured at top sync input signal voltage (rms value) of 10 mV						
Output level for zero signal input (zero point of switched demodulator)		V_{17-6}	5,4	5,8	6,2	V
Output signal top sync level	note 2	V_{17-6}	2,7	2,9	3,1	V
Amplitude of video output signal (peak-to-peak value)		$V_{17-6(p-p)}$	2,3	2,6	2,9	V

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Internal bias current of output transistor (npn emitter follower)		$I_{17(int)}$	1,4	2,0	–	mA
Bandwidth of demodulated output signal		B	4	4,5	–	MHz
Differential gain	note 3	G_{17}	–	4	10	%
Differential phase	note 3	φ	–	3	10	deg
Video non-linearity	note 4	NL	–	4	10	%
Intermodulation with input signal of 10 mV(rms)	see Fig. 2 and Fig. 5					
f = 1,1 MHz (blue)			50	55	–	dB
f = 1,1 MHz (yellow)			48	52	–	dB
f = 3,3 MHz (blue)			50	55	–	dB
f = 3,3 MHz (yellow)			50	55	–	dB
Signal-to-noise ratio	Z_S = 75 Ω; note 5					
V_i = 10 mV		S/N	45	50	–	dB
end of gain control range		S/N	50	55	–	dB
as a function of the input signal		S/N	see Fig. 6			
Residual carrier signal			–	7	30	mV
Residual 2nd harmonic of carrier signal			–	24	40	mV
Tuner AGC	note 6					
Minimum starting point take-over (rms value)		$V_{1-6(rms)}$	–	–	0,5	mV
Maximum starting point take-over (rms value)		$V_{1-6(rms)}$	50	180	–	mV
Maximum output swing		$I_{5(max)}$	6	10	–	mA
Output saturation voltage	I_5 = 2 mA	$V_{5-6(sat)}$	–	100	300	mV
Leakage current		I_5	–	0,7	1	μA
Input signal variation complete tuner control		ΔV_i	0,2	2,0	5,0	dB
AFC circuit (pin 18)	note 7					
AFC output voltage swing (peak-to-peak value)		$V_{18-6(p-p)}$	9,2	10	11,5	V
Available output current		$\pm I_{18}$	–	2,8	–	mA
Control steepness			35	50	70	mV/kHz
Output voltage at nominal tuning of the reference tuned circuit		V_{18-6}	–	6	–	V
Offset current AFC output (pins 20 and 21 short-circuited)		I_{18}	–	0	± 100	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Sound circuit						
Input limiting voltage	$V_o = V_{o(max)} = 3$ dB; $Q_L = 16$; $f_{AF} = 1$ kHz; $f_c = 5{,}5$ MHz	V_{15-6}	–	400	800	μA
Input resistance	$V_{i(rms)} = 1$ mV	R_{15}	–	2,6	–	kΩ
Input capacitance	$V_{i(rms)} = 1$ mV	C_{15}	–	6	–	pF
AM suppression (Figs 7 and 8)	$V_i = 10$ mV	AMS	–	46	–	dB
	$V_i = 50$ mV	AMS	–	50	–	dB
AF output signal (rms value)	$\Delta f = 7{,}5$ kHz; minimum distortion; maximum volume control	$V_{12-6(rms)}$	400	600	800	mV
AF output signal pin 11 as starting pin (rms value)	$\Delta f = 50$ kHz; $V_{11-6} > 10{,}5$ V	$V_{12-6(rms)}$	300	700	1400	mV
AF output impedance		Z_{12}	–	25	100	Ω
Total harmonic distortion	volume control 20 dB; $\Delta f = 7{,}5$ kHz	THD	–	1	3	%
Ripple rejection	volume control 20 dB; $f_k = 100$ Hz	RR	–	27	–	dB
	when muted	RR	–	30	–	dB
Output voltage in mute condition		V_{12-6}	–	3,0	–	V
Signal-to-noise ratio	$\Delta f = 27{,}5$ kHz; weighted noise in accordance with CCIR 468	S/N	–	56	–	dB
Volume control	see Fig. 9					
Output voltage	pin 11 open-circuit	V_{11-6}	–	5,5	7,0	V
Output current	pin 11 short-circuit	I_{11}	–	0,9	1,5	mA
External control resistor		R_{11}	–	4,7	–	kΩ
Suppression output signal during mute condition		OSS	60	66	–	dB

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Sync separator and first control loop						
Required sync pulse amplitude (peak-to-peak value)	R_{17-25} = 1,8 kΩ; note 8	$V_{25-6(p-p)}$	200	800	–	mV
Input current	$V_{25-6} > 5$ V	I_{25}	–	8,5	–	μA
	$V_{25-6} = 0$ V	I_{25}	–	10	–	mA
Holding range PLL		± Δf	–	1100	1500	Hz
Catching range PLL		± Δf	600	1000	–	Hz
Second control loop (positive edge)						
Control sensitivity		Δ_{td}/Δ_{to}	–	50	–	
Control range		t_d	–	25	–	μs
Phase adjustment (via second control loop)						
Control sensitivity			–	25	–	μA/μs
Maximum allowed phase shift		α	–	± 2	–	μs
Horizontal oscillator (pin 23)	note 9					
Free running frequency	R = *; C = 2,7 nF	f_{fr}	–	15625	–	Hz
Spread with fixed external components		Δf	–	0,4	4	%
Frequency variation due to change of supply voltage from 9,5 to 13,2 V		Δf_{fr}	–	0,2	0,5	%
Frequency variation with temperature		TC	–	–	1,6	Hz/K
Maximum frequency shift		Δf_{fr}	–	4	10	%
Maximum frequency deviation at start horizontal output		Δf_{fr}	–	8	10	%
Horizontal output (pin 26)						
Output voltage high level		V_{26-6}	–	–	13,2	V
Output voltage at which protection commences		V_{26-6}	–	13,2	15,8	V
Output voltage LOW	I_{26} = 10 mA	V_{26-6}	–	0,15	0,5	V
Duty cycle of horizontal output signal	t_p = 10 μs	d	–	0,45	–	
Rise time of output pulse		t_r	–	300	370	ns
Fall time of output pulse		t_f	–	120	240	ns

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Horizontal flyback input and sandcastle output	note 10					
Input current required during flyback pulse		I_{27}	0,1	–	2,0	mA
Output voltage						
during burst key pulse		V_{27-6}	8,4	9,0	–	V
during horizontal blanking		V_{27-6}	4,1	4,4	5,0	V
during vertical blanking		V_{27-6}	2,1	2,4	2,7	V
Pulse width						
burst key pulse	60 Hz	t_W	3,1	3,5	3,9	µs
burst key pulse	50 Hz	t_W	3,5	3,8	4,4	µs
horizontal blanking pulse			flyback pulse width			
vertical blanking pulse						
50 Hz divider in search window			–	21	–	lines
60 Hz divider in search window			–	17	–	lines
50 Hz divider in narrow window			–	25	–	lines
60 Hz divider in narrow window			–	21	–	lines
Delay between start of sync pulse at video output and falling edge of burst key pulse for NTSC signals			–	–	9,2	µs
Coincidence detector mute output	note 11					
Voltage for in-sync condition		V_{22-6}	9,5	10,3	11	V
Voltage for no-sync condition	no signal	V_{22-6}	1,2	1,45	2,2	V
Switching level to switch off AFC		V_{22-6}	–	6,4	–	V
Hysteresis AFC switch		V_{22-6}	–	0,4	–	V
Switching level to activate mute function (transmitter identification)		V_{22-6}	2,25	2,4	2,75	V
Hysteresis MUTE function		V_{22-6}	–	0,5	–	V
Charge current (peak-to-peak value)	in-sync 4,7 µs	$I_{22(p-p)}$	0,7	1,0	–	mA
Discharge current (peak-to-peak value)	in-sync 1,0 µs	$I_{22(p-p)}$	–	0,5	–	mA
Required voltage to allow synchronization of circuit with signals which have no relation to the video output signal		V_{22-6}	–	1,0	1,2	mA

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Vertical ramp generator	note 12					
Input current during scan		I_2	–	0,5	2,0	μA
Discharge current during retrace		I_2	0,3	0,35	0,4	mA
Sawtooth amplitude (peak-to-peak value)		$I_{2\text{-}6(p\text{-}p)}$	–	0,8	1,1	V
Vertical drive output (pin 3)						
Maximum available output current		I_3	1,5	3,0	–	mA
Maximum output voltage	I_3 = 1,5 mA	$V_{3\text{-}6}$	–	4,0	–	V
Vertical feedback input (pin 4)						
Input voltage DC component		$V_{4\text{-}6}$	2,9	3,3	3,7	V
AC component (peak-to-peak value)		$V_{4\text{-}6(p\text{-}p)}$	–	1,3	–	V
Input current		I_4	–	–	12	μA
Internal precorrection to sawtooth		Δt_p	–	6	–	%
Deviation amplitude	50/60 Hz		–	–	2	%
Vertical guard	note 13					
Active at a deviation with respect to the DC feedback level	$V_{27\text{-}6}$ = 2,5 V					
switching level LOW		$\Delta_{4\text{-}6}$	–	−1,3	–	V
switching level HIGH		$\Delta_{4\text{-}6}$	–	+1,9	–	V

Notes to the characteristics

1. Pin 11 has a double function. When during switch-on a current of 6 mA is supplied to this pin, which is used to start the horizontal oscillator. The main supply can then be obtained from the horizontal deflection stage. When no current is supplied to this pin it can be used as volume control. The indicated maximum value is the current at which all ICs will start. Higher currents are allowed, the excess current is bypassed to ground.
2. Signal with negative going sync, top white 10% of the top sync amplitude.
3. Measured according the test line shown in Fig. 3:
   - The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier at blanking level.
   - The differential phase is defined as the difference in degrees between the largest and smallest phase angle.
4. This figure is valid for the complete video signal amplitude (peak white-to-black); see Fig. 4.
5. Signal-to-noise ratio = $20 \log \frac{V_{\text{out black-to-white}}}{V_{n(\text{rms}) \text{ at } B = 5\,\text{MHz}}}$.
6. Tuner AGC; starting point tuner take-over at I = 0,2 mA. Take-over to be adjusted with a potentiometer of 47 kΩ. The voltage at pin 1 must not be reduced below 1 V.

Notes to the characteristics (continued)

7. The AFC control voltage is obtained by multiplying the IF output signal (which is also used to drive the synchronous demodulator) with a reference carrier. This reference carrier is obtained from the demodulator tuned circuit via a 90° phase shift network. The IF output signal has an asymmetrical frequency spectrum with respect to the carrier frequency. To avoid problems due to this asymmetrical signal the AFC circuit is gated by an internally generated gating pulse. As a result the detector is operative only during sync/black level at a constant carrier amplitude which contains no additional side bands. Thus the AFC output voltage contains no video information.
   At very weak input signals the drive signal for the AFC circuit will have a high noise content. The noise input has an asymmetrical frequency spectrum which will cause an offset of the AFC output voltage. To avoid problems due to this effect the AFC is switched off when the AGC is controlled to maximum gain.
   Values are measured with an input signal of 10 mV (rms) and the AFC output loaded with 2 x 470 kΩ between supply voltage and ground. The unloaded Q-factor of the reference tuned circuit is 70. The AFC is switched off when no signal is detected by the coincidence detector or when the voltage at pin 22 is between 1,2 V and 6,4 V. This can be realized by a resistor of 68 kΩ connected between pin 22 and ground.
8. The slicing level can be varied by changing the value of the resistance between pin 17 and pin 25. A higher resistance results in a larger value of the minimum sync pulse amplitude. The slicing level is independent of the video information.
9. Frequency control is obtained by supplying a correction current to the oscillator RC-network via a resistor, connected between the Phase 1 detector output and the oscillator network. The oscillator can be adjusted to the correct frequency by one of the two following methods:
   (a) Interrupt $R_{23\text{-}24}$.
   (b) Short-circuit the sync separator bias network (pin 25 to power supply).
   To avoid the necessity of a VCR switch, the time-constant of phase detector at strong input signal is sufficiently short to obtain a stable picture during VCR playback. During the vertical retrace period the time-constant is even shorter so that the head errors of the VCR are compensated at the beginning of the scan. During weak signal conditions (information derived from the AGC circuit) the time constant is increased to obtain a good noise immunity.
10. The horizontal flyback input and the sandcastle output have been combined on pin 27. The flyback pulse is clamped to a level of 4,9 V. The minimum current to drive the second control loop is 0,1 mA.
11. The functions in-sync/out-of-sync and transmitter identification have been combined on pin 22. The capacitor is charged during the sync pulse and discharged during the time difference between gating and sync pulse.
12. The vertical scan is synchronized by means of a divider system. Therefore no adjustment is required for the ramp generator. The divider detects whether the incoming signal has a vertical frequency of 50 or 60 Hz and corrects the vertical amplitude.
13. To avoid screenburn due to a collapse of the vertical deflection a continuous blanking level is inserted into the sandcastle pulse when the feedback voltage of the vertical deflection is not within the specified limits.

Where

SC = sound carrier
CC = chrominance carrier
PC = picture carrier

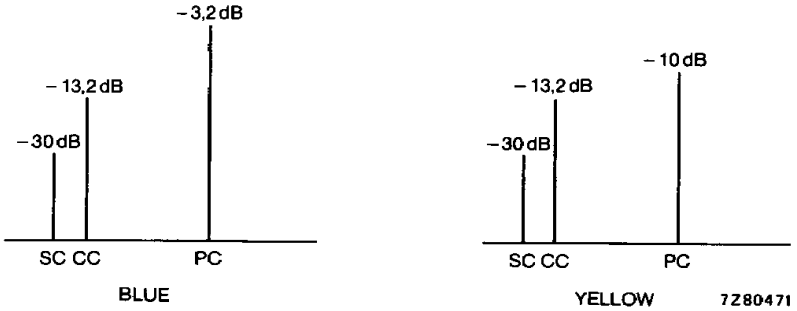


Fig. 2 Input signal conditions for intermodulation test; all values are with respect to the top sync level.

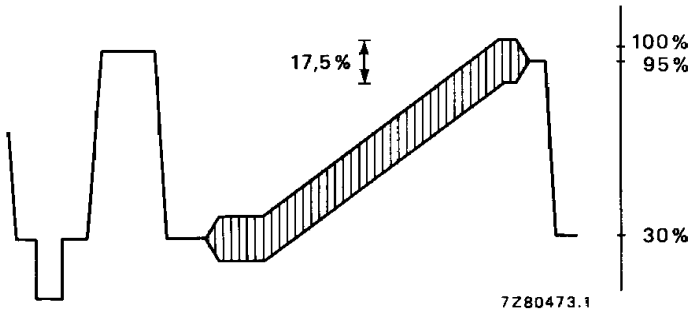


Fig. 3 Video output signal.

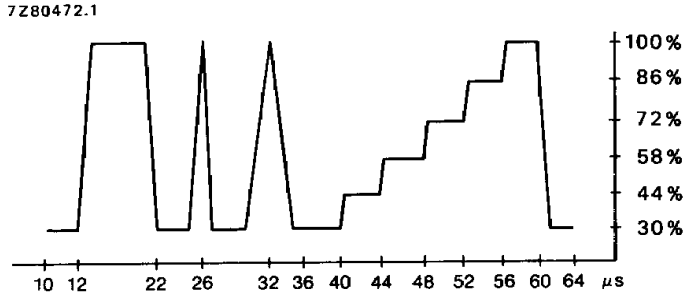
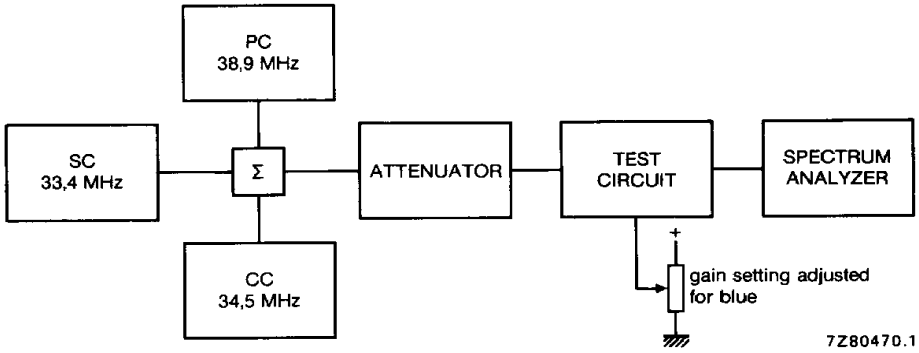


Fig. 4 European Broadcasting Union (EBU) test signal waveform (line 330).

DEVELOPMENT DATA



Where:

Value at 1,1 MHz: $20 \log \frac{V_o \text{ at } 4,4 \text{ MHz}}{V_o \text{ at } 1,1 \text{ MHz}} + 3,6 \text{ dB}$

Value at 3,3 MHz: $20 \log \frac{V_o \text{ at } 4,4 \text{ MHz}}{V_o \text{ at } 3,3 \text{ MHz}}$

Fig. 5 Test set-up intermodulation.

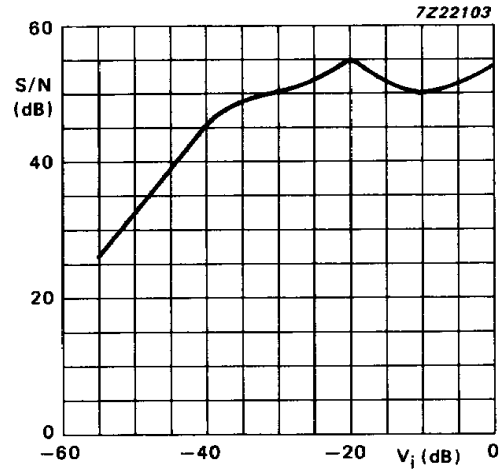


Fig. 6 Signal-to-noise ratio as a function of input voltage; 0 dB = 100 mV.

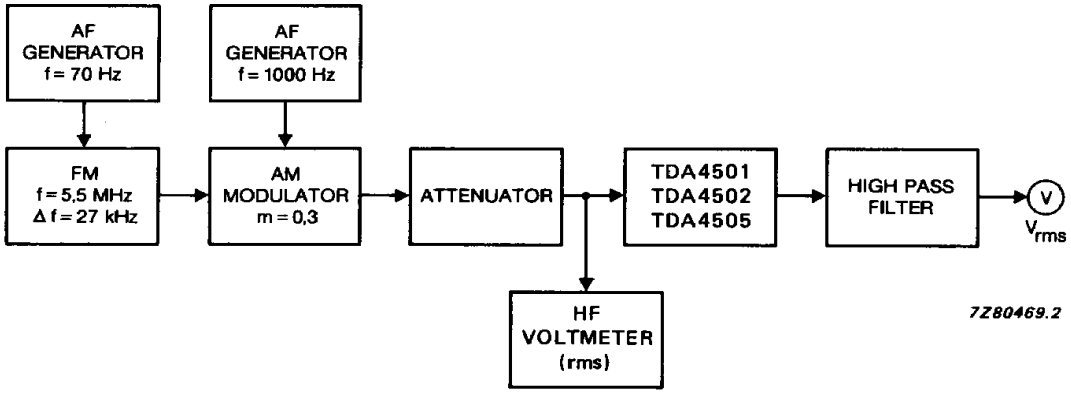


Fig. 7 Test set-up AM suppression.

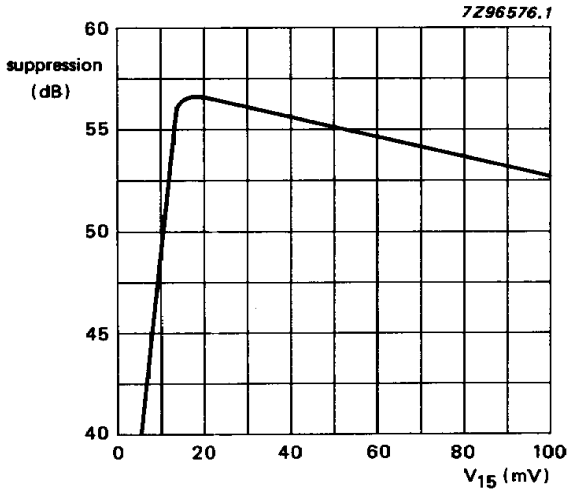


Fig. 8 AM suppression.

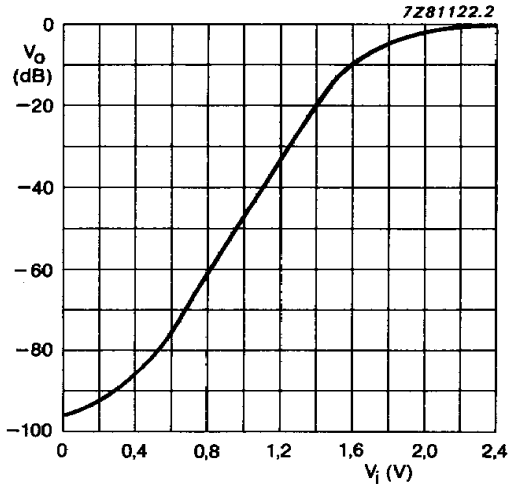


Fig. 9 Volume control characteristics.

APPLICATION INFORMATION

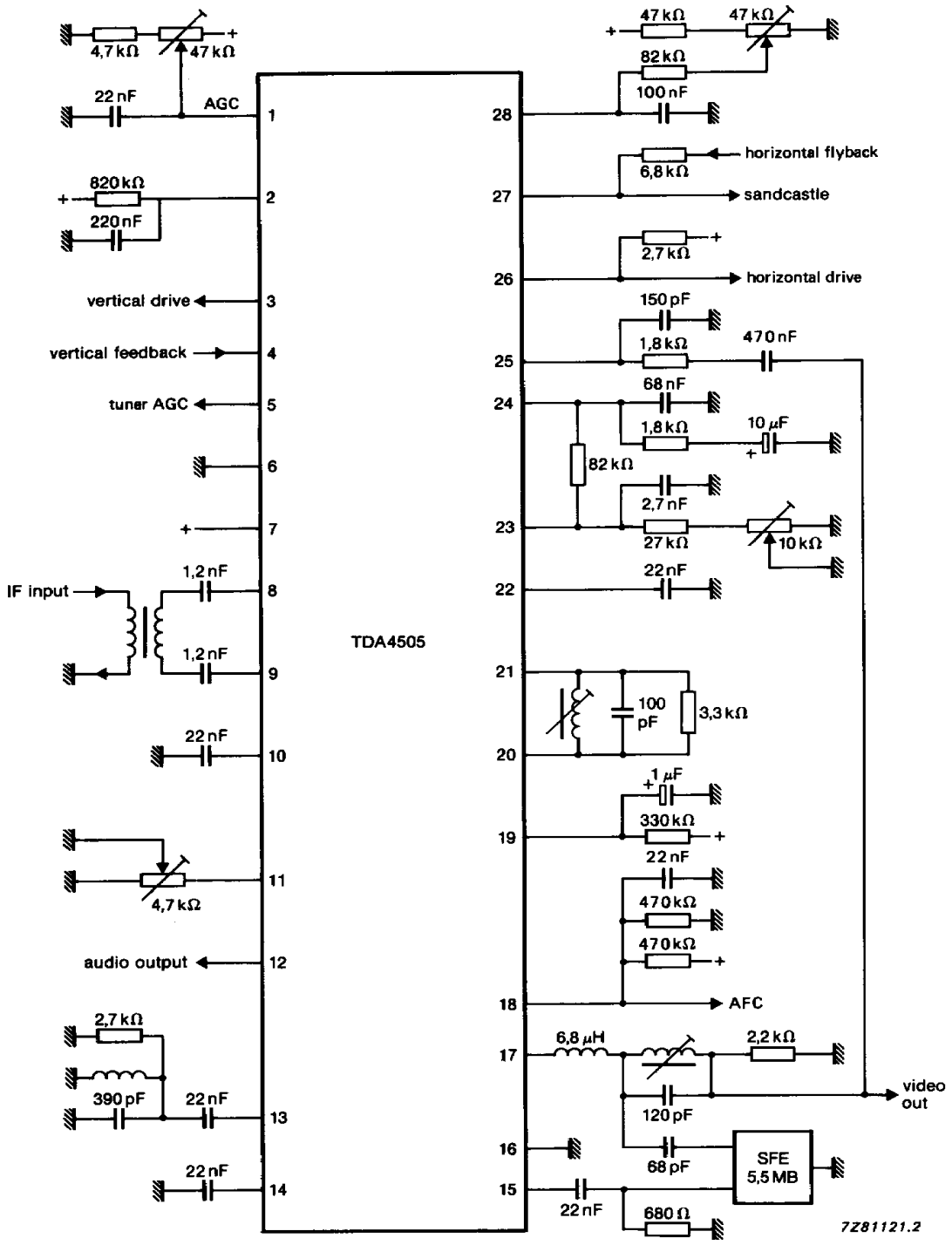


Fig. 10 Application diagram.

DEVELOPMENT DATA