Philips Semiconductors

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TDA4810

Sync processor and horizontal driver for monitors

FEATURES

- Sync separator with AC-coupled and DC-coupled inputs for signals of nearly all existing sync sources (e.g. TTL / video)
- Amplitude dependent sync slicing
- Automatic sync polarity correction
- Wide horizontal frequency range
- Artificial sync generator for sync pulse-width-independent operation
- Short vertical integration time
- Vertical/composite sync output signal selectable
- Super sandcastle pulse generator
- Two phase loops (PLL1, PLL2) to achieve excellent sync-locking and horizontal picture shift
- Horizontal output stage optimized for bipolar and Darlington deflection transistors
- Protection circuits against too low supply voltage and excessive EHT (X-ray protection)
- Voltage stabilizer with excellent ripple rejection
- Number of external components depend on the requirements and realized features

GENERAL DESCRIPTION

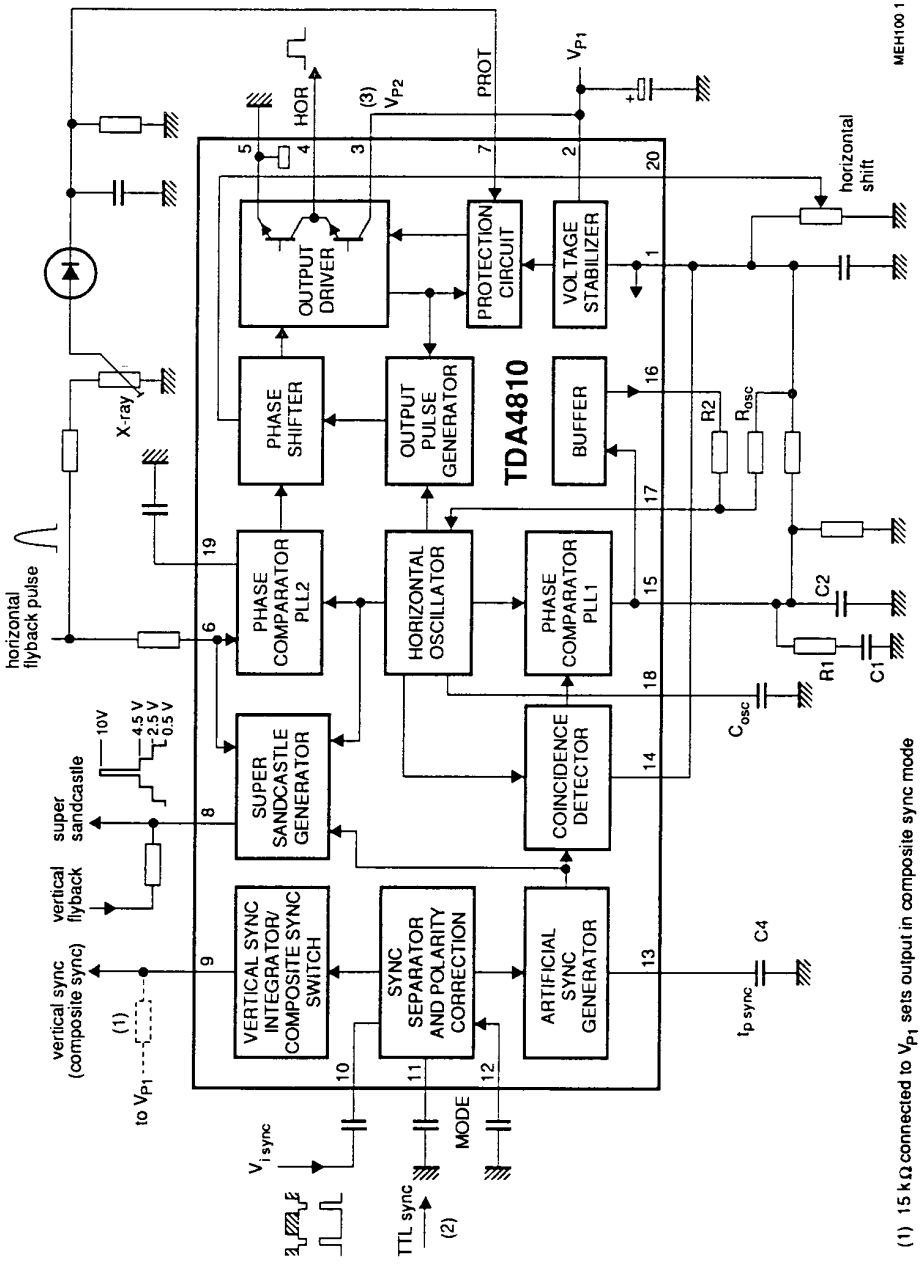
Monolithic integrated circuit for sync processing in monochrome and colour monitors, applicable for all commonly used graphic cards (e.g. EGA, Super VGA and IBM8514/A). The flexible sync separator handles different sync signals of either polarity over a wide amplitude range.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{P1}	supply voltage (pin 2)	8.5	12	16	V
V_{P2}	supply voltage (pin 3)	8.5	12	16	V
V_{stab}	stabilized output voltage (pin 1)	6.18	6.3	6.5	V
I_{P1}	supply current (pin 2)	-	35	-	mA
$V_{i\ sync}$	mode 1: AC-coupled negative-going input signal on pin 10 (peak-to-peak value)	-	1	1.5	V
	mode 2: AC-coupled positive- or negative-going sync pulse on pin 10 (peak-to-peak value)	2	-	5.5	V
	mode 3: DC-coupled positive- or negative-going sync pulse on pin 11 (peak value)	3.2	-	5.5	V
V_9	vertical/composite sync output voltage HIGH ($I_9 = -1$ mA)	-	10	-	V
I_4	maximum horizontal output current for Darlington deflection transistor ($-I_4 = I_3$)	-	-	−900	mA
	maximum horizontal output sink current for bipolar deflection transistor	-	-	100	mA

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4810	20	DIL	plastic	SOT146



(1) 15 kΩ connected to V_{P1} sets output in composite sync mode
(2) connection for other modes as described in Fig.3
(3) connection for Darlington deflection transistor as described in Fig.4

Fig.1 Block diagram for full facility (mode 2); horizontal output signal suitable for bipolar deflection transistor.

Sync processor and horizontal driver for monitors

TDA4810

PINNING

SYMBOL	PIN	DESCRIPTION
V_{stab}	1	stabilizer voltage output (6.3 V)
V_{P1}	2	supply voltage
V_{P2}	3	supply voltage for horizontal output
HOR	4	horizontal pulse output
GND	5	ground (0 V)
FLB	6	horizontal flyback pulse input
PROT	7	protection input (for over-current /EHT protection)
SSC	8	super sandcastle generator output
VS	9	vertical sync / composite sync output
$V_{i\ sync}$	10	sync input signal , AC-coupled
TTL	11	alternative sync input DC-coupled, e.g. TTL
APC	12	automatic sync polarity correction
C_{SY}	13	capacitor of artificial sync generator
COIN	14	coincidence detector
PLL1	15	time constant of PLL1
BUF	16	buffered PLL1 output
R_{osc}	17	reference current of horizontal oscillator
C_{osc}	18	capacitor of horizontal oscillator
PLL2	19	time constant of PLL2
SHIFT	20	horizontal phase shift

PIN CONFIGURATION

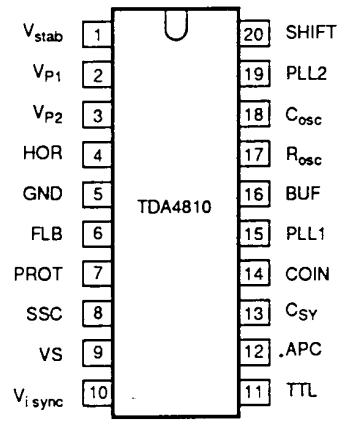


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Sync separator and polarity correction (Fig.1)

The circuit handles sync signals of nearly all existing standards . Features of the sync separator:

- inputs for DC-coupled signal or AC-coupled signal
- automatic sync polarity correction
- amplitude dependent sync slicer

The type of coupling and the necessary external components are shown in Figure 3.

Mode 1: A negative going sync signal (V_i sync < 1.5 V (p-p)) is fed via a coupling capacitor to pin 10. The sync separator clamps the bottom of the input signal on 1.28 V. Sync is sliced 120 mV above. Since the automatic polarity correction does not work below 2 V (p-p), pins 11 and 12 are connected to ground.

Mode 2: Positive or negative going sync pulses >2 V(p-p) (e.g. TTL) are AC-coupled to pin 10. The upper level is peak-rectified referred to the external capacitor on pin 11 at $V_{11} = 1.28V + 0.5 \times V_{i\ sync}$. This means, the slicing level tracks with typical 50% of $V_{i\ sync}$. The polarity switch corrects the polarity automatically by means of the external capacitor on pin 12. If only sync pulses of one polarity are applied to the input, the capacitor on pin 12 is not necessary. Then pin 12 can be connected to ground or V_{stab} (pin 1) to force the polarity.

Mode 3: Positive or negative going sync signals >3.2 V(p) (e.g. TTL) are DC-coupled to pin 11. They are sliced at 1.4 V according to TTL standard. If only sync pulses of one polarity are applied to the input, the capacitor on pin 12 is not necessary. Pin 12 can be connected to ground or V_{stab} (pin 1) to select the polarity from external.

Vertical/composite sync output

If a video signal or composite sync signal is applied to pin 10 the vertical sync separator generates a vertical sync trigger pulse. The separated vertical and composite sync pulses are fed to the vertical or composite sync switch and to the output stage (pin 9).

The external load current at pin 9 determines which of the two signals is fed out of pin 9. If there is an additional current from V_{P1} via the 15 kΩ resistor, composite sync signal is achieved (without additional current the vertical sync pulse is output.

Artificial sync generator

The sync signal from the sync separator is directly fed to the phase comparator (with unchanged leading and trailing edges), if the internal monoflop at pin 13 is connected to ground. This operation is possible.

Sync signals with leading edge as only sync reference (because the trailing edge could occur at an undefined time) is achieved by connecting a time-determining capacitor from pin 13 to ground. The internal monoflop generates an artificial sync signal triggered by the leading edge of the incoming sync signal.
Furthermore, the artificial sync generator reduces disturbances of the PLL1 during vertical sync.

Coincidence detector

Coincidence is detected between the input sync pulse and the gating pulse of the oscillator. The centring current for PLL1 is switched off at coincidence (V_{14} > 3 V).

Phase comparator PLL1

This stage compares the PLL1 (timing reference of the oscillator) with the centre of the horizontal input sync pulse (respectively with the artificial sync pulse, Fig.6). The time difference is converted into a proportional current on pin 15 to tune the oscillator via the buffer amplifier. This ensures that the phase relationship in the TDA4810 is stable independent of changes in frequency.

Horizontal oscillator (Fig.6)

The frequency of the free-running oscillator is determined by the capacitor on pin 18 and the reference current via pin 17. The reference current is fed from the voltage stabilizer via R_{osc}, and also from the PLL1 buffer amplifier via R2 to define the catching range. In order to cover a wide frequency range (one octave) R_{osc} can be modified as described in notes to the characteristics.

Phase comparator PLL 2 (Fig.6)

This stage compares the centre of the positive-going flyback pulse (on pin 6, internal threshold voltage 3 V) with the PLL2 timing reference generated by the horizontal oscillator. A time difference is converted into a proportional current on pin 19. The line flyback pulse and the oscillator pulse are compared to eliminate the delay time in the horizontal deflection stage.

Horizontal phase shifter

An external stabilized voltage on pin 20 sets the phase relationship between sync pulse and horizontal flyback pulse. The horizontal output pulse can be adjusted over a wide range (±20% referred to the horizontal period time) by means of the external potentiometer (Fig.1).

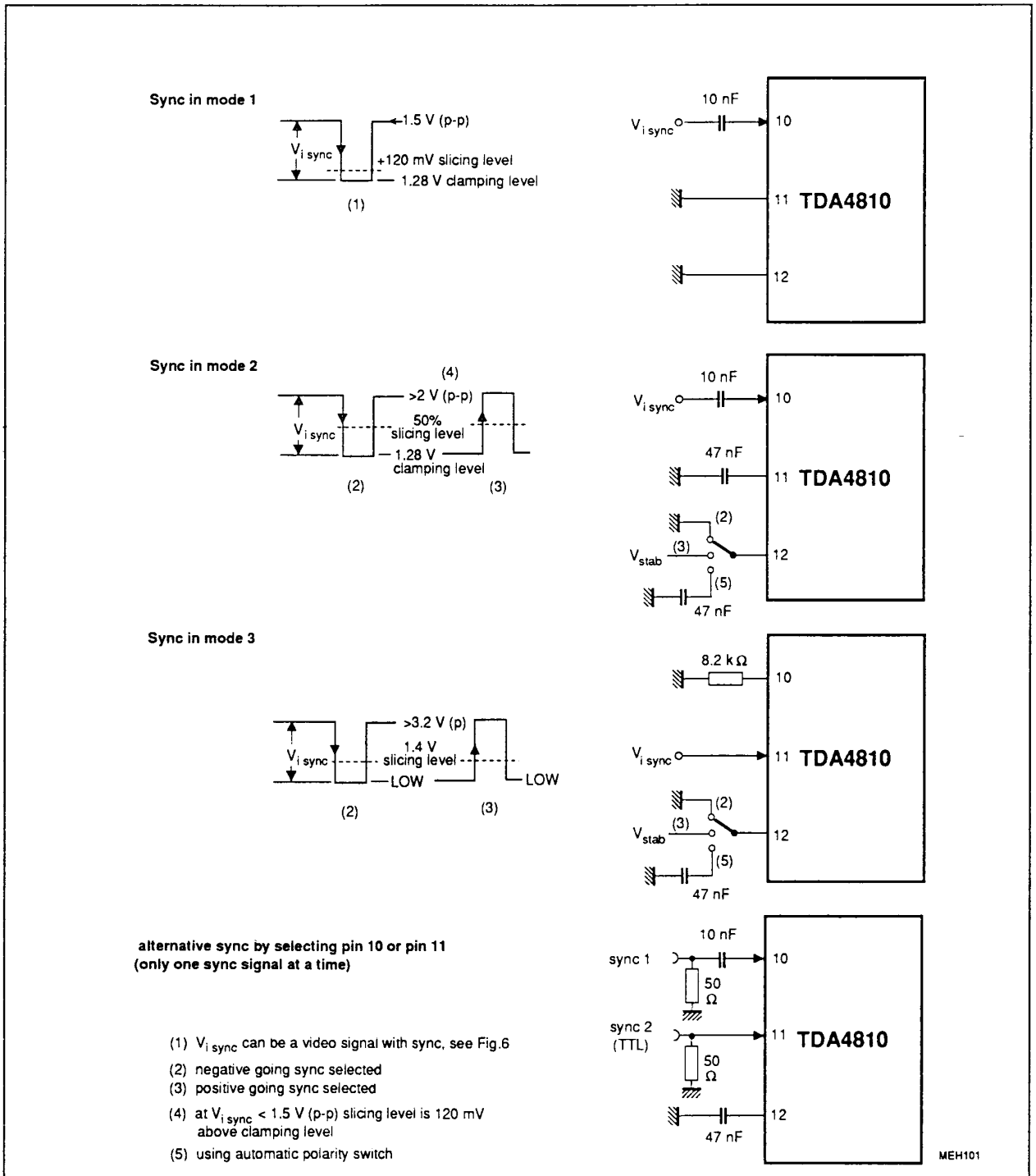


Fig.3 Sync modes of TDA4810.

Output pulse generator and horizontal output (Fig.4)

The output pulse generator generates a pulse of constant width within the control range of the PLL 2. The horizontal output driver generates two different pulse widths (Fig.6) depending on the voltage between pins 2 and 3

- 45% relative pulse width for standard bipolar deflection transistor ($V_3 = V_2$)
- 30% relative pulse width for Darlington deflection transistor. ($V_3 < V_2$)

NON-INVERTED POLARITY.

The push-pull output stage of the horizontal driver is connected between the supply voltage (pin 3) and ground (pin 5). The output signal (pin 4) is usually fed to a transformer-coupled driver. The upper transistor (collector on pin 3) is designed for a maximum current of 900 mA, the lower one for 100 mA.

INVERTED POLARITY

The horizontal output signal is now available on pin 3 by means of the 220 Ω pull-up resistor. Pin 4 is connected to ground. The open-collector output can directly drive a Darlington deflection transistor.

Voltage stabilizer

A stabilized voltage of 6.3 V, based on a bandgap reference, is provided on pin 1. This avoids phase jitter in deflection, caused by an insufficient filtered supply voltage. The excellent performance of the voltage stabilizer allows the TDA4810 to be driven directly by a switch mode power supply.

Super sandcastle pulse generator

Three levels are generated (Fig.6):

a) The 2.5 V level is generated by a external vertical blanking current which is fed into pin 8.

b) The 4.5 V level is derived from the line flyback pulse referred to a threshold of 0.3 V for horizontal blanking. When horizontal flyback pulses are absent, the 4.5 V level is inserted by the protection circuit to blank the screen continuously .

c) The 10 V level starts with the trailing edge of the sync pulse (respectively with artificial sync) and ends with a pulse, derived from the horizontal oscillator saw-tooth signal.

Protection circuit

The protection circuit is activated and the horizontal output is switched off when the voltage on pin 7 exceeds V_{stab} = 6.3 V or decreases below −0.2 V . One of these both thresholds can be used for X-ray protection or for over-current protection (Fig.1).

There is an additional protection against too low supply voltage (V_{P1}< 5.8 V).

Operations:

- output pin 4 goes to ground when $V_2 = V_3$ (e.g. in a bipolar deflection transistor application)
- output pin 3 goes to ground when $V_3 < V_2$ (e.g. in a Darlington deflection transistor application)
- the error indication is latched; therefore all the supply voltages must be switched off and on again, to enable the circuit.

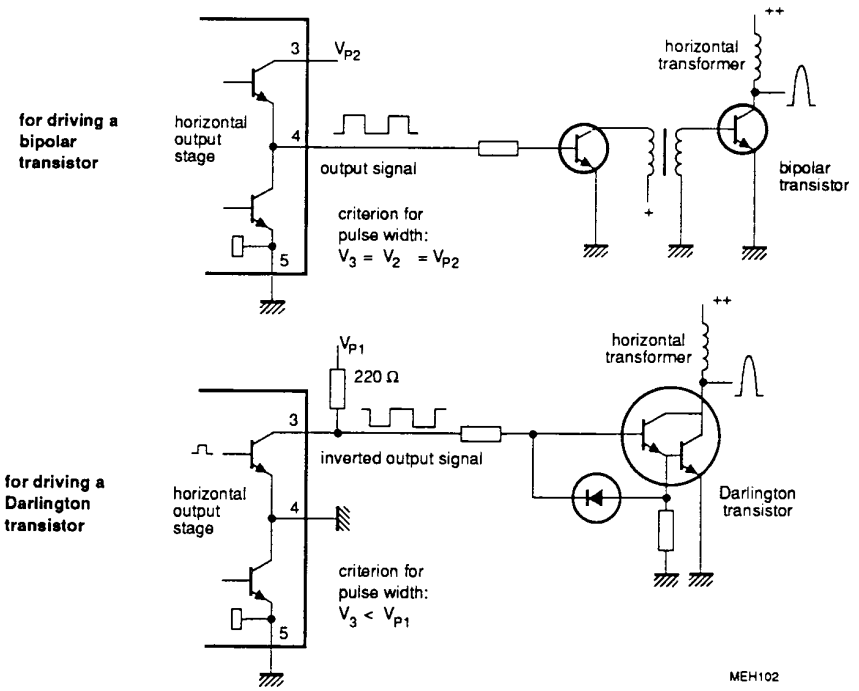


Fig.4 Horizontal output stage.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	supply voltage (pin 2)	0	16	V
V_{P2}	supply voltage (pin 3)	0	16	V
$V_{10, 11}$	input voltage	–0.5	8	V
I_3	supply current for horizontal output	-	1.0	A
I_4	horizontal output current	-	+200	mA
		-	–1.0	A
I_6	flyback input current	-	±10	mA
I_9	vertical sync output current	-	–10	mA
I_{16}	buffer output current	-	±10	mA
P_{tot}	total power dissipation	-	1.2	W
T_{stg}	storage temperature range	–25	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	-	±300	V

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C and measurements taken in Fig.5 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}	supply voltage range (pin 2)		8.5	12	16	V
V_{P2}	supply voltage range (pin 3)		8.5	12	16	V
I_{P1}	supply current		-	35	-	mA
V_{stab}	stabilized voltage (pin 1)		6.18	6.3	6.5	V
RR	ripple rejection for V_{stab}	f_R = 1 kHz (sinewave) on supply voltage	60	70	-	dB
Sync input signal modes 1 and 2, AC-coupled to pin 10						
$V_{i\ sync}$	negative-going sync input signal (peak-to-peak value, pin 10)	mode 1; Fig.3; R_S = 50 to 500 Ω	-	1	1.5	V
	sync amplitude in video signal		180	300	400	mV
	clamping voltage		-	1.28	-	V
	slicing level above clamping level	$t_{p\ sync}/t_H$ = 0.1	-	120	-	mV
	voltage for automatic polarity correction inactive	mode 1	-	-	1.5	V
	positive or negative-going sync input signal (peak-to-peak value, pin 10)	mode 2; Fig.3; R_S = 50 to 500 Ω	2	-	5.5	V
	voltage for automatic polarity correction active	mode 2	2	-	-	V
	slicing level	mode 2	25	50	75	%
I_{10p}	input current	during video signal	1	2	3.5	µA
R_{10}	input resistance	V_{10} < 1.28 V	-	50	-	Ω
		V_{10} > 1.28 V	-	high-ohmic	-	Ω
V_{11}	charging current (peak value)	mode 2	-	–6	-	mA
	discharging current	V_{11} > 1.4 V	-	10	-	µA
V_{12}	threshold voltage for automatic polarity correction	mode 2	2.6	3.0	3.4	V
	voltage to select positive-going sync		3.5	V_{stab}	-	V
	voltage to select negative-going sync		0	-	2.5	V
I_{12}	charging current at positive-going sync	mode 2	-	–50	-	µA
	discharging current at negative-going sync		-	50	-	µA
Sync input signal mode 3 DC-coupled to pin 11 (8.2 kΩ from pin 10 to ground)						
V_{11}	positive or negative-going sync input signal (peak value, pin 11)	mode 3; Fig.3	3.2	-	5.5	V
	slicing level of sync pulses		1.25	1.4	1.55	V
	voltage for automatic polarity switch active		3.2	-	-	V
V_{12}	input voltage to select polarity correction	positive-going sync	3.5	V_{stab}	-	V
		negative-going sync	0	-	2.5	V
$t_{p\ sync}/t_H$	duty cycle for automatic correction in polarity		-	-	25	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vertical/composite sync output						
$V_{9\,H}$	sync output voltage HIGH	I_9 = −1 mA	9.3	10	11	V
$V_{9\,L}$	sync output voltage LOW	I_9 = 0.3 mA	-	0.7	1.1	V
R_9	resistor from V_{P1} to pin 9 to achieve composite sync mode	Fig.1	-	15	-	kΩ
t_d	delay time between leading edge of vertical sync and vertical trigger pulse	pin 9	7.5	15	20	µs
Artificial sync generator						
V_{13}	threshold voltage	lower threshold; Fig.6	-	1.6	-	V
		upper threshold	-	4.8	-	V
	input voltage for generator off	direct sync	ground-connected			V
I_{13}	output current	generator active	-	$\pm I_{17}$	-	µA
$t_{p\,sync}$	internal sync pulse width	C4 = 120 pF; note 5 f_{osc} = 64 kHz	-	1.5	-	µs
Coincidence detector		with 47 nF from pin 14 to ground				
V_{14}	capacitor voltage	during coincidence	-	5	-	V
		during catching	-	-	1.5	V
I_{14}	charging current	during sync pulse	-	−150	-	µA
	discharging current	during gating pulse	-	25	-	µA
Phase comparator PLL1						
V_{15}	control voltage	lower limit	-	1.6	-	V
		upper limit	-	4.6	-	V
I_{15}	control current	during sync pulse	-	$\pm 0.8 I_{17}$	-	µA
I_{16}	buffer output current		-	±2	-	mA
R_{16}	buffer output resistance		-	10	-	Ω
Horizontal oscillator						
f_{osc}	free-running frequency	R_{osc} = 12 kΩ; C_{osc} = 1.1 nF; note 1	-	65	-	kHz
$\Delta f / f_o$	frequency deviation with fixed external components		-	-	±3	%
TC	temperature coefficient	$(\Delta f/f_o)/\Delta T$	-	-	±15	10^{-5}/K
$\Delta f/\Delta V_{P1}$	frequency dependent on supply voltage	8.5 V < V_{P1} < 16 V	-	±5	±20	Hz/V
φ_H / t_H	relative holding/catching range	R2 = 100 kΩ; note 2	±4.5	±5	-	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Phase comparator PLL2 and phase shifter						
V_{19}	control voltage	upper limit	-	4.6	-	V
		lower limit	-	1.6	-	V
I_{19}	control current during flyback	$V_6 > 3.4$ V	-	$\pm 0.8 I_{17}$	-	µA
V_{20}	input voltage range		-	1.6 to 4.6	-	V
$\Delta t_s/t_H$	phase shifting range, Fig.6	leading edge of sync to middle of flyback	-	±20	-	%
$t_{d\ FLB}$	relative delay time between middle of sync pulse and middle of flyback pulse	Fig.6	3.6	4.4	5.3	%
Horizontal flyback input						
V_6	maximum input voltage		internal limited			V
	slicing level for PLL2	Fig.6	-	3	3.4	V
	slicing level for horizontal blanking		-	0.3	0.45	V
Horizontal pulse generator and output for bipolar deflection transistor						
V_4	output voltage LOW	$I_4 = 100$ mA	-	0.8	1.2	V
I_4	output current (sink)	Fig.4	-	-	100	mA
t_p/t_H	relative pulse width	$V_3 = V_2 = V_{P1}$	-	45	-	%
Horizontal pulse generator and output for Darlington deflection transistor						
V_{3-4}	saturation voltage	$I_3 = -I_4 = 900$ mA	-	1.4	2	V
		$I_4 = -100$ mA	-	0.25	0.4	V
I_3	output current (sink)		-	-	900	mA
t_p/t_H	relative pulse width	$V_3 < V_{P1}$	-	30	-	%
Super sandcastle pulse generator (SSC)						
V_8	output voltage during horizontal scan	$I_8 = 0$	-	-	0.5	V
	output voltage during vertical blanking	$I_8 = 2.8$ mA	2.15	2.5	3.0	V
	output voltage during horizontal blanking		4.2	4.5	4.9	V
	output voltage during clamping pulse	note 3	-	11	-	V
I_8	sink current during trailing edge	$V_8 = 1.5$ V	-	2	-	mA
	vertical blanking current	$V_8 > 2.15$ V	2.3	-	-	mA
		$V_8 < 3$ V	-	-	3.3	mA
$t_{p\ SC}$	gating pulse width	Figures 5 and 6; note 6	-	0.8	-	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Protection circuit input						
V_7	threshold input voltage for horizontal output off	note 4 V_7 positive-going V_7 negative-going	6.18 -	6.3 –0.2	6.5 -	V V
t_d	switching off delay time		-	17	-	µs
V_{P1}	too low supply voltage threshold	horizontal output off horizontal output on	5.4 6.0	5.8 6.4	6.2 6.8	V V

Notes to the characteristics

1. $T_{osc} = 1.16 \times R_{osc} \times C_{osc}$ (approximate value); R_{osc}: 9 kΩ to 18 kΩ
2. $R2 = 48 / p \times R_{osc}$ (approximate value); p ≤10% (catching range)
3. The leading edge of the clamping pulse starts after the trailing edge of the sync pulse respectively with artificial sync.
4. The effect of the protection circuit is to switch off the horizontal output and to latch the error indication. Therefore, the supply voltage must be switched off and on to enable the circuit again
5. Approximate sync pulse width $t_{p\ sync} = C4 \times R_{osc}$
6. Gating pulse width $t_{p\ SC} = 0.1t_H - t_{p\ sync} / 2$ (approximate value at V_8 = 7 V)

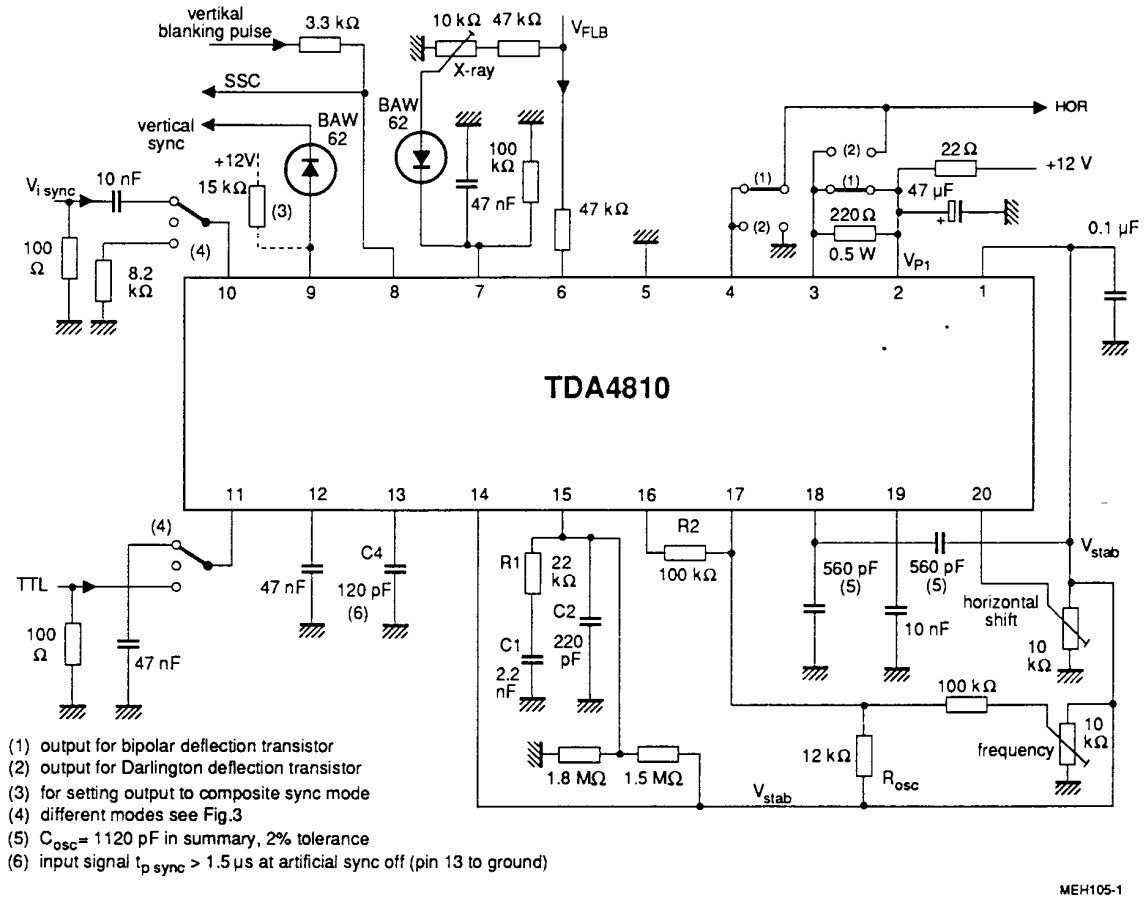


Fig.5 Test and application circuit for 64 kHz deflection.

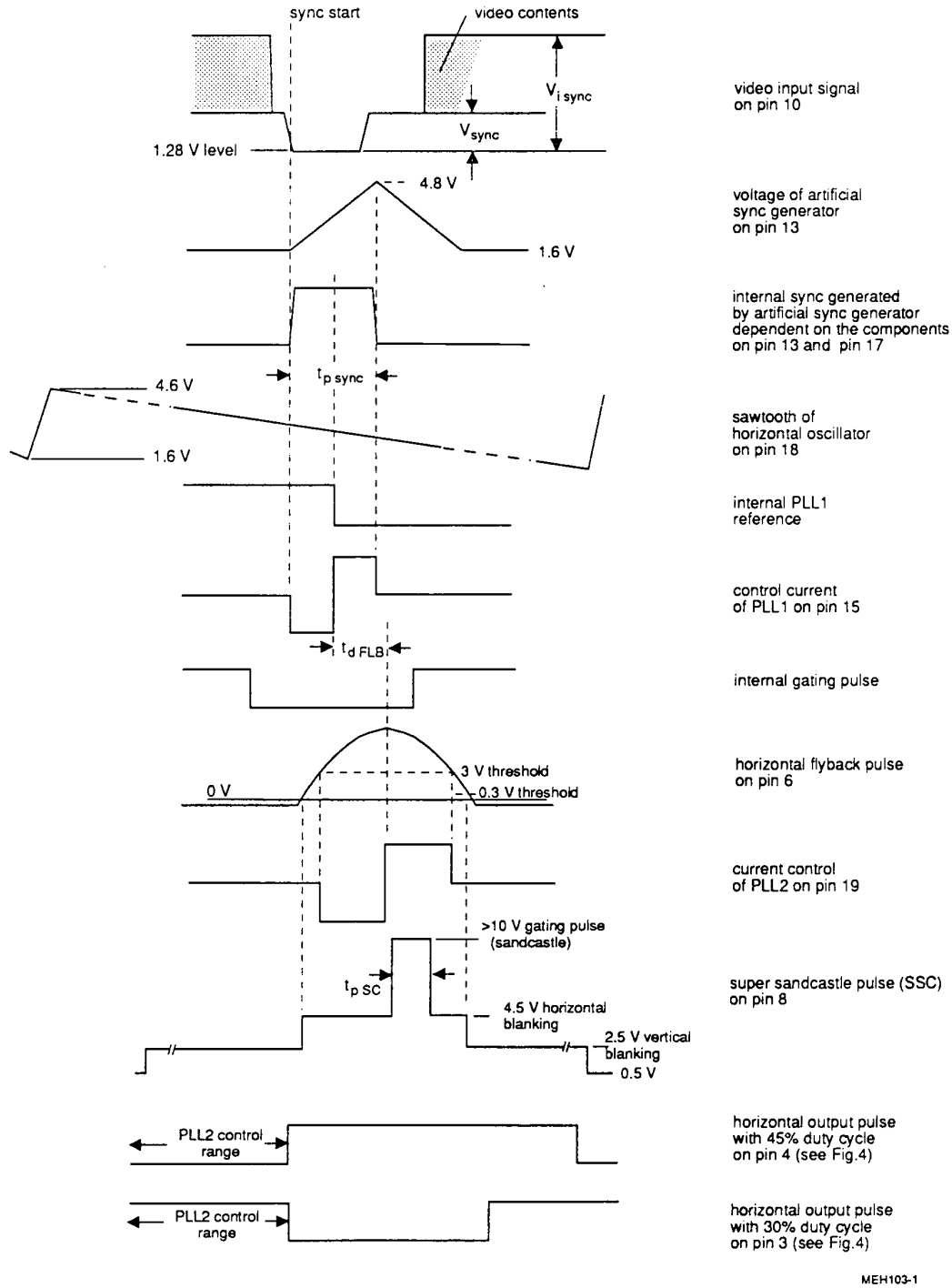


Fig.6 Timing diagram using the artificial sync generator.

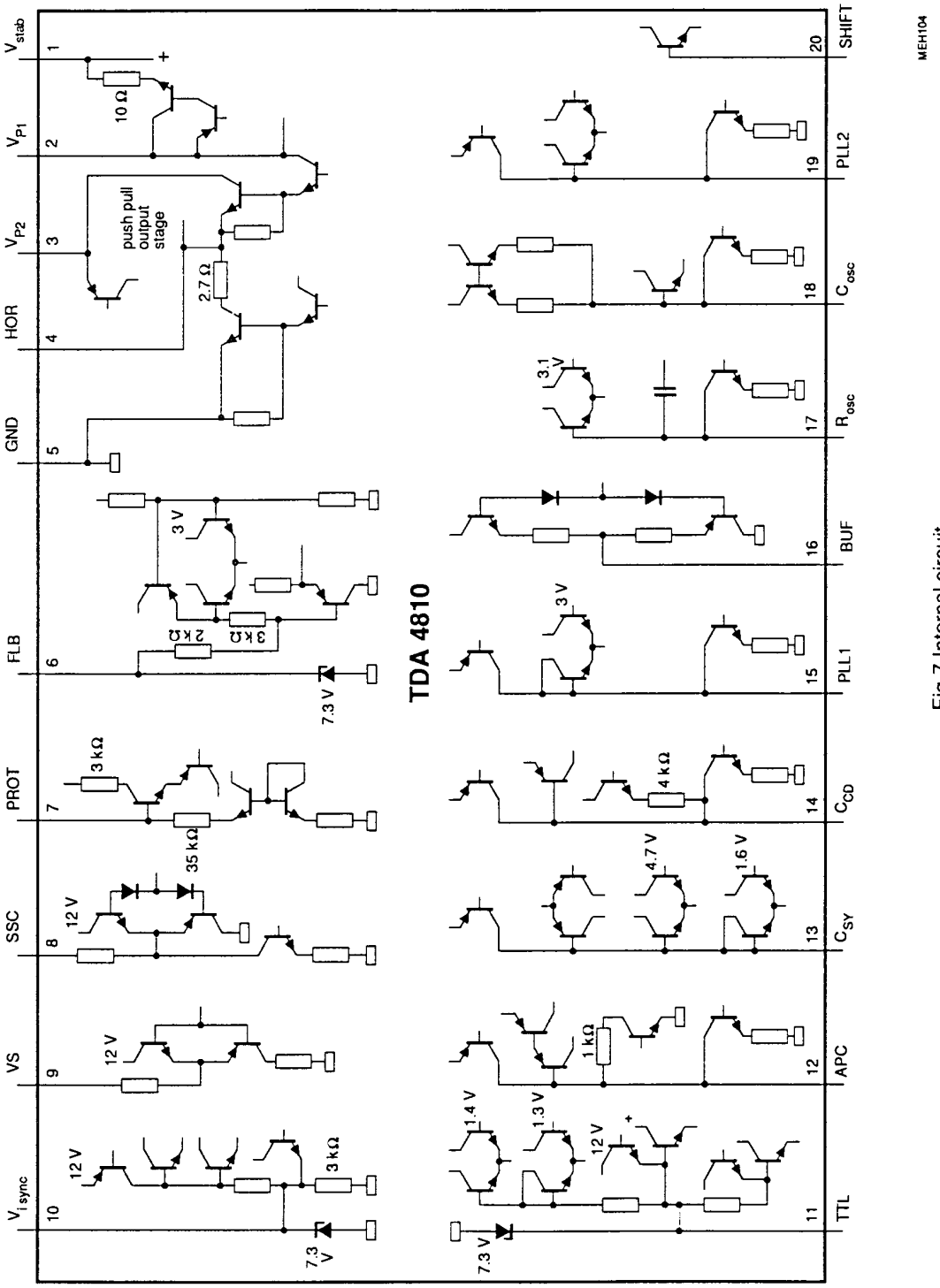


Fig.7 Internal circuit.