ML6461

CCIR656 NTSC Video Encoder

GENERAL DESCRIPTION

The ML6461 is a multi-standard CCIR656 (4:2:2) video (input) composite and S-video (outputs) encoder for NTSC systems. It is designed to provide a low cost, single-chip output interface for a variety of video applications including set-top decoders, DVD players, and other YCrCb to Y/C equipment.

The ML6461 accepts 8-bit YCrCb video in either CCIR656 or Square Pixel format and generates analog Y, C and CV waveforms complete with Closed Caption encoding.

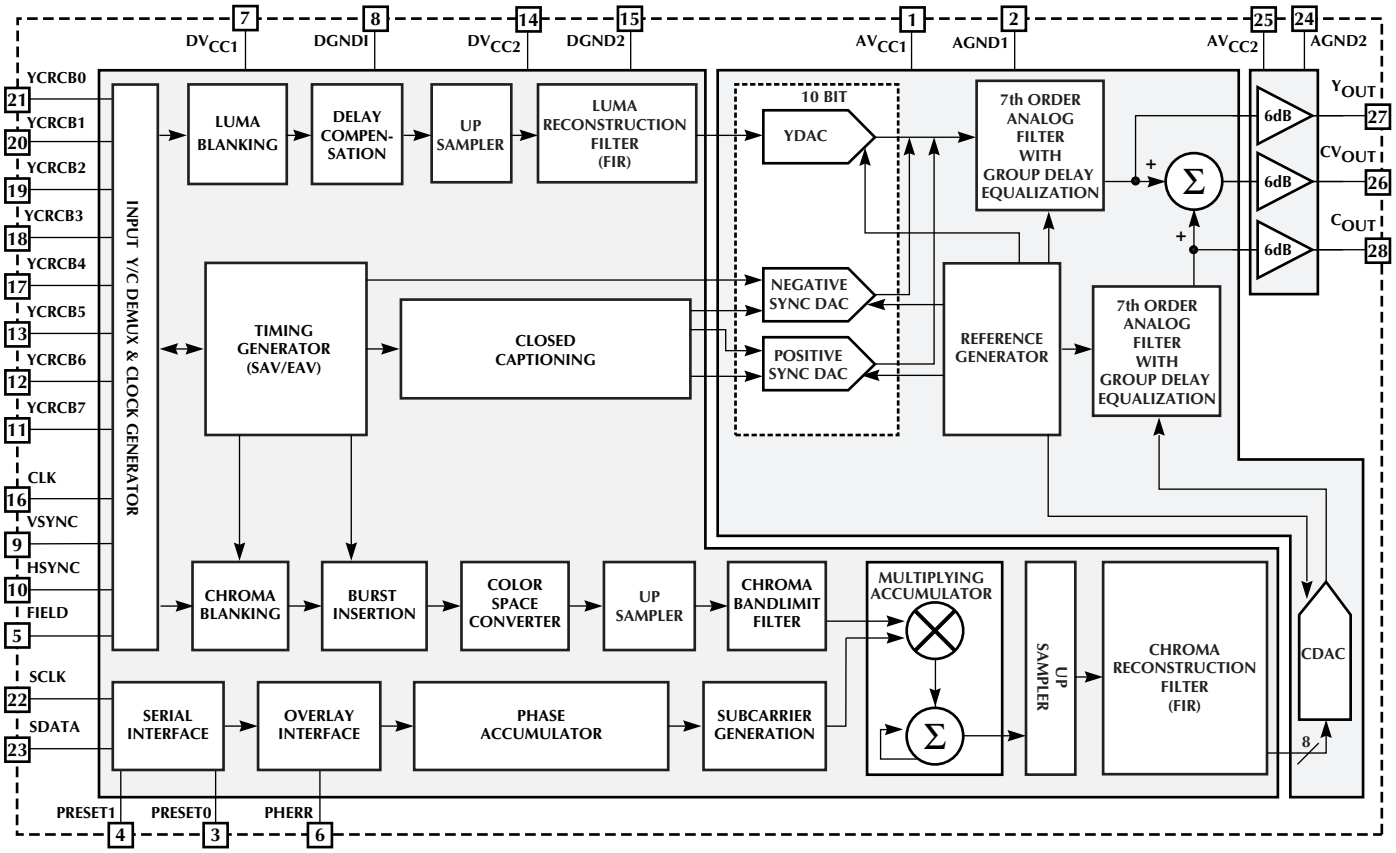
The ML6461 includes output analog reconstruction filters, phase equalizer, and 6dB (2X gain) drivers. Gain scaling, sync, and Y+C mixing are performed at the output of the relevant 10-bit DAC, eliminating the gain mapping stages that require additional DAC bits. The result is Y SNR and granularity remain precisely the same as the source.

The ML6461 supports both master and slave timing operations. S-Video and multiple composite signals can be driven simultaneously into 75Ω loads.

FEATURES

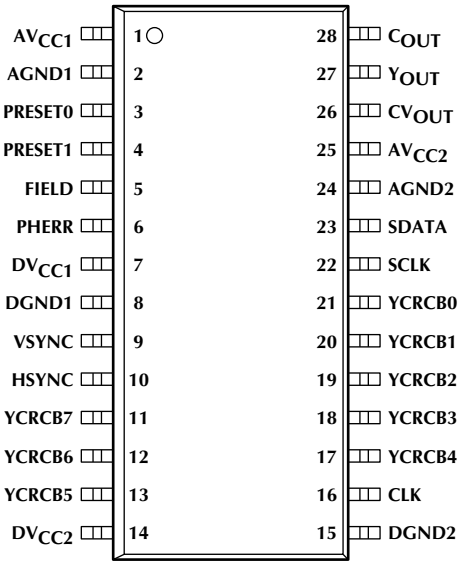
- Closed Caption VBI encoder for line 21 and 284
- Handles SAV/EAV codes for CCIR656 Video
- Single clock input: 27MHz CCIR656, 24.54MHz Sq. Pix.
- Color subcarrier correction for overlay applications
- Onboard analog 7th-order reconstruction filters and 6dB drivers with differential gain/phase of 0.5%/0.5º
- Y, C, CV outputs drive both AC or DC coupled loads
- Multiple 75Ω line drivers for two composite outputs, channel modulator, and S-Video
- 2-wire serial control bus, or selectable presets for stand-alone operation
- Handles Japanese NTSC signals

BLOCK DIAGRAM



PIN CONFIGURATION

ML6461
28-Pin SOIC (S28)



TOP VIEW

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	AV_{CC1}	Analog 5V supply pin
2	AGND1	Analog ground pin
3	PRESET0	Preset input pin for stand alone operation
4	PRESET1	Preset input pin for stand alone operation
5	FIELD	This pin can be configured as an input or output via the control register (bits B8 and B9). If configured as output, it can be programmed to give analog or digital (even/odd) field information. If configured as input, it can be used to set analog fields (1 and 2) or (3 and 4).
6	PHERR	External chroma lock input
7	DV_{CC1}	Digital 5V supply pin
8	DGND1	Digital ground pin
9	VSYNC	Vertical synchronization signal. Pin is configured as input in external slave mode and as output in master and internal slave (CCIR656) modes. Polarity and function are programmed in control register in bits B10, B17, B26, and B28.
10	HSYNC	Horizontal synchronization signal. Pin is configured as input in external slave mode and as output in master and internal slave (CCIR656) modes. Polarity and function are programmed in control register in bits B15, B25, B28, and B29.
11	YCRCB7	YCRCB digital input bit 7
12	YCRCB6	YCRCB digital input bit 6
13	YCRCB5	YCRCB digital input bit 5
14	DV_{CC2}	Digital 5V supply pin
15	DGND2	Digital ground pin
16	CLK	System clock: 27Mhz (CCIR656 rate), 24.54Mhz (Square Pixel rate)
17	YCRCB4	YCRCB digital input bit 4
18	YCRCB3	YCRCB digital input bit 3
19	YCRCB2	YCRCB digital input bit 2
20	YCRCB1	YCRCB digital input bit 1
21	YCRCB0	YCRCB digital input bit 0
22	SCLK	Serial control bus clock input
23	SDATA	Serial control bus data input
24	AGND2	Analog ground pin
25	AV_{CC2}	Analog 5V supply pin
26	CV_{OUT}	Composite video output
27	Y_{OUT}	Luma output
28	C_{OUT}	Chroma output

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

AV_{CC}, DV_{CC} ..... –0.3 to 7V
Analog and Digital Inputs/Outputs .... –0.3 to AV_{CC} + 0.3V
Input current per pin ..... –25 to 25mA

Storage Temperature ..... –65 to 150ºC
Junction Temperature 120ºC

OPERATING CONDITIONS

Temperature Range ..... 0°C to 70°C
Operating Supply Range ..... 4.5V to 5.5V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, AV_{CC} = DV_{CC} = 4.5V to 5.5V, T_A = Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER PERFORMANCE						
	Power Dissipation			750		mW
SUPPLIES						
AV_{CC}	Analog Supply Voltage		4.5		5.5	V
DV_{CC}	Digital Supply Current		4.5		5.5	V
I_{SA}	Analog Supply Current			125		mA
I_{SD}	Digital Supply Current	Max. Programmed Clock Rates		35		mA
DIGITAL INPUT SIGNALS						
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
I_{IL}	Low Level Input Current	V_{IN} = at 0.1V			1	µA
I_{IH}	High Level Input Current	V_{IN} = at DV_{CC} – 0.1V			1	µA
	Input Capacitance			2		pF
DIGITAL OUTPUT SIGNALS						
V_{OL}	Low Level Output Voltage	I_{OUT} = 2mA			0.4	V
V_{OH}	High Level Output Voltage	I_{OUT} = 100µA	V_{CC}-0.4			V
	Output Capacitance			50		pF
ENCODER AND DAC (Note 2)						
	Output Amplitude Accuracy	SMPTE Color Bars		2	5	%
	CV Output Amplitude	SMPTE Color Bars, Peak-to-Peak	0.95		1.05	V
	C Output Amplitude	SMPTE Color Bars, Peak-to-Peak	0.594		0.657	V
	Y Analog/Digital Bandlimit	Swept Multiburst		5.7		MHz
	C Analog/Digital Bandlimit	Swept Multiburst		1.5		MHz
	Vector Phase Accuracy (Note 3)	Swept Multiburst	–2.5	1	2.5	º
	Vector Amplitude Accuracy (Note 3)	SMPTE Color Bars	–2.5		2.5	%
	Chroma Phase Linearity	NTC7 Stepped Subcarrier	–2		2	º
	Chroma Amplitude Linearity	NTC7 Stepped Subcarrier	–1		1	IRE
	Differential Gain	NTC7 Modulated Staircase (Note 2)		0.5	1	%
	Differential Phase	NTC7 Modulated Staircase (Note 2)		0.5	1	º

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ENCODER AND DAC (Continued) (Note 2)						
	Luma Nonlinearity		–1		1	IRE
	F_{SC} Phase Jitter (RMS)	SMPTE Color Bars		1		°
	Quadrature Error	SMPTE Color Bars		1		°

SERIAL BUS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT						
V_{IL}	Low Level Input Voltage		0		0.8	V
V_{IH}	High Level Input Voltage		V_{CC} – 0.8		V_{CC}	V
I_{IL}	Low Level Input Current	V_{IN} = 0V			1.0	µA
I_{IH}	High Level Input Current	V_{IN} = DV_{CC}			1.0	µA
Z_{IN}	Input Impedance	f_{CLK} = 100kHz		1		MΩ
C_{IN}	Input Capacitance			2		pF
SYSTEM TIMING						
f_{CLOCK}	S_{CLK} Frequency				100	kHz
V_{HYS}	Input Hysteresis		0.2			V
t_{SPIKE}	Spike Suppression	Max Length for Zero Response		50		ns
t_{WAIT}	Wait Time From STOP to START On S_{DATA}			1.3		µs
$t_{HD/START}$	Hold Time for START On S_{DATA}			0.6		µs
$t_{SU/START}$	Setup Time for START On S_{DATA}			0.6		µs
t_{LOW}	Min LOW Time On S_{CLK}		1.3			µs
t_{HI}	Min HIGH Time On S_{CLK}		0.6			µs
$t_{HD/DATA}$	Hold Time On S_{DATA}			5.0		µs
$t_{SU/DATA}$	Setup Time On	Fast mode	100			ns
		Slow mode	250			ns
t_{LH}	Rise Time for S_{CLK} & S_{DATA}			30	300	ns
t_{HL}	Fall Time for S_{CLK} & S_{DATA}			30	300	ns
$t_{SU/STOP}$	Setup Time for STOP On S_{DATA}			0.6		µs

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.

Note 2: All specifications include reconstruction filter and line driver.

Note 3: Normalized to burst.

FUNCTIONAL DESCRIPTION

INTRODUCTION

The ML6461 is a single-chip NTSC video encoder for generating analog composite (CV) and S-video (Y/C) outputs from YCrCb digital inputs. The ML6461 is a mixed signal processor optimizing SNR and distortion by performing subcarrier generation, sync generation, modulation and upsampling in the digital domain, while performing mixing, reconstruction and gain scaling in the analog domain. In particular, the Y channel requires no digital scaling, eliminating the need for higher precision digital solutions. All timing is based on an external clock source either 27MHz for CCIR656 clock rate or 24.54MHz for square pixel clock rate.

Additionally, the ML6461 allows the inclusion of Closed Captioning codes in the vertical blanking interval (VBI). Both lines 21 and 284 support Closed Captioning.

Other special functions include: programmable polarity and relative position of sync pulses, master and slave modes of which includes the ability to handle ITU-R656-compliant digital TV or ITU-R/SMPTE specifications, chroma subcarrier phase and frequency adjustments from external source; Japanese NTSC support; 100% color bars processing; and internal 7th order reconstruction filters with group delay equalization and 6dB line drivers for direct TV output.

The ML6461 can be programmed and controlled via a two-wire serial bus or preset modes. A summary of the features of the ML6461 are listed in Table 1.

VIDEO STANDARDS SUPPORTED

The ML6461 supports NTSC only. The video standards and clock rates are listed in Table 2.

DEVICE	FUNCTIONAL DESCRIPTION								
	Video Formats		Clock Rates		DAC	Closed Caption Encoder	Macrovision	Reconstruction Filter	75Ω Cable Driver
	NTSC	PAL	CCIR656	Square Pixel					
ML6460	Yes. Input: 8-Bit YCrCb digital Outputs: Y, C, and CV analog	No	Yes	Yes	Yes. 10-bit DAC	Yes	Yes	Yes. 7th-order Butterworth, with group delay equalization	Yes.
ML6461	Yes. Input: 8-Bit YCrCb digital Outputs: Y, C, and CV analog	No	Yes	Yes	Yes. 10-bit DAC	Yes	No	Yes. 7th-order Butterworth, with group delay equalization	Yes.

Table 1. Video Encoder Functional Selection

INPUT	CLOCK RATE	HORIZONTAL LINES PER FRAME	PIXELS PER HORIZONTAL LINE
NTSC CCIR656	27 MHz	525	858
NTSC Square Pixel	24.54 MHz	525	780

Table 2: Video Standards and Clock Rates

MODE	VSYNC PIN	HSYNC PIN	FIELD PIN
Master Mode	OUT	OUT	IN/OUT
External Slave Mode	IN	IN	IN/OUT
Internal Slave Mode (SAV/EAV CCIR656)	OUT	OUT	IN/OUT

Table 3: Pin Assignments for Various Master/Slave Modes

FUNCTIONAL DESCRIPTION (Continued)

VIDEO TIMING AND INPUTS

The clock source for the ML6461 can be either 27MHz (CCIR656) or 24.54MHz (NTSC Square Pixel). The ML6461 internal timing generator also provides necessary horizontal and vertical syncs, video blanking, burst, and closed caption timing. The internal clock is derived through buffering and inverting the external CLK signal. The inputs YCRCB<7:0>, VSYNC, and HSYNC are registered at the rising edge of CLK and PHERR is registered at the falling edge of CLK. All inputs must be valid for the minimum setup time of 5ns. The outputs VSYNC, HSYNC, and FIELD are clocked at the rising edge of CLK and are valid 10ns following the edge of the clock.

The ML6461 can operate in master and slave modes. In master mode, the ML6461 internally generates the vertical reset (VSYNC pin is an output) and horizontal reset (HSYNC pin is an output). In the slave modes, there are two alternatives. External slave mode allows the user to provide an external vertical reset (VSYNC pin is an input) and an external horizontal reset (HSYNC pin is an input). Internal slave mode (CCIR656) uses the SAV and EAV codes to generate the vertical and horizontal resets. The master/slave modes are selected via register program. Table 3 provides a description of the various modes and the assignments of the VSYNC, HSYNC, and FIELD pins.

MASTER MODE

A logical 0 in the SLAVE/MASTER bit (bit B28) will configure the ML6461 in the master mode. Multiplexed Y, Cr, Cb data is streamed through the YCRCB <7:0> input pins. VSYNC and HSYNC pins are configured as outputs and provide vertical and horizontal sync information. The polarity of the active edge of the HSYNC and VSYNC pulses can be programmed through the control register via the SENSE_HSYNC bit (bit B15) and the SENSE_VSYNC bit (bit B10), respectively. Coincident active edges of the horizontal and vertical syncs at the start of the line 4 indicates the beginning of an odd field, whereas, the active edge of the vertical sync pulse when the horizontal sync is non-active at the middle of line 266, indicates the beginning of an even field (Figure 1). The FIELD pin can be configured either as an input or output through the FRAME_MODE bit (bit B8). If configured as output (B8 =0) it can be set to provide either even/odd field information (B9 = FLD_FRM_MODE = 0) or analog field information (B9 = 1). For the former case, a logical 1 on the FIELD pin indicates odd fields and a logical 0 even fields. For the latter,(on the FIELD pin), a logical 1 is held during analog fields 1 and 2, and a logical 0 during analog fields 3 and 4. If the FIELD pin is configured as an input (B8 = FRAME_MODE = 1) it must be held low and high on alternating frames and it should change state at the beginning of vertical sync during fields 1 and 3. The internal subcarrier oscillator is reset to make the frame — for which FIELD pin is held 1 — correspond to analog fields 1 and 2 (Figure 2). In master mode, a composite blanking signal is also available thru the HSYNC pin. This can be activated via the CBLANK bit (B29=1). The polarity of the composite blanking signal is programmable from the SENSE_HSYNC bit (B15). When the SENSE_HSYNC bit is set (B15=1), the ML6461 will output a logic 0 at the HSYNC pin during the pixels which are blanked. Conversely, when the SENSE_HSYNC bit is cleared (B15=0), the ML6461 will output a logic 1 at the HSYNC pin during the pixels which are blanked. Consequently, the YCRCB<7:0> inputs will be ignored and a constant blanking level will be output to the analog channels YOUT, COUT, and CVOUT. The operation of the VSYNC and FIELD pins are not affected by the settings of CBLANK and SENSE_HSYNC.

SLAVE MODES

A logical 1 in the SLAVE/MASTER bit (B28) will configure the ML6461 for slave mode. Based on what timing information is provided, there are two slave modes: internal and external. Composite blanking—similar to that described in Master Mode—is also available. Note that in the internal slave mode, vertical and horizontal sync pulses and/or composite blanking signals are output for monitoring purposes only. All timing is derived from SAV/EAV codes.

Internal Slave Mode for CCIR656 with SAV/EAV codes

In this mode (B26 = SLAVE_MODE=1), all the horizontal and vertical timing information including odd/even field selection is embedded in the multiplexed Y, Cr, Cb data stream input through the YCRCB <7:0> pins. VSYNC and HSYNC pins are configured as outputs to give vertical and horizontal sync pulses respectively. The operation of the FIELD pin is similar to that in the master mode. Composite blanking — similar to the one described in the master mode — is also available. Note that in the internal slave mode, vertical and horizontal sync pulses and / or composite blanking signal is output for monitoring purposes only. As mentioned above, all timing is derived from SAV/EAV codes.

External Slave Mode

In this mode: Where (B26 = SLAVE_MODE=0), horizontal and vertical reset pulses must be provided externally through HSYNC and VSYNC pins which are configured as inputs. The polarity of these pulses is programmed through bits SENSE_HSYNC (B15) and SENSE_VSYNC (B10). A horizontal reset pulse on the HSYNC pin can be given either at the beginning of active video (B25=HRESET_MODE=1) or at the beginning of horizontal blanking (B25=HRESET_MODE=0). Once per frame, the active edge of a vertical reset pulse coincident with the active edge of a horizontal reset pulse initializes the internal vertical line counter to the beginning of an odd field at line 4. Non-coincident vertical reset pulses, for example, the ones which fall outside of the interval (see Figure 3) determined by the active edge of the horizontal reset pulse, will be ignored. The FIELD pin, as explained above can be configured as an input to dictate analog fields or as an output to monitor odd/even fields or analog

FUNCTIONAL DESCRIPTION (Continued)

fields (1-2) and (3-4). The ML6461 also supports a frame based synchronization mode (B17 = FSYNC = 1) where a vertical reset pulse unconditionally resets the vertical line counter to line 4. For proper operation only one active edge should be sent per frame. The polarity is controlled by SENSE_VSYNC (B10).

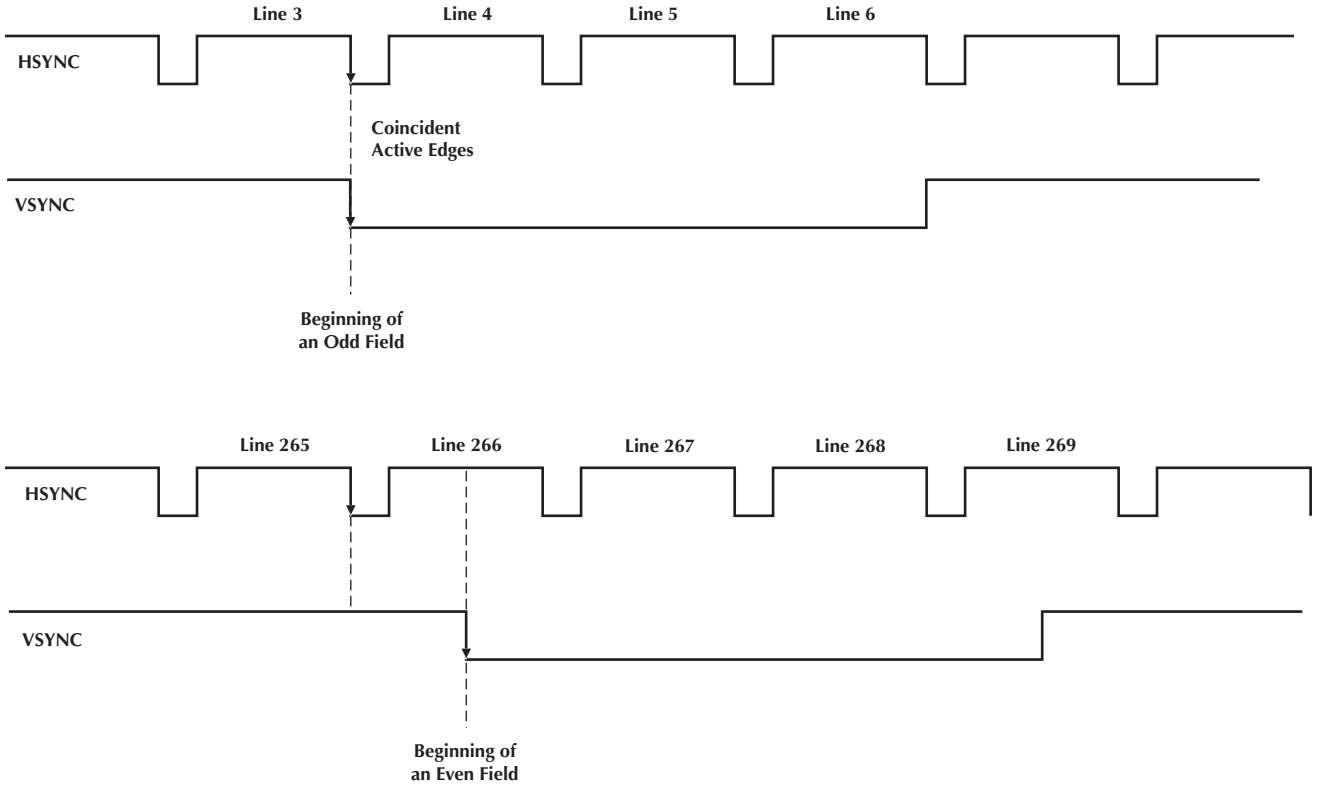


Figure 1. Example of the Beginning of the Odd And Even Fields vs. HSYNC and VSYNC in Master Mode. (SLAVE/MASTER = 0, SENSE_HSYNC = 0, SENSE_VSYNC = 0)

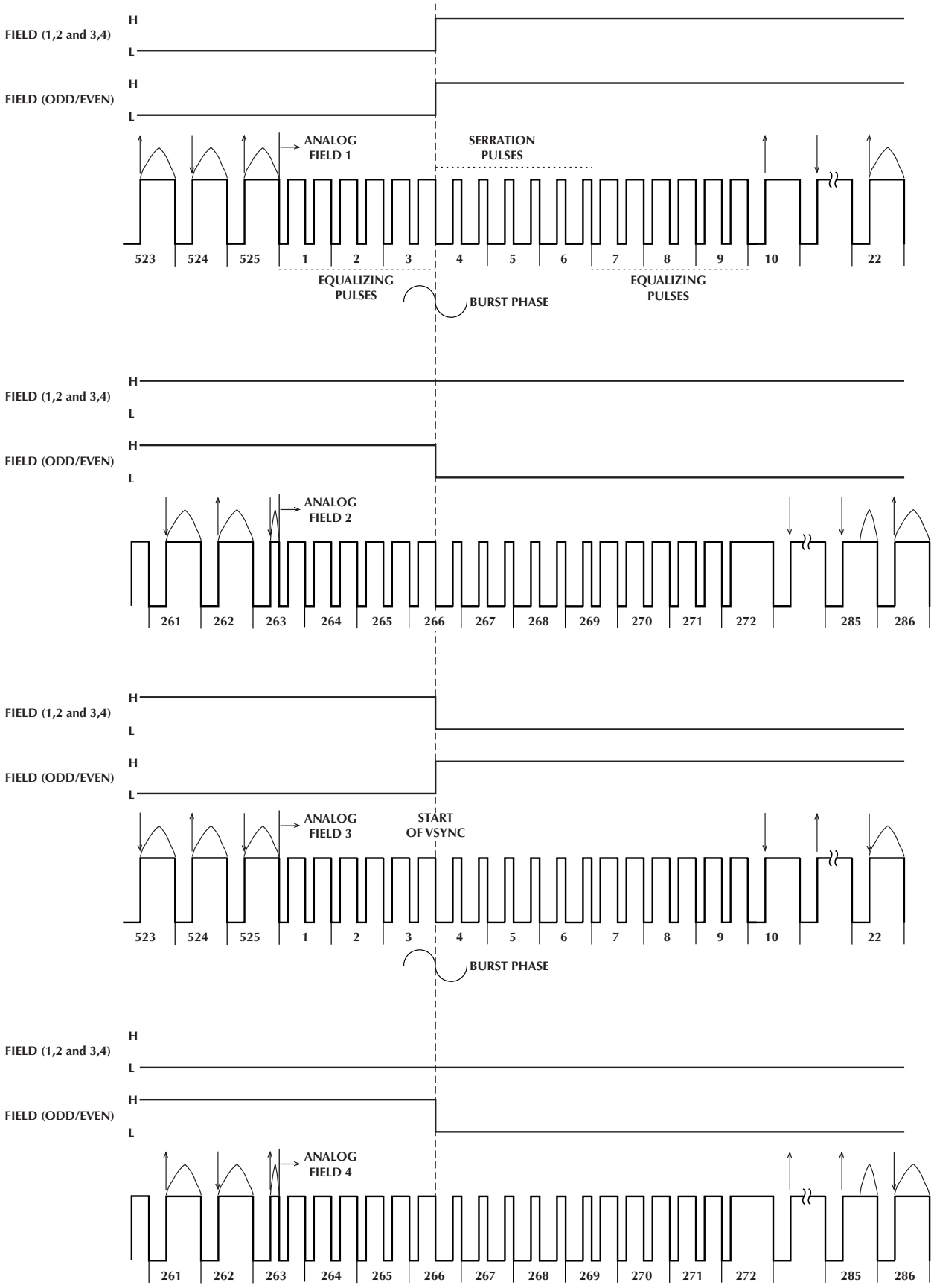


Figure 2. Four Fields (M) NTSC Format FIELD Pin Out

FUNCTIONAL DESCRIPTION (Continued)

PIXEL SYNCHRONIZATION

Master Mode

In this mode, the active edge of horizontal sync pulse through the HSYNC pin (configured as an output) indicates the beginning of an active video line (or the beginning of the horizontal blanking) and the multiplexed YCrCb pixel data must be synchronized to this edge for proper video location, as well as the proper demultiplexing of YCrCb values. This synchronization, as shown in Figures 4 through 5a, is controlled by SEL_HSYNC1 (B14) and SEL_HSYNC0 (B13). Figures 4 and 4a show synchronization for active edge at the beginning of active video for positive or negative HSYNC polarity while Figures 5 and 5a show synchronization for active edge at the beginning of horizontal blanking for positive or negative HSYNC polarity.

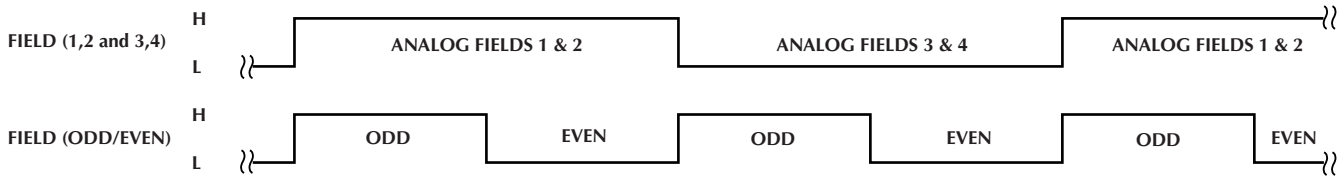


Figure 2a. FIELD Pin Output Summary

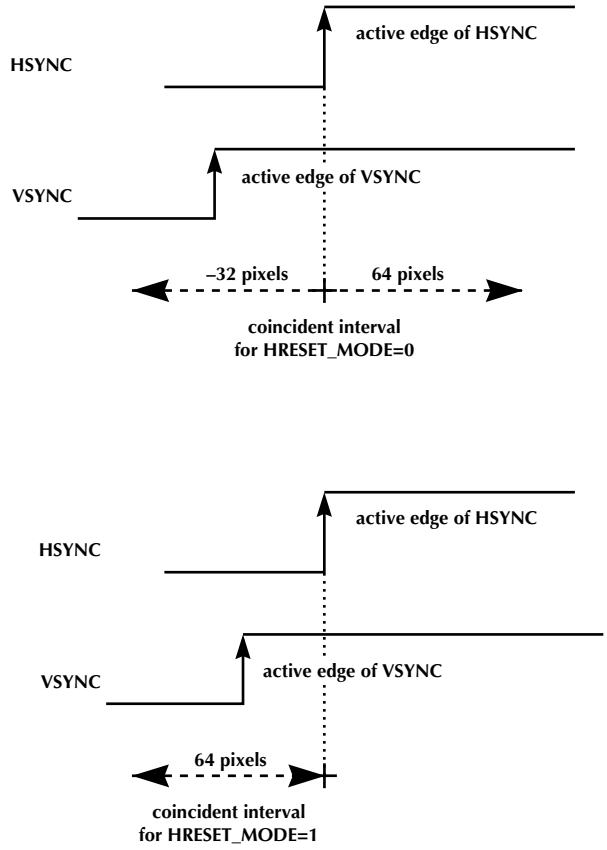


Figure 3. Coincident Valid Sync Intervals for External Slave Mode

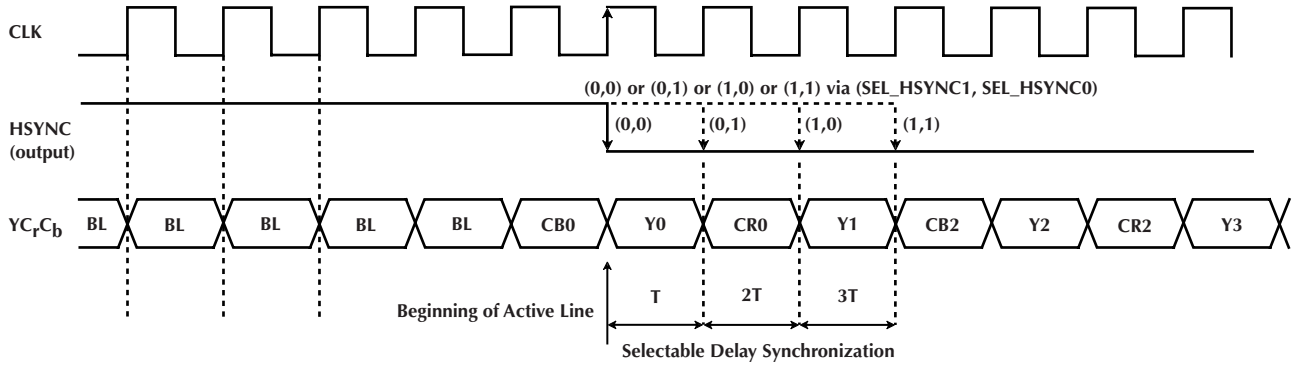


Figure 4. Pixel Synchronization. For Master Mode, Active Edge at Beginning of Active Video. (CBLANK = 1, SENSE_HSYNC = 0) (BL = Blanked Pixel)

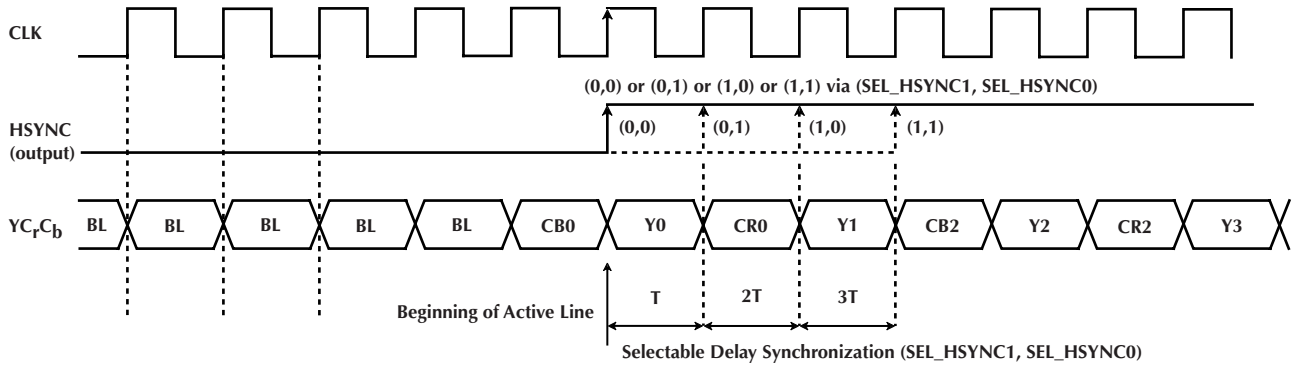
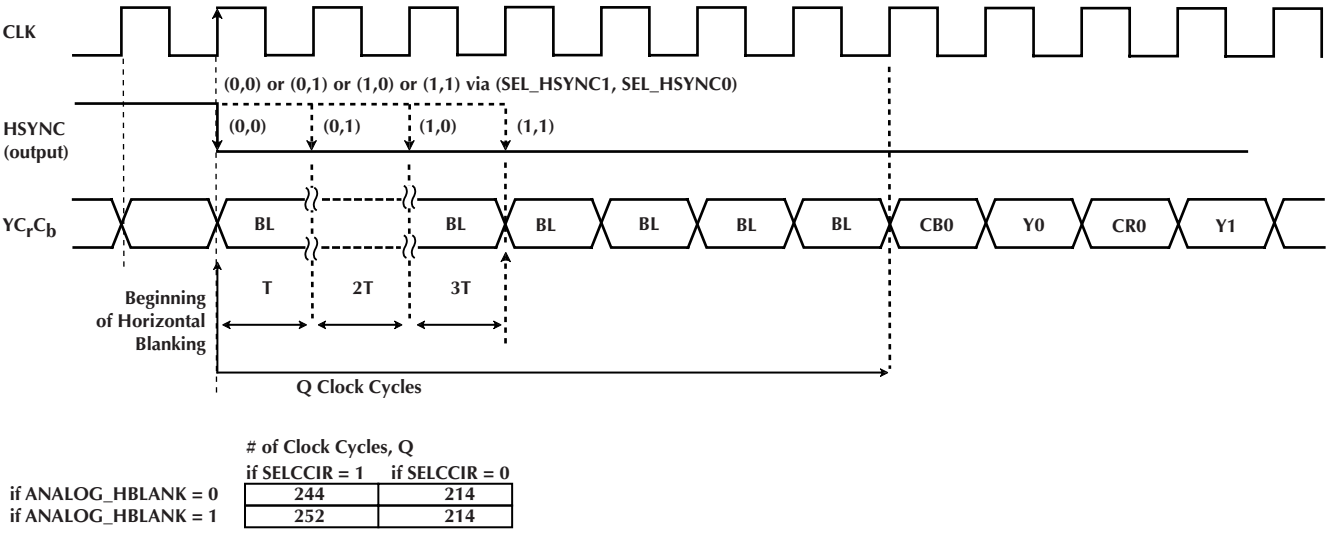
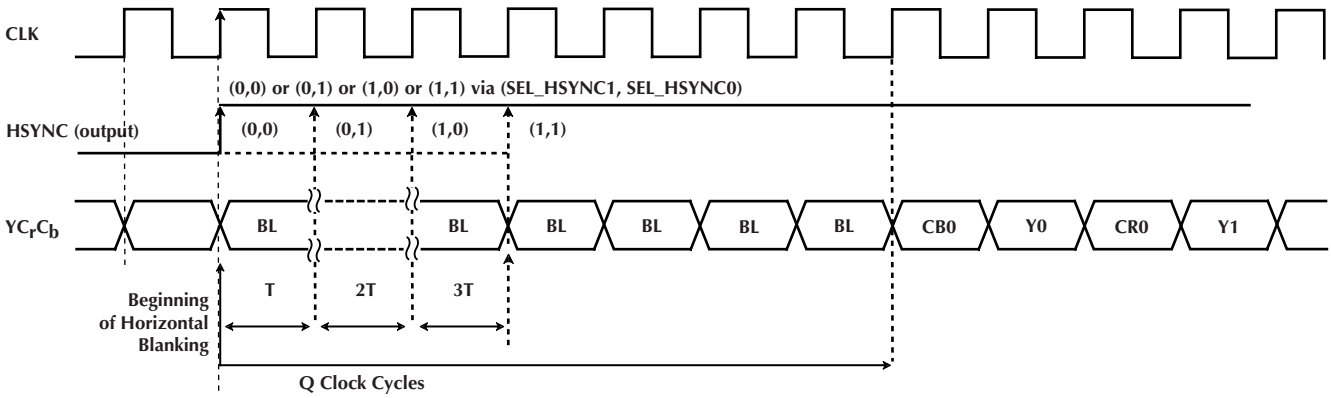


Figure 4a. Pixel Synchronization. For Master Mode, Active Edge at Beginning of Active Video. (CBLANK = 1, SENSE_HSYNC = 1) (BL = Blanked Pixel)



	# of Clock Cycles, Q	
	if SELCCIR = 1	if SELCCIR = 0
if ANALOG_HBLANK = 0	244	214
if ANALOG_HBLANK = 1	252	214

Figure 5. Pixel Synchronization. For Master Mode, Active Edge at Beginning of Horizontal Blanking. (CBLANK = 0, SENSE_HSYNC = 0) (BL = Blanked Pixel)



	# of Clock Cycles, Q	
	if SELCCIR = 1	if SELCCIR = 0
if ANALOG_HBLANK = 0	244	214
if ANALOG_HBLANK = 1	252	214

Figure 5a. Pixel Synchronization. For Master Mode, Active Edge at Beginning of Horizontal Blanking. (CBLANK = 0, SENSE_HSYNC = 1) (BL = Blanked Pixel)

FUNCTIONAL DESCRIPTION (Continued)

Internal Slave Mode

Embedded in the YCrCb data stream, the timing code 0xFF, 0x00, 0x00, 0x(SAV) must be inserted before the samples of the first active pixel. Figures 6 through 6b illustrate timing for CCIR656 video with SAV and EAV codes for CCIR or Square Pixel clocking.

External Slave Mode

A horizontal reset pulse can be used either at the beginning of active video or the beginning of horizontal blanking to provide synchronization of the YCrCb data to the internal clock. Bits SEL_HSYNC1(B14) and SEL_HSYNC0 (B13) are provided to achieve some degree of programmability in this synchronization. Figures 7 and 7a show synchronization for active edge at the beginning of active video for positive or negative HSYNC polarity while Figures 8 and 8a show synchronization for active edge at the beginning of horizontal blanking for positive or negative HSYNC polarity.

Polarity of HSYNC and VSYNC

In both the Master and Slave modes, the HSYNC and VSYNC polarity can be selected via bit SENSE_HSYNC and SENSE_VSYNC. When the SENSE_HSYNC bit is set to logical 1, the HSYNC pulse is on the rising edge. When the SENSE_HSYNC bit is cleared to logical 0, the HSYNC pulse is on the falling edge. Similarly, when the SENSE_VSYNC bit is set logical 1, the VSYNC pulse is on the rising edge. When the SENSE_VSYNC bit is cleared to logical 0, the VSYNC pulse is on the falling edge.

HSYNC Timing Delay

In both Master and Slave modes, the SEL_HSYNC1(B14) and SEL_HSYNC0 (B13) bits of the control register can be programmed to delay the HSYNC active edge up to three clock periods, 3T, where T is one period of the clock.

CHROMA AND LUMA PROCESSING

Refer to Figures 9 through 12.

VIDEO OUTPUT STAGE

Reconstruction filtering, clamping, and line drivers

The ML6461 can simultaneously provide outputs for S-video, two composite video, and a TV modulator. Differential gain and phase are guaranteed at the outputs of the line drivers. Two internal 7th-order Butterworth filters and a group delay equalizer are used as reconstruction filters on S-video (NTSC). The composite signal is generated after reconstruction. The S-video (Y and C) and composite video (CV) are then fed into 75Ω line drivers.

Each of the filter/drivers are designed to guarantee a differential phase of 0.5º and differential gain of 0.5%.

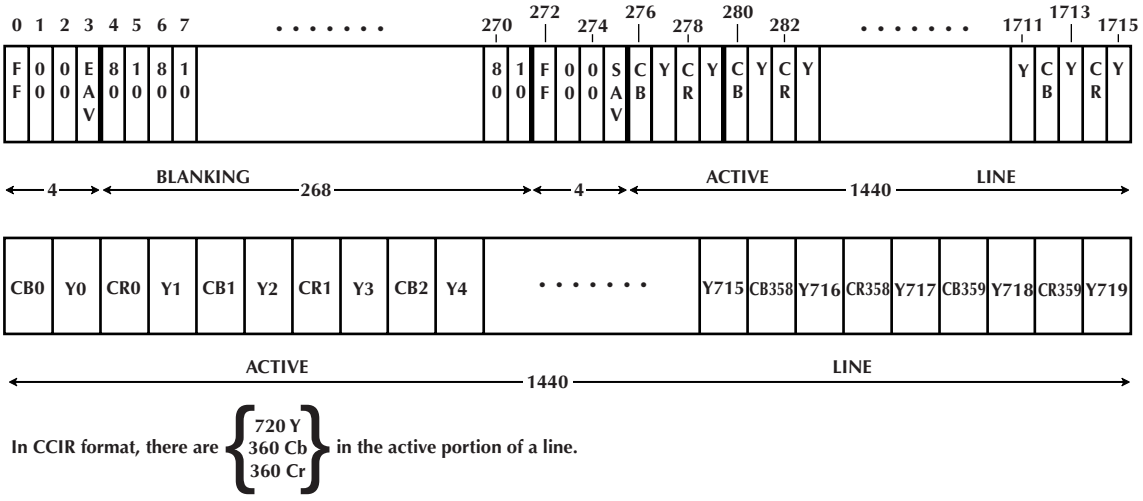


Figure 6. CCIR Format: CLK = 27MHz

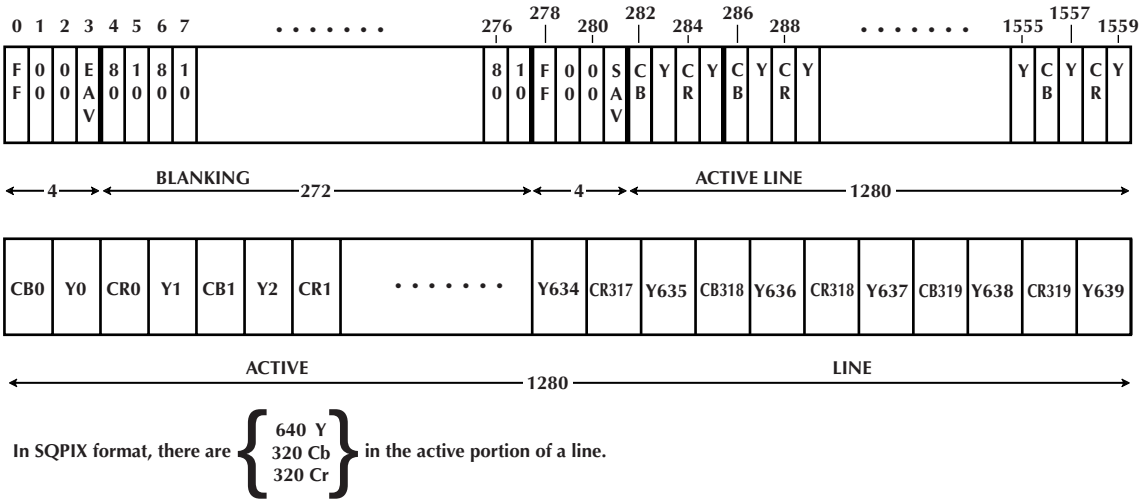
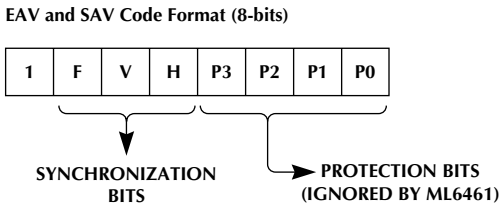
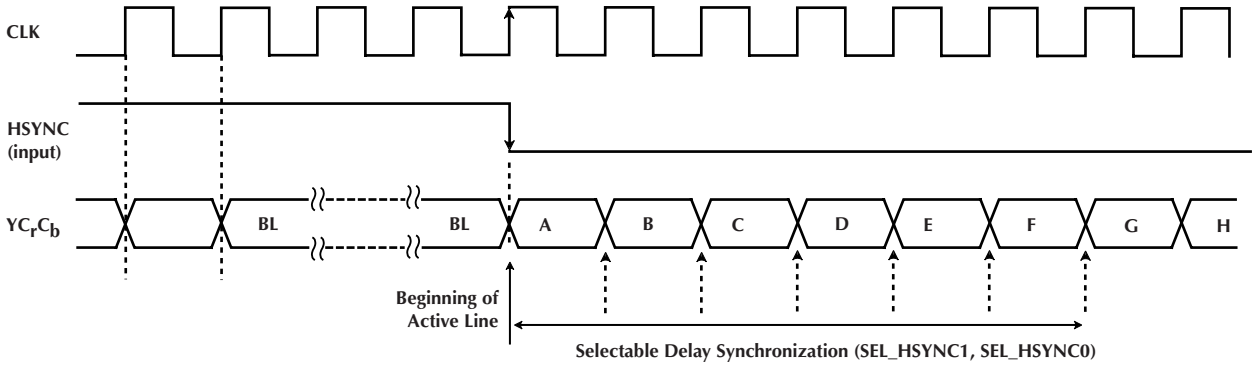


Figure 6a. Square Pixel (SQPIX) Format: CLK = 24.54MHz



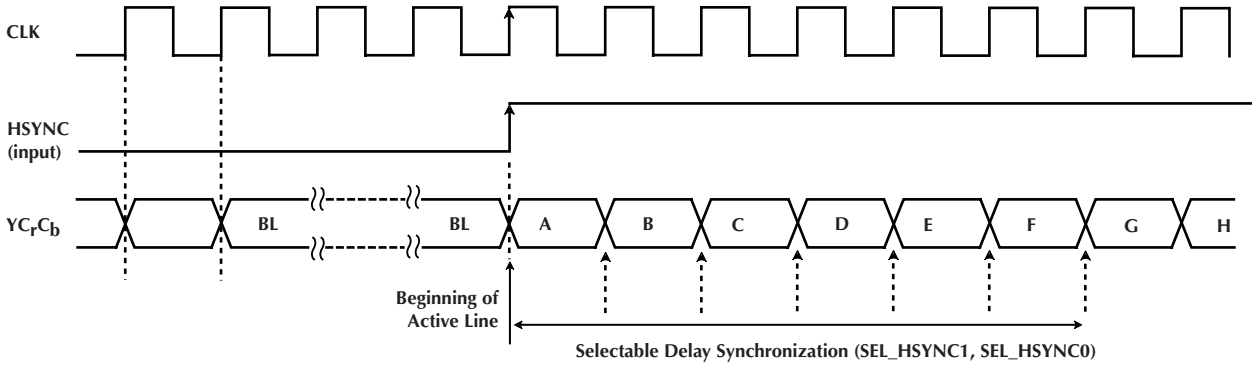
		Format <1,F,V,H,P3,P2,P1,P0>				
Line Number	Code	1	F	V	H	P3~P0
1 to 3	EAV	1	1	1	1	X
	SAV	1	1	1	0	X
4 to 19	EAV	1	0	1	1	X
	SAV	1	0	1	0	X
20 to 263	EAV	1	0	0	1	X
	SAV	1	0	0	0	X
264 to 265	EAV	1	0	1	1	X
	SAV	1	0	1	0	X
266 to 282	EAV	1	1	1	1	X
	SAV	1	1	1	0	X
283 to 525	EAV	1	1	0	1	X
	SAV	1	1	0	0	X

Figure 6b. SAV/EAV Codes for 525/60.



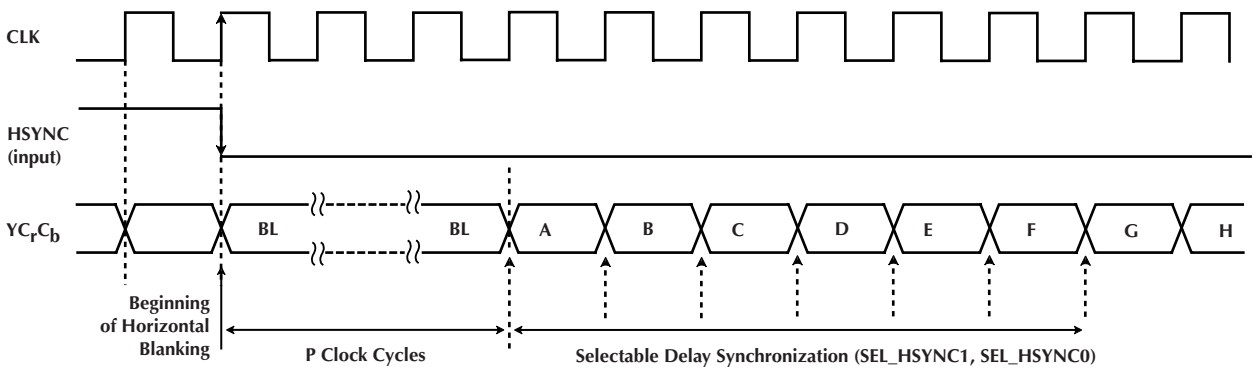
		Value (SEL_HSYNC1, SEL_HSYNC0)			
		(0,0)	(0,1)	(1,0)	(1,1)
Bit	A	CB0	BL	BL	BL
	B	Y0	CB0	BL	BL
	C	CR0	Y0	CB0	BL
	D	Y1	CR0	Y0	CB0
	E	CB2	Y1	CR0	Y0
	F	Y2	CB2	Y1	CR0
	G	CR2	Y2	CB2	Y1
	H	Y3	CR2	Y2	CB2

Figure 7. Pixel Synchronization. For External Mode, Active Edge at Beginning of Active Video. (HRESET_MODE = 1, SENSE_HSYNC = 0, BL = Blanked Pixel) (ANALOG_HRESET = ANALOG_HBLANK = 0 OR ANALOG_HRESET = ANALOG_HBLANK = 1)



		Value (SEL_HSYNC1, SEL_HSYNC0)			
		(0,0)	(0,1)	(1,0)	(1,1)
Bit	A	CB0	BL	BL	BL
	B	Y0	CB0	BL	BL
	C	CR0	Y0	CB0	BL
	D	Y1	CR0	Y0	CB0
	E	CB2	Y1	CR0	Y0
	F	Y2	CB2	Y1	CR0
	G	CR2	Y2	CB2	Y1
	H	Y3	CR2	Y2	CB2

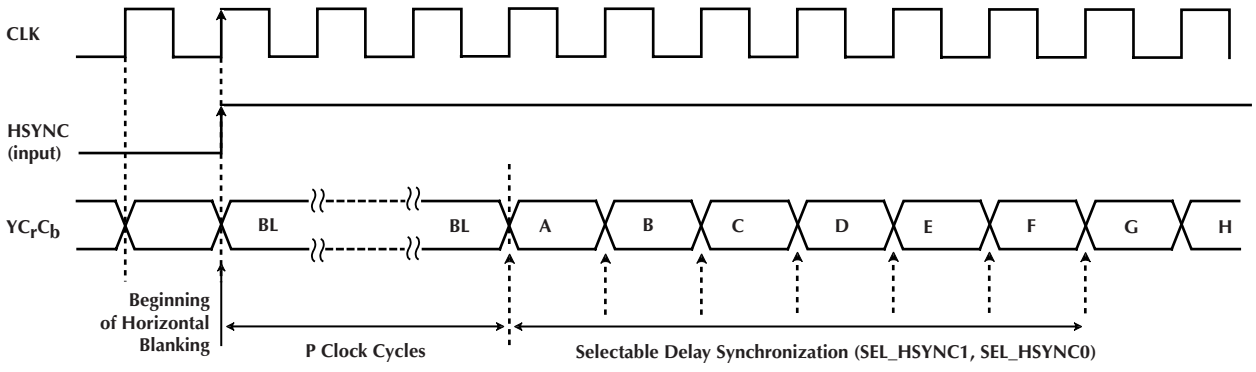
Figure 7a. Pixel Synchronization. For External Mode, Active Edge at Beginning of Active Video. (HRESET_MODE = 1, SENSE_HSYNC = 1, BL = Blanked Pixel) (ANALOG_HRESET = ANALOG_HBLANK = 0 OR ANALOG_HRESET = ANALOG_HBLANK = 1)



# of Clock Cycles, P	if SELCCIR = 1	if SELCCIR = 0
If ANALOG_HBLANK = 0	244	220
If ANALOG_HBLANK = 1	252	220

		Value (SEL_HSYNC1, SEL_HSYNC0)			
		(0,0)	(0,1)	(1,0)	(1,1)
Bit	A	CB0	BL	BL	BL
	B	Y0	CB0	BL	BL
	C	CR0	Y0	CB0	BL
	D	Y1	CR0	Y0	CB0
	E	CB2	Y1	CR0	Y0
	F	Y2	CB2	Y1	CR0
	G	CR2	Y2	CB2	Y1
	H	Y3	CR2	Y2	CB2

Figure 8. Pixel Synchronization. For External Mode, Active Edge at Beginning of Horizontal Blanking. (HRESET_MODE = 0, SENSE_HSYNC = 0, BL = Blanked Pixel)



# of Clock Cycles, P	if SELCCIR = 1	if SELCCIR = 0
If ANALOG_HBLANK = 0	244	220
If ANALOG_HBLANK = 1	252	220

		Value (SEL_HSYNC1, SEL_HSYNC0)			
		(0,0)	(0,1)	(1,0)	(1,1)
Bit	A	CB0	BL	BL	BL
	B	Y0	CB0	BL	BL
	C	CR0	Y0	CB0	BL
	D	Y1	CR0	Y0	CB0
	E	CB2	Y1	CR0	Y0
	F	Y2	CB2	Y1	CR0
	G	CR2	Y2	CB2	Y1
	H	Y3	CR2	Y2	CB2

Figure 8a. Pixel Synchronization. For External Mode, Active Edge at Beginning of Horizontal Blanking. (HRESET_MODE = 0, SENSE_HSYNC = 1, BL = Blanked Pixel)

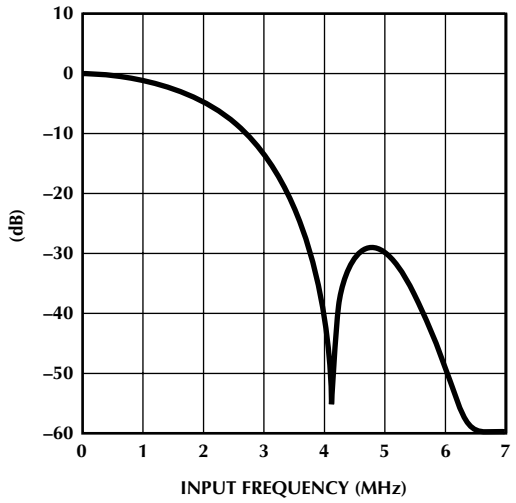


Figure 9. Chroma Bandlimit Filter: Stopband (FIR Filter)

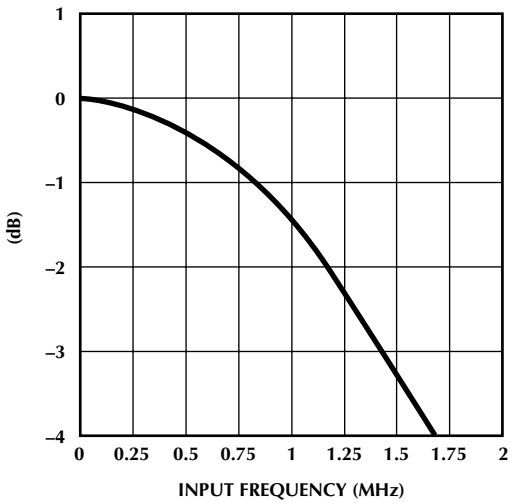


Figure 10. Chroma Bandlimit Filter: Passband (FIR Filter)

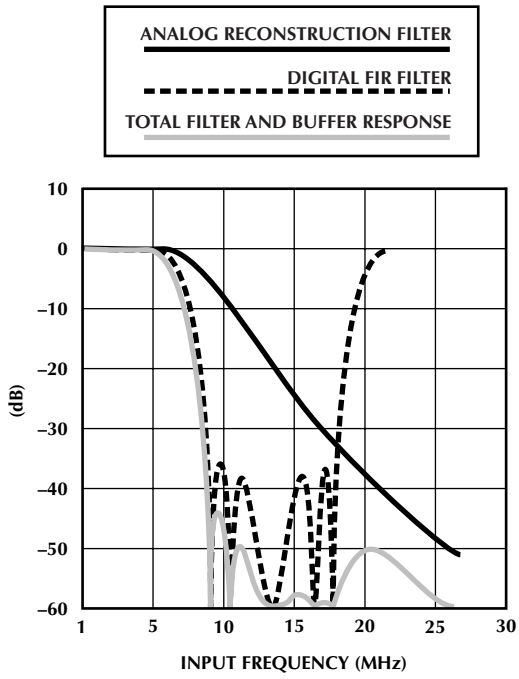


Figure 11. Reconstruction Filter: Stopband (Normalized)

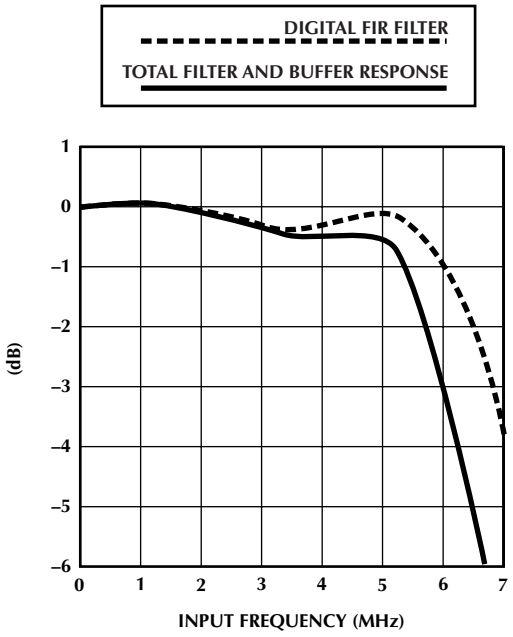


Figure 12. Reconstruction Filter: Passband (Normalized)

FUNCTIONAL DESCRIPTION (Continued)

PHASE ERROR INPUT AND CHROMA SUBCARRIER CORRECTION (FOR OVERLAY APPLICATIONS)

The chroma oscillator phase and frequency can be altered in real time using the PHERR input. This pin can receive a signal that corrects chroma variations for signals with unstable time base errors. To properly initialize the ML6461 overlay interface, follow the steps below:

1. Set the control register bit OVERLAY_ON (B16) to logical 0. This will disable the interface and let the chroma subcarrier oscillator run free.

2. Force the PHERR input to logical 0 (idle state) for at least 128 clock cycles and set the control register bit OVERLAY_ON (B16) to logical 1 while PHERR is held low. This will enable the interface.

3. Clock in the startup code of 101 and then serially (LSB first) the 32-bit frequency value FSQ (frequency number) followed by the 12-bit phase value PHQ (phase number). Equation 1 calculates color subcarrier frequency:

$$F_{SC} = \frac{F_{SQ}}{2^{32}} \times \frac{F_{CLK}}{2} \qquad (1)$$

   Where F_{CLK} is the 27 MHz (or 24.54MHz) as the system clock and F_{SC} is the actual color subcarrier frequency.

4. To turn-off the interface and have the subcarrier oscillator on free run, the control register bit OVERLAY_ON (B16) must be reset to logical 0.

5. When this function is disabled, the internal default values for F_{SQ} are:
   0X 43E0F7AD for CCIR656
   0X 4AAAAA0B for Square Pixel.

CLOSED CAPTIONING

The ML6461 enables the transmission of VBI Closed Caption codes on lines 21 and 284. To properly initialize the closed caption interface, follow the steps below:

1. Set the control register bits CC_21 (B19) and CC_284 (B18) to logical 0. This will disable transmission of Closed Caption (CC) data.

2. For each line, write the two byte closed caption (CC) data, including the parity bit, to the CC data register through the serial bus interface. Note that the ML6461 does not generate the parity bits. If only line 21 or line 284 transmission is desired, only two bytes of data are needed per frame. If both lines are used for transmission, then four bytes (the first two bytes corresponding to line 21) must be entered all at once into the closed caption data register (CC register).

3. Set the control register bits CC_21 (B19) and/or CC_284 (B18) to logical 1. This will enable CC transmission at the desired lines.

4. Repeat STEP 2 as many times as needed.

Note that CC data is transmitted once (twice if both lines are used) per frame. Hence attempts to transmit CC data at a rate faster than four bytes per frame will result on overwriting some of the previously entered data before the encoder has a chance to transmit. To prevent overwriting of data, the CC controller and the ML6461 need to be synchronized. This can be easily achieved by polling the vertical blanking pulse and updating the CC data registers once per frame during the vertical blanking interval or any appropriate interval which does not include lines 21 or 284. Also, active video information is blanked on lines for which closed caption transmission is enabled. Note that the last data written on the CC registers will be sent continuously once per frame (on line 21 or line 284 depending on the mode chosen) until the interface is disabled. Figure 13 shows Closed Caption waveforms for various modes. See Table 7 and Figure 17 for more Closed Caption information. Note that parity bits A7, A15, A23, and A31 must be generated externally.

PROGRAMMING INTERFACE

The ML6461 can be programmed either through PRESET modes or through SERIAL BUS mode.

REGISTER INFORMATION

See Table 6 for ML6461 register summary information.

CONTROL REGISTERS: DESCRIPTION OF FUNCTION

Reserved, B31:B30 These bits are reserved and must be set to 1 (B31=B30=1) for normal operation.

CBLANK, B29 In master mode, and internal slave mode, a composite blanking signal is also available thru the HSYNC pin. This can be activated via the CBLANK bit (B29=1). The polarity of the composite blanking signal is programmable thru the SENSE_HSYNC bit (B15). When the SENSE_HSYNC bit is set (B15=1), the ML6461 will output a logic 0 at the HSYNC pin during the pixels which are blanked. Conversely, when the SENSE_HSYNC bit is cleared (B15=0), the ML6461 will output a logic 1 at the HSYNC pin during the pixels which are blanked. Consequently, the YCRCB<7:0> inputs will be ignored and a constant blanking level will be output to the analog channels YOUT, COUT, and CVOUT. The operation of the VSYNC and FIELD pins are not affected by the settings of CBLANK and SENSE_HSYNC.

SLAVE/MASTER, B28 This bit determines if device operates in master or slave modes. Configuration of HSYNC, VSYNC and FIELD are determined upon selection of this bit. Table 3 provides a summary of Slave / Master modes. When this bit is set (B28=1), the ML6461 is in slave mode. When this bit is cleared (B28=0), the ML6461 is in master mode. Special note for slave modes: this bit (B28) along with the SLAVE_MODE bit (B26)

FUNCTIONAL DESCRIPTION (Continued)

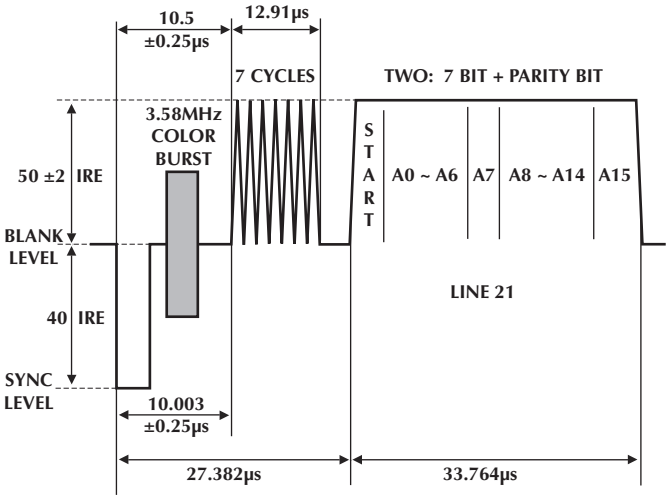
selects between internal (B26=1) and external slave modes (B26=0).

SELCCIR, B27 This bit determines the frequency of choice between CCIR656 clock rate(27MHz) and Square Pixel clock rate (24.54MHz). When this bit is set (B27=1), CCIR656 clock rate is selected. When this bit is cleared (B27=0), the Square Pixel clock rate is selected.

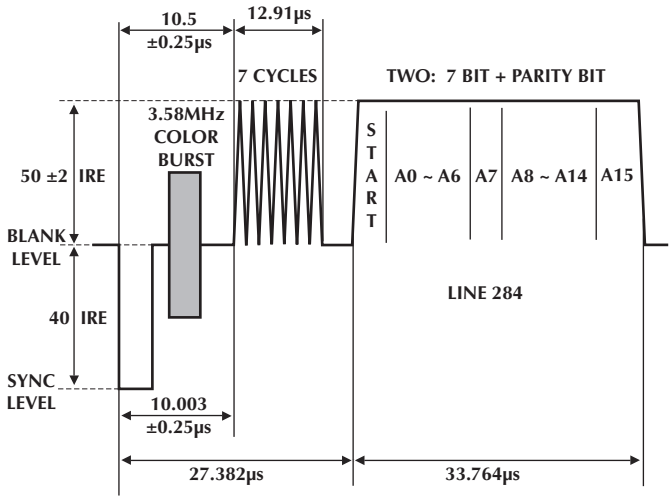
SLAVE_MODE, B26 This bit determines the choice of two slave modes: internal slave mode or external slave mode. In internal slave mode (B26=1), horizontal and vertical timing information is embedded in the YCrCb data (via SAV / EAV codes); while the HSYNC and VSYNC pins can be used as outputs. In external slave mode (B26=0), horizontal and vertical sync pulses must be provided for timing and synchronization;in this case HSYNC and VSYNC pins are inputs. See Table 3.

HRESET_MODE, B25 This bit determines whether the HSYNC is given at the beginning of active video (B25=1) or HSYNC is given at the beginning of blanking (B25=0). This bit (B25) is only available for external slave modes.

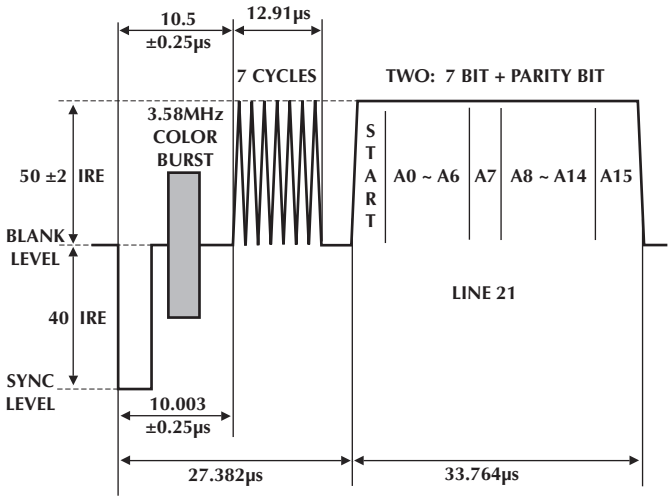
ANALOG_HBLANK, B24 This bit determines whether the ML6461 is to encode for ITU_R656_compliant "digital" or ITU_/SMPTE_compliant "analog" encoding specifications. When this bit is cleared (B24=0), the ML6461 is optimized for full "digital" line encoding, where the number of active pixels is 720 for CCIR656 rates and 640 for square pixel rates. No tapering (edge

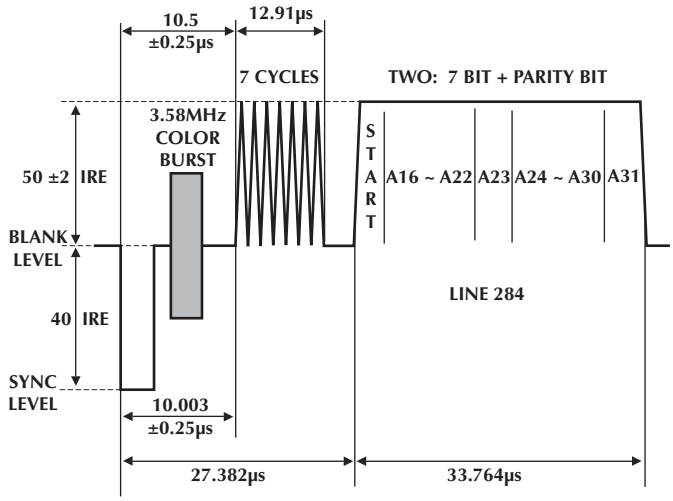


Closed Caption on Line21
[CC_21 = 1 and CC_284 = 0]



Closed Caption on Line284
[CC_21 = 0 and CC_284 = 1]





Closed Caption on Line21 and Line 284
[CC_21 = 1 and CC_284 = 1]

Figure 13. Closed Caption on Line 21 and Line 284.

FUNCTIONAL DESCRIPTION (Continued)

smoothing) is done to the beginning and end of the active portion of the line. When this bit is set (B24=1), the ML6461 is optimized for "analog" line encoding, where the number of active pixels is 712 for CCIR656 rates and 640 for square pixel rates. The beginning and end of the active video portion of the line is tapered (smoothed) to minimize ringing introduced due to fast transitions. Figure 14 below illustrates the timing comparisons.

Note: For the square pixel rate the only difference between "analog" and "digital" encoding is the tapering (smoothing) at the beginning and end of the active video portion of the line. The number of pixels encoded during the active video portion is the same in both cases. The positioning of the active portion is the same as in "analog" line encoding.

ANALOG_HRESET, B23 This bit is active only in external slave mode and when the external sync is given at the beginning of active video. In this mode, ANALOG_HRESET (B23) must be used in conjunction with ANALOG_HBLANK (B23) to choose between "analog" and digital" line encoding. The possible approaches are summarized in Table 4 below.

FULL_BAR, B22 This bit is used to program the ML6461 to encode in normal modes or 100% amplitude video (100% color bar). When this bit is set (B22=1), the ML6461 is ready to handle 100% color bars. With 75% amplitude signals, this bit should be cleared (B22=0) for optimum signal to noise performance.

JAPAN_BLANK, B21 This bit is used to program the ML6461 to encode Japanese NTSC by removing the 7.5 IRE setup in blanking and thus boosting the gain of luma and chroma DACs. This bit is set (B21=1) to handle Japanese NTSC modes.

WIDE_VBLANK, B20 Determines which lines to blank at the beginning of each field. For wide blanking, this bit is set (B20=1), the ML6461 provides 15 lines of blanking. For narrow blanking, this bit is cleared (B20=0), the ML6461 provides 9 lines of blanking.

CC_21, B19 This bit enables (B19=1) and disables (B19=0) the transmission of closed captioning data on line 21.

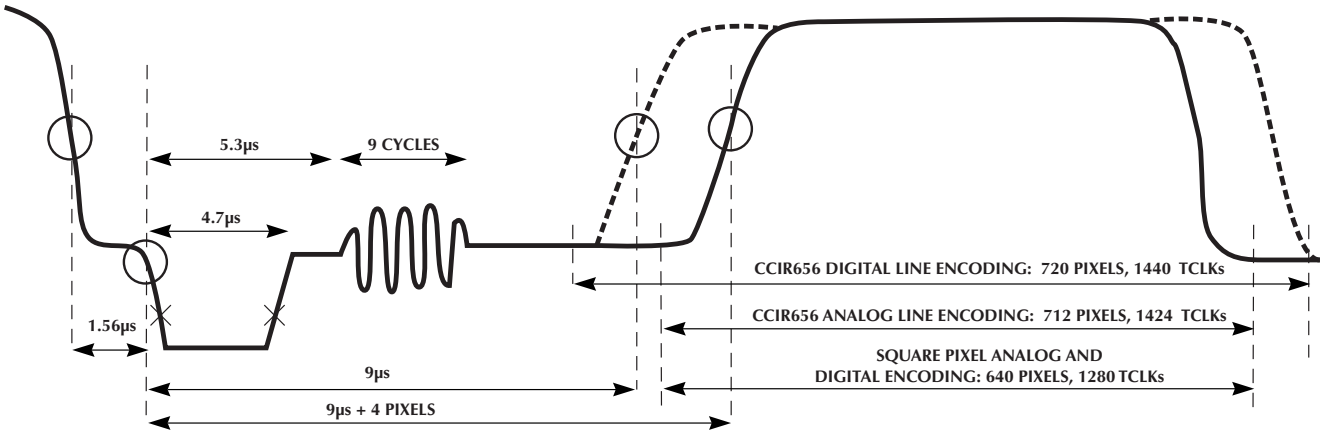


Figure 14. Timing of Horizontal Blanking Interval and Active Video

ANALOG_ HRESET B23	ANALOG_ HBLANK B24	RECOMMENDED ENCODING	TIME BETWEEN H_SYNC AND ACTIVE VIDEO	PIXELS ENCODED CCIR 656	PIXELS ENCODED SQUARE PIXEL	EDGE SMOOTHING (B24 = 1)
0	0	ITU-R656 Digital TV Line	9µs	720	640	none
0	1	Optional	9µs + 4pixels = 9.3µs	712 **See Note 1**	640	Yes
1	0	Not Recommended				
1	1	ITU-R/SMPTE Analog	9µs + 4pixels = 9.3µs	712 **See Note 2**	640	Yes

Note 1: Ignore first four and last four pixels.

Note 2: Ignore last eight pixels.

Table 4. Video Encoding Standards and Horizontal/Active Video Timing

FUNCTIONAL DESCRIPTION (Continued)

CC_284, B18 This bit enables (B18=1) and disables (B18=0) the transmission of closed caption data on line 284.

FSYNC, B17 This bit enables (B17=1) and disables (B17=0) frame syncing.

OVERLAY_ON, B16 This bit enables (B16=1) and disables (B17=0) the PHERR pin to be used as an interface to set the internal subcarrier oscillator's phase and frequency.

SENSE_HSYNC, B15 This bit selects the polarity of the HSYNC active edge to a rising edge (if B15=1) or a falling edge (if B15=0). This bit is active in master modes or in external slave modes. In internal slave modes HSYNC is configured as an output to be used for monitoring purposes. The polarity is still affected by this bit.

SEL_HSYNC1, B14 This bit, in conjunction with SEL_HSYNC0 (B13), is used to facilitate pixel synchronization. Figures 4, 5, 7, and 8 provide a detailed description. This bit is only active in master modes or in external slave modes. This bit is de-activated in internal slave modes.

SEL_HSYNC0, B13 This bit, in conjunction with SEL_HSYNC1 (B14), is used to facilitate pixel synchronization. Figures Figures 4, 5, 7, and 8 provide a detailed description. This bit is only active in master modes or in external slave modes. This bit is de-activated in internal slave modes.

SWITCH_UV, B12 This bit is used to switch Cr and Cb internally when set (B12=1). This bit is cleared (B12=0) for normal operation. This bit is intended for debug purposes only. If used, there may be some slight artifacts at the end of active line.

SWITCH_FIELD, B11 This bit is used to switch even/odd fields when set (B11=1). This bit is cleared (B12=0) for normal operation. This bit is only active in internal slave mode.

SENSE_VSYNC, B10 This bit selects the polarity of the VSYNC active edge to a rising edge (if B10=1) or a falling edge (if B10=0). In internal slave modes VSYNC is configured as an output to be used for monitoring purposes. The polarity is still affected by this bit.

YDEL1 (B7)	YDEL0 (B6)	OPERATION
0	0	Normal
0	1	Delay Luma Channel by 1 TCLK
1	0	Advance Luma Channel by 1 TCLK
1	1	Advance Luma Channel by 2 TCLK

Table 5. Luma Delay Selection

FLD_FRM_MODE, B9 When set (B9=1), it causes the ML6461 FIELD pin to give analog field information if the FIELD pin is configured as an output (see B8). When cleared (B9=0), it causes the field pin to give odd/even field information if the FIELD pin is configured as an output (see B8).

FRAME_MODE, B8 This bit configures the FIELD pin of the ML6461 as an input (if B8=1) or as an output (if B8=0).

YDEL1, B7 This bit, in conjunction with YDEL0 (B6), is used to select luma delay in order to align luma and chroma data. See Table 5.

YDEL0, B6 This bit, in conjunction with YDEL1 (B7), is used to select luma delay in order to align luma and chroma data. See Table 5.

BURST_ON, B5 When active (B5=1) this bit provides burst at all times for testing purposes only. For normal operation this bit is cleared (B5=0).

ACTIVE_ON, B4 When active (B4=1) this bit eliminates horizontal and vertical blanking intervals. Burst is suppressed. For testing purposes only. For normal operation this bit is cleared (B4=0).

FIX_SCH, B3 When active (B3=1) this bit maintains SCH phase. In this condition known as a "coherent subcarrier" such that the subcarrier has a known phase relative to the active edge of HSYNC pulse. When this bit is cleared (B3=0), the subcarrier generation block is in free run mode. This condition is known as "incoherent subcarrier" where the phase of the subcarrier relative to the HSYNC is not fixed.

CC_ALL, B2 When active (B2=1) this bit enables closed caption transmission on every line. For testing purposes only. For normal operation this bit is cleared (B2=0) and closed caption is enabled through control register bits CC_21 (B19) and CC_284 (B18).

SUBCARRIER_OFF, B1 When active (B1=1) this bit disables the internal subcarrier oscillator. Used for test purposes only. For normal operation this bit is cleared (B1=0).

AC_DC, B0 This bit configures the output buffers for AC coupled drive (if B0=1) and DC couple drive (if B0=0).

	DATA BIT	NAME	DESCRIPTION	BIT CODE RANGE
LOWER BYTE	B0	AC_DC	Configures analog output buffers for AC or DC drive	0 = DC, 1 = AC
	B1	SUBCARRIER_OFF	Disable internal subcarrier oscillator - for test only	0 = Normal, 1= Disable oscillator
	B2	CC_ALL	Enables Closed Caption transmission on every line	0 = Normal, 1 = Enable
	B3	FIX_SCH	Enable reset of subcarrier oscillator every other frame to maintain SCH phase	0 = Not reset, 1 = Oscillator reset
	B4	ACTIVE_ON	Eliminate H & V intervals, suppress burst — for test only	0 = Normal, 1 = Test Mode
	B5	BURST ON	Burst Available at all time — For test only	0 = Normal, 1 = Test Mode
	B6	YDEL0	Delay/Advance luma channel	<YDEL1, YDEL0> = 00 = Normal <YDEL1, YDEL0> = 01= Delay luma 1 clock cycle
	B7	YDEL1	Delay/Advance luma channel	<YDEL1, YDEL0> = 10 = Advance luma 1 clock cycle, <YDEL1, YDEL0> = 11= Advance luma 2 clock cycles
LOWER MIDDLE BYTE	B8	FRAME_MODE	Configure FIELD pin as input or output	0 = output, 1= input
	B9	FLD_FRM_MODE	Configure FIELD pin to give odd/even or 1,2 and 3,4 info	0 = odd/even, 1= 1,2 or 3,4
	B10	SENSE_VSYNC	Set vertical reset pulse polarity	0 = Falling edge, 1= Rising edge
	B11	SWITCH_FIELD	Switches even/odd fields	0 = Normal, 1= switch even/odd
	B12	SWITCH_UV	Switch Cr and Cb internally	0 = Normal, 1= Switch Cr & Cb
	B13	SEL_HSYNC0	Used to facilitate pixel synchronization	See Figures 4, 5, 7, 8
	B14	SEL_HSYNC1	Used to facilitate pixel synchronization	See Figures 4, 5, 7, 8
	B15	SENSE_HSYNC	Set horizontal reset pulse polarity	0 = Falling edge, 1= Rising edge
UPPER MIDDLE BYTE	B16	OVERLAY_ON	Enables use of PHERR pin	0 = Disable, 1= Enable PHERR pin
	B17	FSYNC	Enable frame syncing	0 = Disable, 1= Enable
	B18	CC_284	Enable transmission of Closed Caption data on line 284	0 = Disable, 1= Enable transmission
	B19	CC_21	Enable transmission of Closed Caption data on line 21	0 = Disable, 1= Enable transmission
	B20	WIDE_BLANK	Select wide or narrow blanking	0 = 9 lines of blanking, 1= 15 lines
	B21	JAPAN_BLANK	Removes 7.5 IRE setup in blanking and boosts Y & C gain	0 = Normal, 1= Japanese NTSC
	B22	FULL_BAR	To handle 100% amplitude video (100% colorbars)	0 = Normal, 1 handles 100%Amp. Video
	B23	ANALOG_HRESET	Selects position of horizontal reset	0 = Digital H blank edge, 1= Analog H blank edge
UPPER BYTE	B24	ANALOG_HBLANK	Select analog blanking with smooth transition at the edges or digital blanking	0 = Digital blanking, 1= Analog blanking
	B25	HRESET_MODE	Select H reset at start of active video or start of H blanking	0 = Start of blanking, 1= Start of active
	B26	SLAVE_MODE	Select external H/V reset or embedded H/V reset	0=External H/V reset (H/V ext. source) 1=Embedded H/V reset (SAV/EAV codes)
	B27	SELCCIR	Select CCIR656 rate or Square Pixel rate	0 = Square Pixel, 1= CCIR656
	B28	SLAVE/MASTER	Select slave or master mode	0 = Master mode, 1= Slave mode
	B29	CBLANK	Composite Blanking	0 = Disable, 1= Enable
	B30	Reserved	Set to 1 for Proper Operation	
	B31	Reserved	Set to1 for Proper Operation	

Note: B31 is MSB

Table 6: Control Register (CNTR) Summary

	DATA BIT	NAME	DESCRIPTION	CC-21=1; CC-284=0	CC21=0; CC-284=1	CC21=1; CC-284=1
LOWER BYTE	A0	CC0	Closed Caption bit 0	line 21	line 284	line 21
	A1	CC1	Closed Caption bit 1	line 21	line 284	line 21
	A2	CC2	Closed Caption bit 2	line 21	line 284	line 21
	A3	CC3	Closed Caption bit 3	line 21	line 284	line 21
	A4	CC4	Closed Caption bit 4	line 21	line 284	line 21
	A5	CC5	Closed Caption bit 5	line 21	line 284	line 21
	A6	CC6	Closed Caption bit 6	line 21	line 284	line 21
	A7	CC7	Closed Caption bit 7	line 21	line 284	line 21
LOWER MIDDLE BYTE	A8	CC8	Closed Caption bit 8	line 21	line 284	line 21
	A9	CC9	Closed Caption bit 9	line 21	line 284	line 21
	A10	CC10	Closed Caption bit 10	line 21	line 284	line 21
	A11	CC11	Closed Caption bit 11	line 21	line 284	line 21
	A12	CC12	Closed Caption bit 12	line 21	line 284	line 21
	A13	CC13	Closed Caption bit 13	line 21	line 284	line 21
	A14	CC14	Closed Caption bit 14	line 21	line 284	line 21
	A15	CC15	Closed Caption bit 15	line 21	line 284	line 21
UPPER MIDDLE BYTE	A16	CC16	Closed Caption bit 0	X	X	line 284
	A17	CC17	Closed Caption bit 1	X	X	line 284
	A18	CC18	Closed Caption bit 2	X	X	line 284
	A19	CC19	Closed Caption bit 3	X	X	line 284
	A20	CC20	Closed Caption bit 4	X	X	line 284
	A21	CC21	Closed Caption bit 5	X	X	line 284
	A22	CC22	Closed Caption bit 6	X	X	line 284
	A23	CC23	Closed Caption bit 7	X	X	line 284
UPPER BYTE	A24	CC24	Closed Caption bit 8	X	X	line 284
	A25	CC25	Closed Caption bit 9	X	X	line 284
	A26	CC26	Closed Caption bit 10	X	X	line 284
	A27	CC27	Closed Caption bit 11	X	X	line 284
	A28	CC28	Closed Caption bit 12	X	X	line 284
	A29	CC29	Closed Caption bit 13	X	X	line 284
	A30	CC30	Closed Caption bit 14	X	X	line 284
	A31	CC31	Closed Caption bit 15	X	X	line 284

Note: A31 is MSB

Table 7. Closed Caption (CC) Register Summary

FUNCTIONAL DESCRIPTION (Continued)

PRESET PIN CONTROL

The ML6461 can be controlled by a pair of preset mode pins. These pins do not allow access to all of the programmable features of the ML6461, but are intended to provide a simpler interface for most applications. Refer to Table 8 for preset modes.

SERIAL BUS OPERATION

The serial bus control in the ML6461 has two levels of addressing: Device Addressing and Functional Addressing.

Device Addressing: Figures 15, 16, and 17 show the physical waveforms generated in order to address the ML6461. There are six basic parts of the waveform:

1. Start Indication: Clock Cycle 0
2. Device Address Shifted in: Clock Cycle 1 through 8
3. Device Address Strobed and Decoded: Clock Cycle 9
4. Function Address Shifted in: Clock Cycle 10 through 17
5. Function Address Strobed and Decoded: Clock Cycle 18
6. Data Shifted in 8 bits at a time, MSB first: Clock Cycle 19 through 26
7. Data Shifted: Clock Cycle 27
8. Repeat strep 6 & 7 until all data is clocked in.
9. Stop indication: After Last Clock Cycle (54 for CC, 54 for CNTR)

Note: data at SDATA is ignored at steps 3, 5, and 7.

Device & Function Addressing: Figures 15, 16, an17 show the register address procedure of the ML6461.

Device Address (8 bit)

1011 0100 (Hex = B4)

Function Address (8 bit)

Closed Caption Data Registers (CC): 0000 0000 (Hex = 00)
Control Registers (CNTR): 0000 0011 (Hex = 03)

Number of Data Bits

Closed Caption Data Registers (CC): 4 x 8 bits
Control Registers (CNTR): 4 x 8 bits

CONTROL REGISTER DEFAULT SETTINGS

At Power up, the ML6461 default settings are as follows:

- Control Register is undefined when the serial bus mode is enabled.
- Chip is ready to process video
- Preset Pins are available and if used will configure the control register.
- Must write logic “0” (zero) to A30 to get video

To get black at power up will require logic “1” in A30.

MODE	PRESET1	PRESET0	CC	CNTR
A	0	0	XX	XXXXXXXX
B	0	1	XX	09080209
C	1	0	XX	1C080209
D	1	1	XX	11080209

X = don't care

Mode Description

Mode A: All register contents are programmed through serial interface.
Mode B: Master mode, CCIR656 rate, analog blanking.
Mode C: Slave mode, SAV and EAV codes, CCIR656 rate, digital blanking.
Mode D: Slave mode, external sync at start of line, Square pixel rate, analog blanking

Table 8. Preset Modes and Register Values

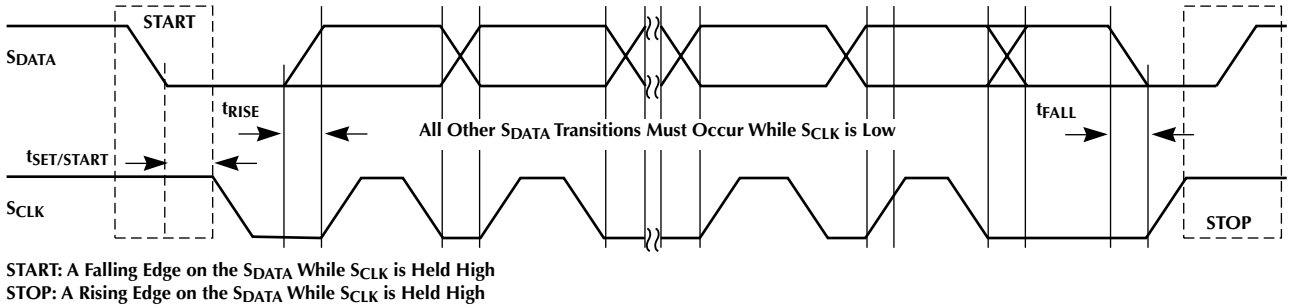


Figure 15. Definition of START & STOP on Serial Data Bus

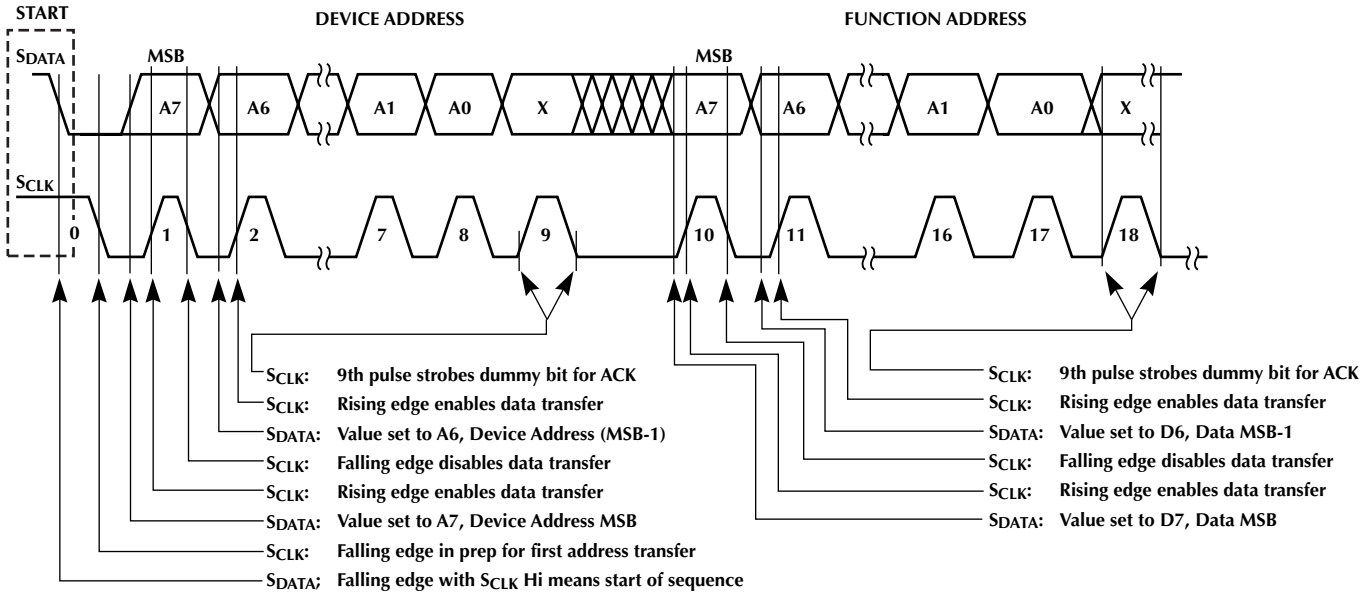


Figure 16. Definition of ADDRESS FORMAT on Serial Data Bus

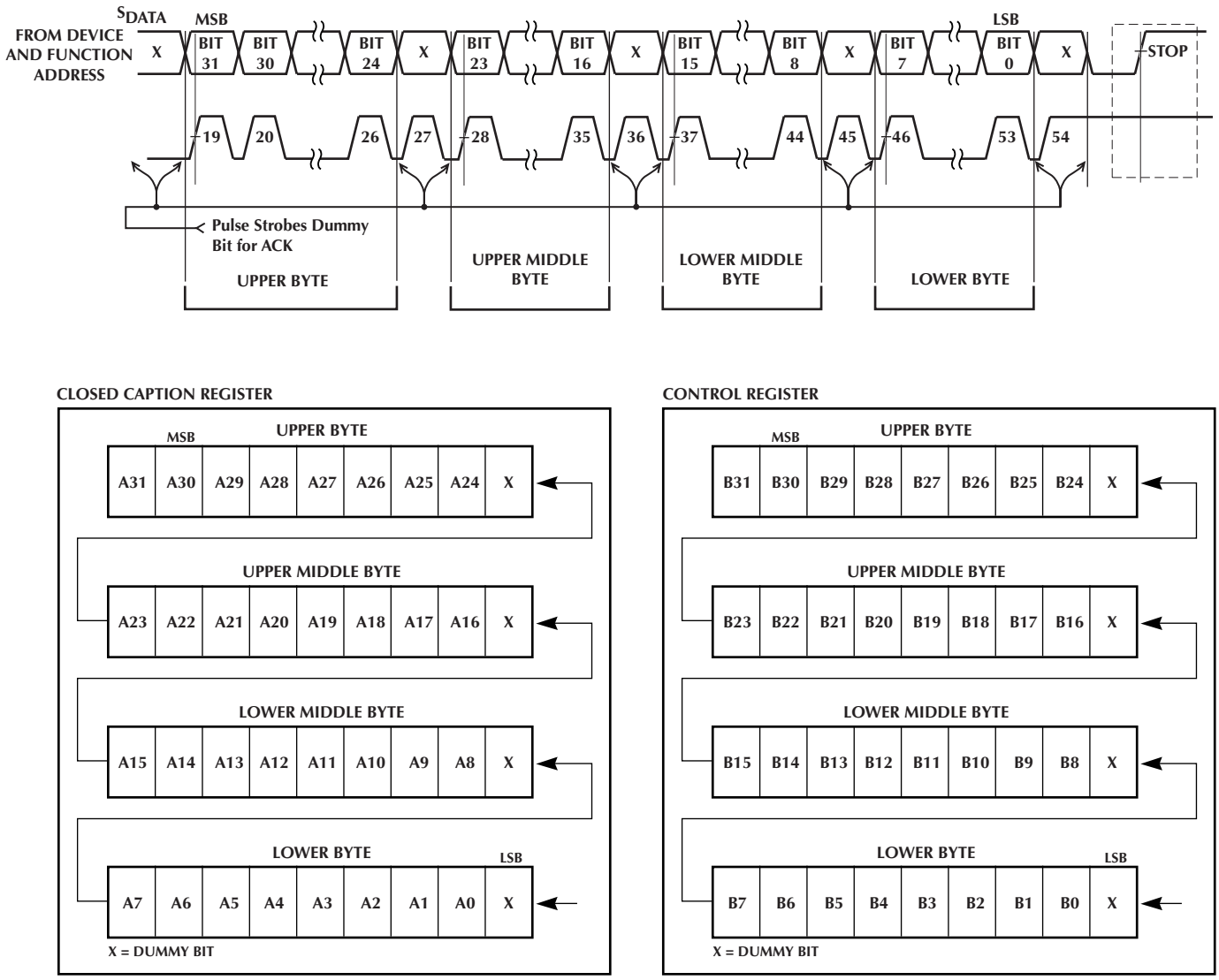


Figure 17. Register Organization and Timing

TYPICAL APPLICATIONS

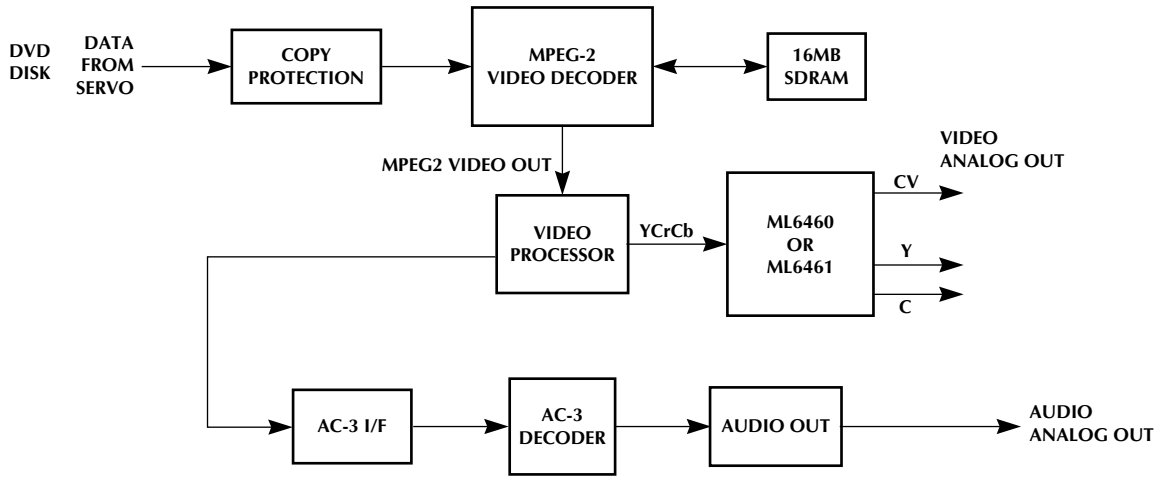


Figure 18. Typical Encoding Application (DVD Systems)

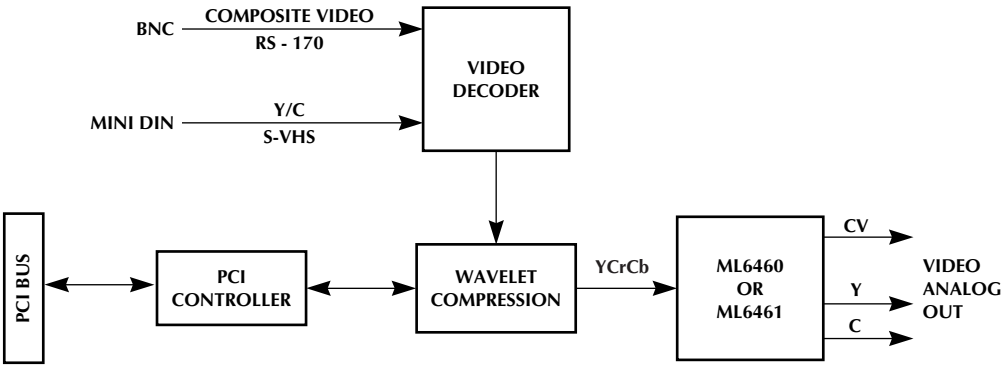


Figure 19. Typical Encoding Application (Low Cost Video Capture or Camera Systems)

TYPICAL APPLICATIONS

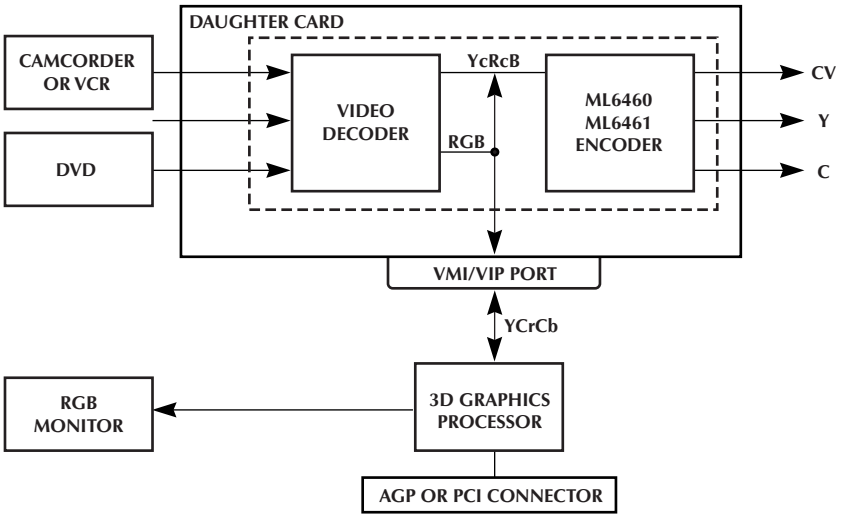


Figure 20. Typical Encoding Application (PC/TV DVD on Graphics Card)

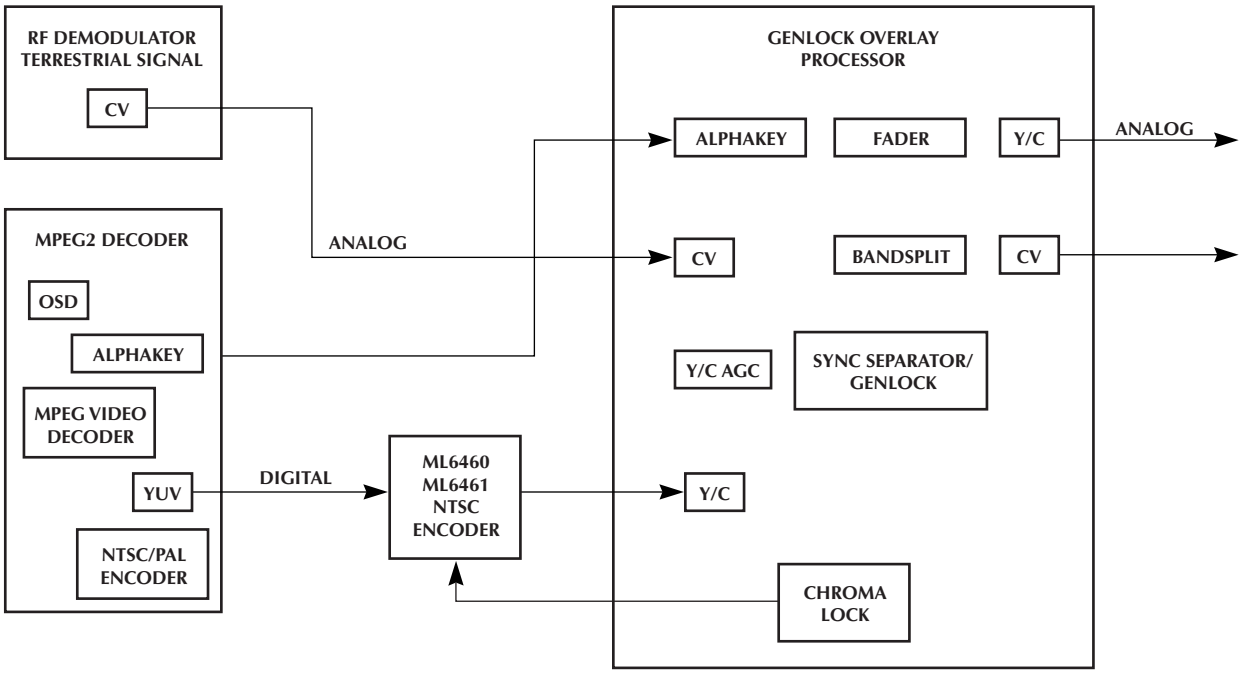


Figure 21. Typical Encoding Application (MPEG2/Overlay Systems)

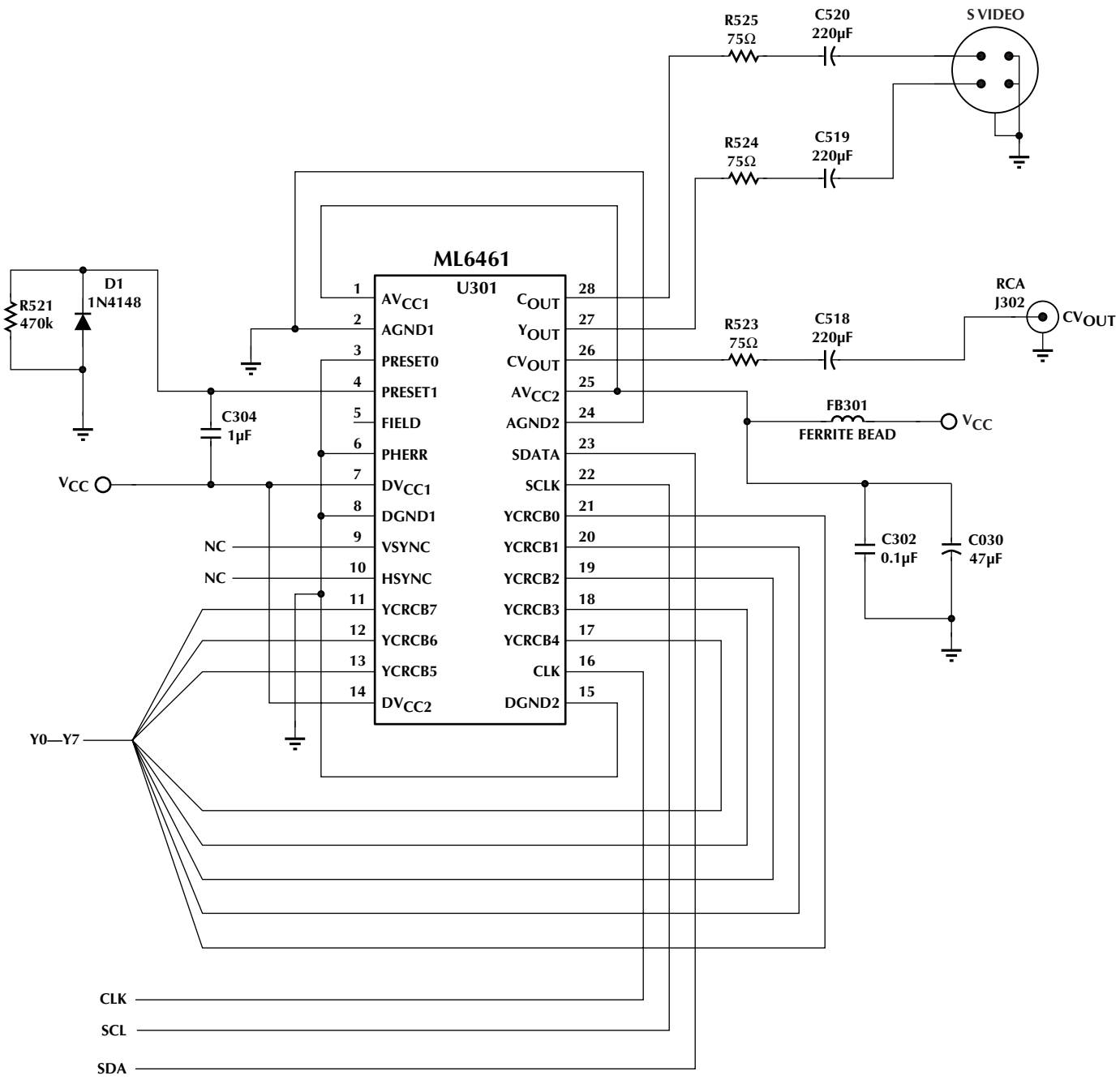
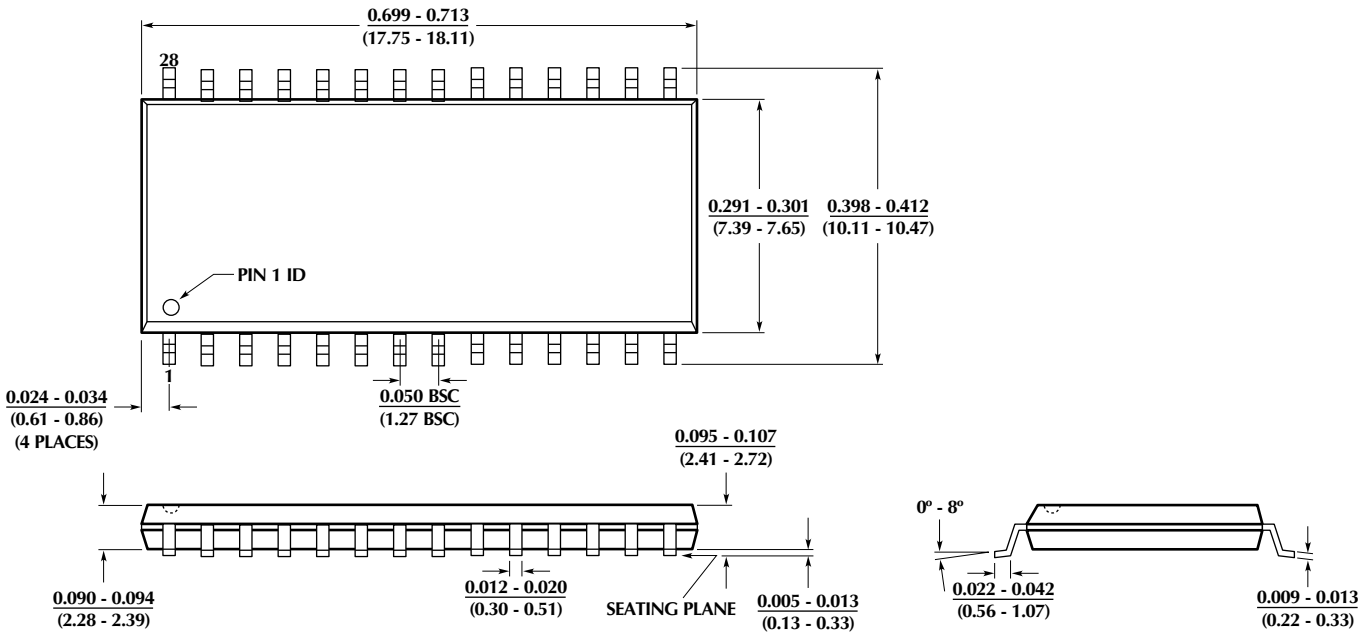


Figure 22. Typical Application Schematic

PHYSICAL DIMENSIONS inches (millimeters)

Package: S28
28-Pin SOIC



ORDERING INFORMATION

PART NUMBER	MACROVISION®	TEMPERATURE RANGE	PACKAGE
ML6461CS	YES	0°C to 70°C	28 Pin SOIC (S28)

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