Sync Separator, Low Power

The EL1881 video sync separator is manufactured using Elantec's high performance analog CMOS process. This device extracts sync timing information from both standard and non-standard video input. It provides composite sync, vertical sync, burst/back porch timing, and odd/even field detection. Fixed 70mV sync tip slicing provides sync edge detection when the video input level is between $0.5V_{P-P}$ and $-2V_{P-P}$ (sync tip amplitude 143mV to 572mV). A single external resistor sets all internal timing to adjust for various video standards. The composite sync output follows video in sync pulses and a vertical sync pulse is output on the rising edge of the first vertical serration following the vertical pre-equalizing string. For non-standard vertical inputs, a default vertical pulse is output when the vertical signal stays low for longer than the vertical sync default delay time. The odd/even output indicates field polarity detected during the vertical blanking interval. The EL1881 is plug-in compatible with the industry-standard LM1881 and can be substituted for that part in 5V applications with lower required supply current.

The EL1881 is available in the 8-pin PDIP and SO packages and is specified for operation over the full -40°C to +85°C temperature range.

Ordering Information

PART NUMBER	PACKAGE	TAPE & REEL	PKG. DWG. #
EL1881CN	8-Pin PDIP	-	MDP0031
EL1881CS	8-Pin SO	-	MDP0027
EL1881CS-T7	8-Pin SO	7"	MDP0027
EL1881CS-T13	8-Pin SO	13"	MDP0027
EL1881CSZ (See Note)	8-Pin SO (Pb-free)	-	MDP0027
EL1881CSZ-T7 (See Note)	8-Pin SO (Pb-free)	7"	MDP0027
EL1881CSZ-T13 (See Note)	8-Pin SO (Pb-free)	13"	MDP0027

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020C.

Features

- NTSC, PAL, SECAM, non-standard video sync separation
- Fixed 70mV slicing of video input levels from $0.5V_{P-P}$ to $2V_{P-P}$
- Low supply current - 1.5mA typ.
- Single +5V supply
- Composite, vertical sync output
- Odd/even field output
- Burst/back porch output
- Available in 8-pin PDIP and SO packages
- Pb-free available

Applications

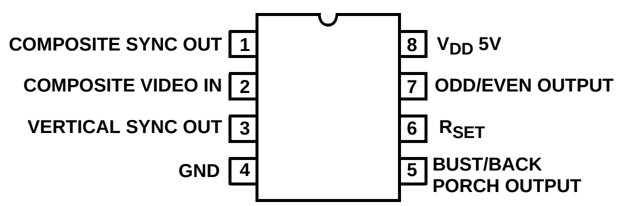
- Video amplifiers
- PCMCIA applications
- A/D drivers
- Line drivers
- Portable computers
- High-speed communications
- RGB applications
- Broadcast equipment
- Active filtering

Demo Board

A dedicated demo board is available.

Pinout

EL1881
(8-PIN PDIP, SO)
TOP VIEW



Absolute Maximum Ratings (T_A = 25°C)

V_{CC} Supply 7V
Storage Temperature. . . . .-65°C to +150°C
Pin Voltages. . . . . -0.5V to V_{CC} +0.5V
Operating Ambient Temperature Range . . . .-40°C to +85°C
Operating Junction Temperature. . . . . 150°C
Power Dissipation 400mW

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Specifications V_{DD} = 5V, T_A = 25°C, R_{SET} = 681kΩ, unless otherwise specified.

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
I_{DD}, Quiescent	V_{DD} = 5V	0.75	1.5	3	mA
Clamp Voltage	Pin 2, I_{LOAD} = -100µA	1.35	1.5	1.65	V
Clamp Discharge Current	Pin 2 = 2V	6	12	16	µA
Clamp Charge Current	Pin 2 = 1V	-1.3	-1	0.7	mA
R_{SET} Pin Reference Voltage	Pin 6	1.1	1.22	1.35	V
V_{OL} Output Low Voltage	I_{OL} = 1.6mA		0.24	0.5	V
V_{OH} Output High Voltage	I_{OH} = -40µA	4	4.8		V
	I_{OH} = -1.6mA	3	4.6		

Dynamic Specifications

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
Comp Sync Prop Delay, t_{CS}	See Figure 2	20	35	75	ns
Vertical Sync Width, t_{VS}	Normal or Default Trigger, 50%-50%	190	230	300	µs
Vertical Sync Default Delay, t_{VSD}	See Figure 3	35	62	85	µs
Burst/Back Porch Delay, t_{BD}	See Figure 2	120	200	300	ns
Burst/Back Porch Width, t_B	See Figure 2	2.5	3.5	4.5	µs
Input Dynamic Range	Video Input Amplitude to Maintain 50% Slice Spec	0.5		2	V_{P-P}
Slice Level	V_{SLICE}/V_{CLAMP}	55	70	85	mV

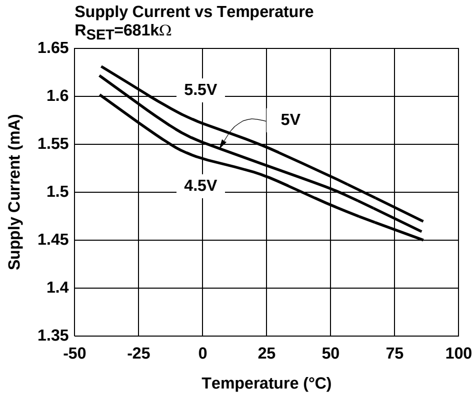
Pin Descriptions

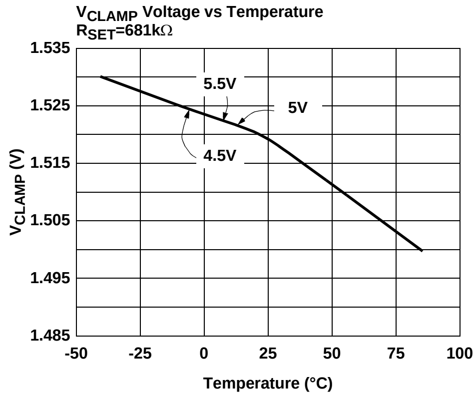
PIN NUMBER	PIN NAME	PIN FUNCTION
1	Composite Sync Out	Composite sync pulse output; sync pulses start on a falling edge and end on a rising edge
2	Composite Video In	AC coupled composite video input; sync tip must be at the lowest potential (positive picture phase)
3	Vertical Sync Out	Vertical sync pulse output; the falling edge of vert sync is the start of the vertical period
4	GND	Supply ground
5	Burst/Back Porch Output	Burst/back porch output; low during burst portion of composite video
6	RSET (Note 1)	An external resistor to ground sets all internal timing; a 681k 1% resistor will provide correct timing for NTSC signals
7	Odd/Even Output	Odd/even field output; high during odd fields, low during even fields; transitions occur at start of vert sync pulse
8	VDD 5V	Positive supply (5V)

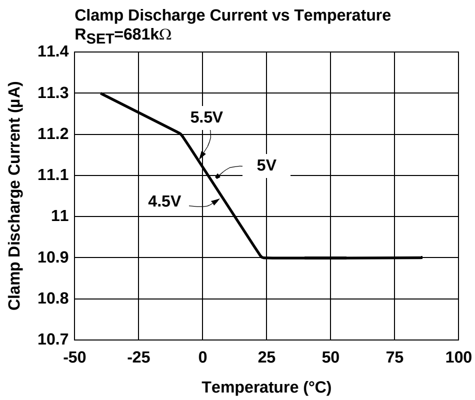
NOTE:

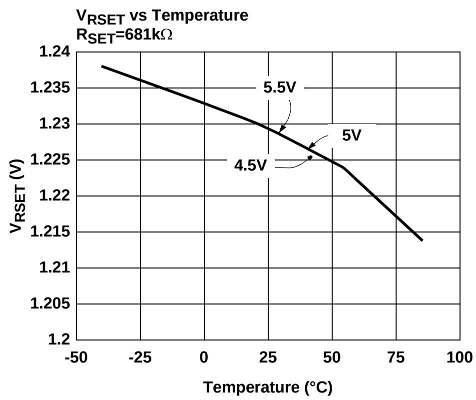
1. R_{SET} must be a 1% resistor

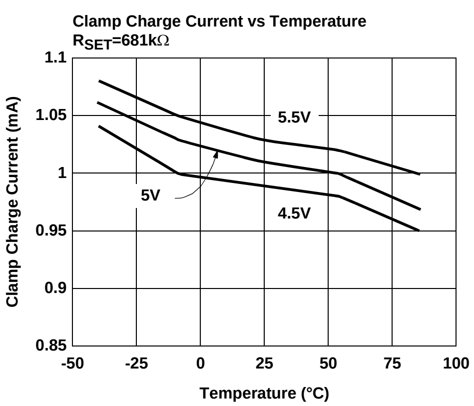
Typical Performance Curves

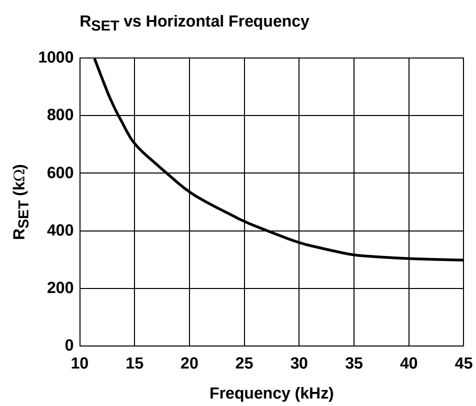






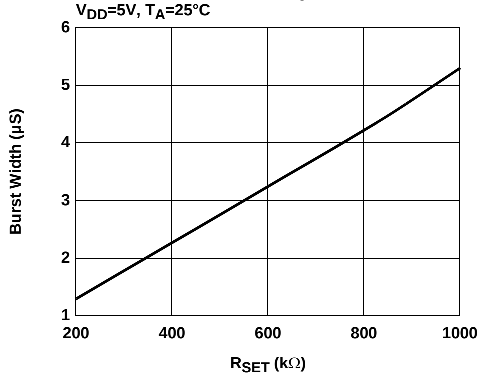




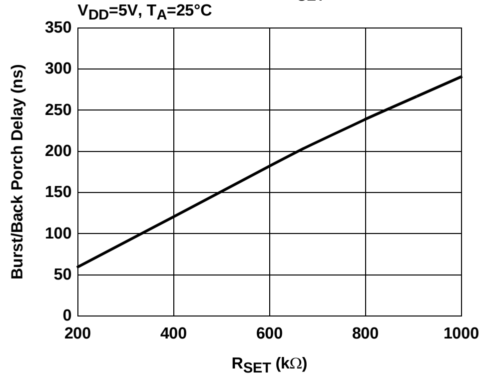


Typical Performance Curves (Continued)

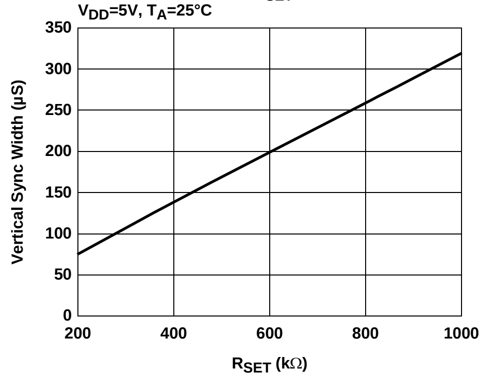
Burst/Back Porch Width vs R_{SET}
V_{DD}=5V, T_A=25°C



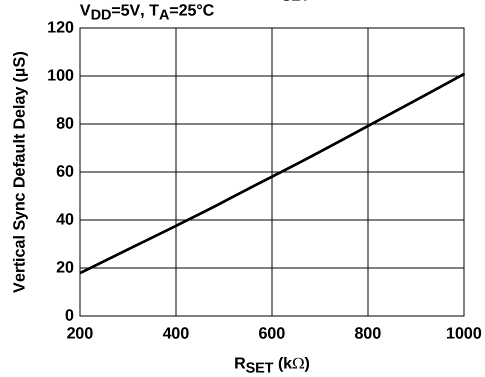
Burst/Back Porch Delay vs R_{SET}
V_{DD}=5V, T_A=25°C



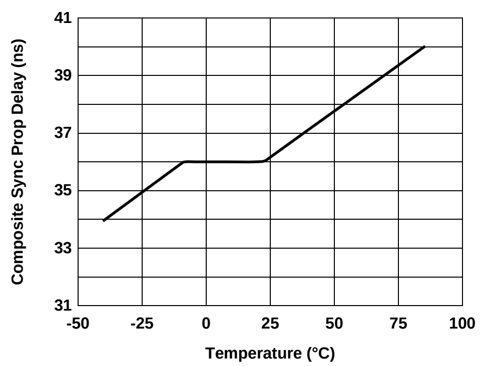
Vertical Sync Width vs R_{SET}
V_{DD}=5V, T_A=25°C



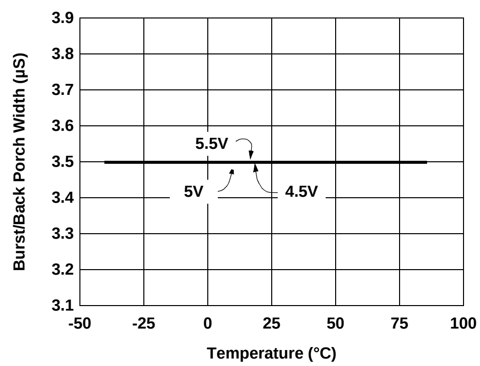
Vertical Default Delay vs R_{SET}
V_{DD}=5V, T_A=25°C



Composite Sync Prop Delay vs Temperature

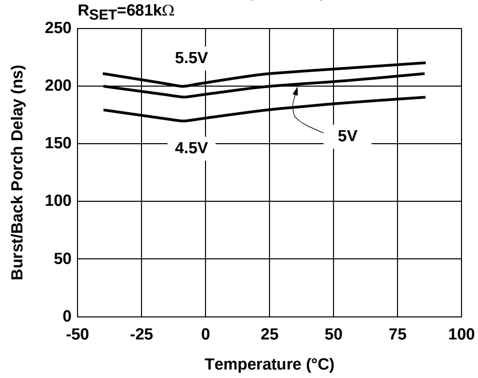


Burst/Back Porch Width vs Temperature

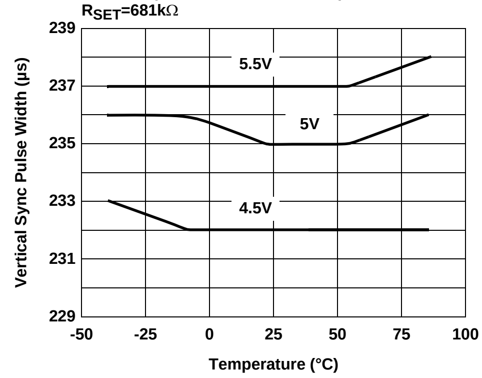


Typical Performance Curves (Continued)

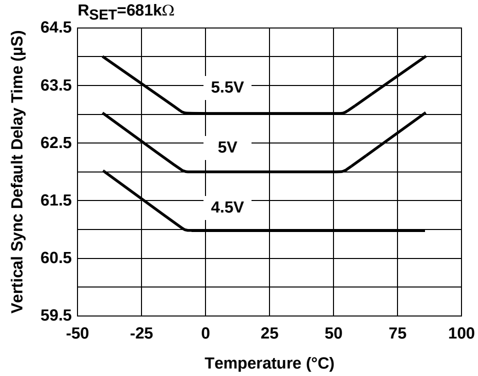
Burst/Back Porch Delay vs Temperature
R_{SET}=681kΩ



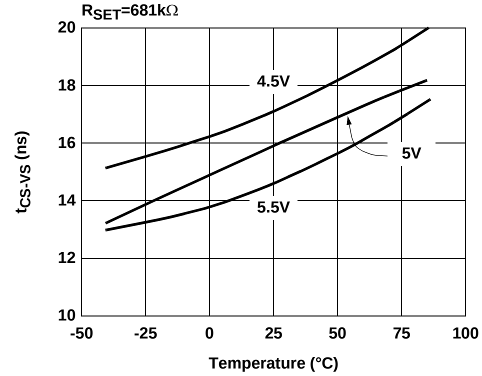
Vertical Sync Pulse Width vs Temperature
R_{SET}=681kΩ



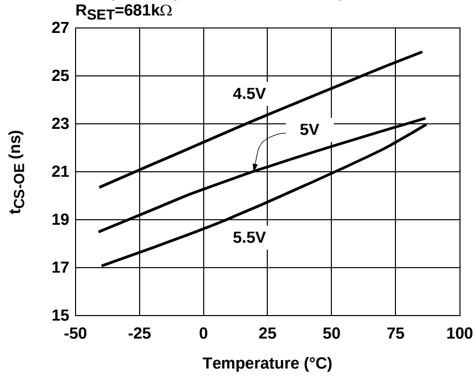
Vertical Sync Default Delay Time vs Temperature
R_{SET}=681kΩ



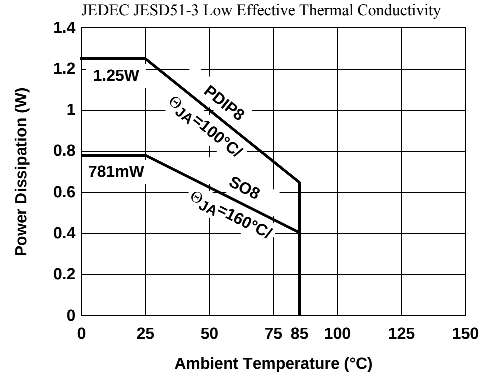
Composite Sync to Vertical Sync Delay Time
R_{SET}=681kΩ



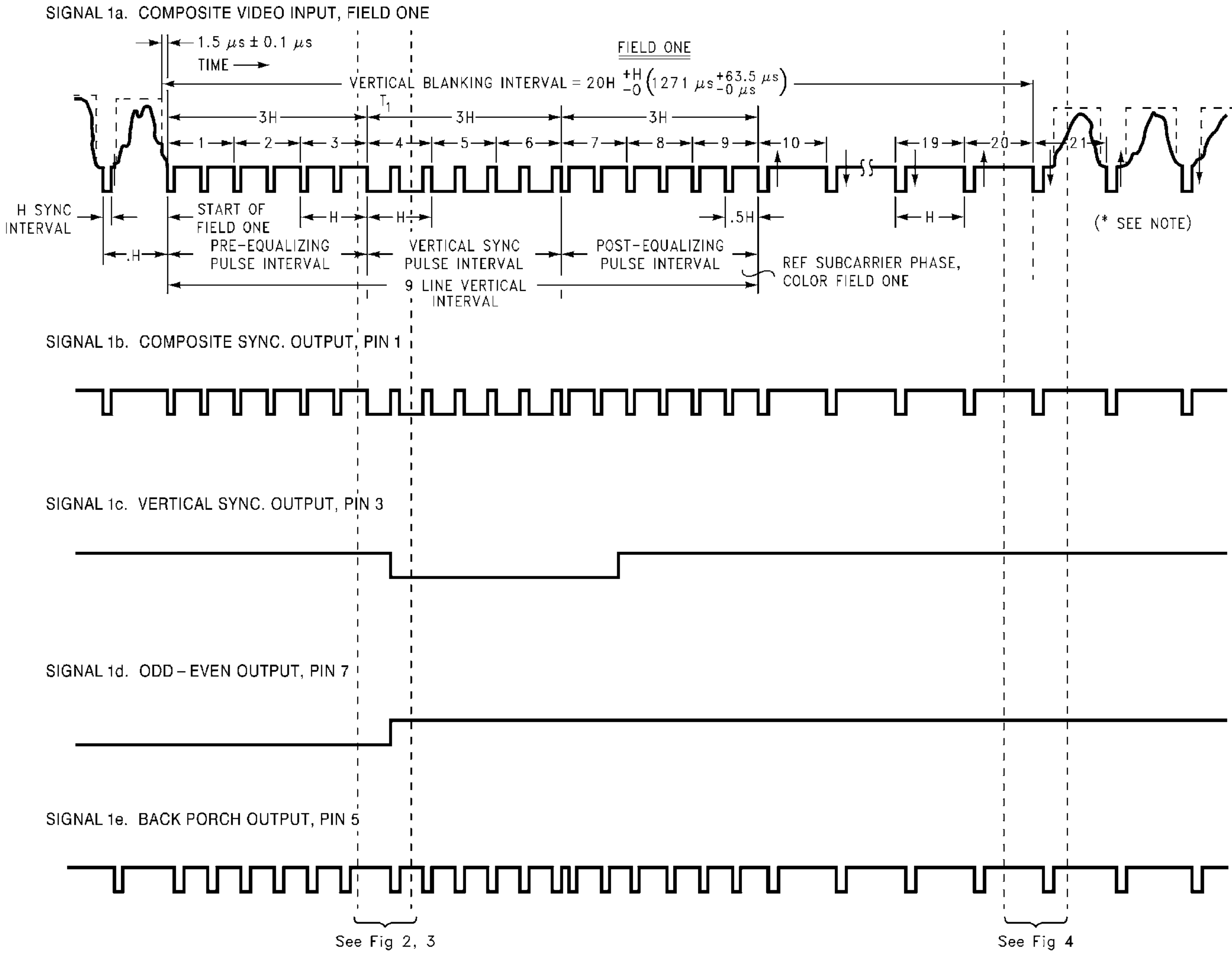
Composite Sync to Odd/Even Delay Time
R_{SET}=681kΩ



Package Power Dissipation vs Ambient Temp.
JEDEC JESD51-3 Low Effective Thermal Conductivity



Timing Diagrams



NOTES:

b. The composite sync output reproduces all the video input sync pulses, with a propagation delay.

c. Vertical sync leading edge is coincident with the first vertical serration pulse leading edge, with a propagation delay.

d. Odd-even output is low for even field, and high for odd field.

e. Back porch goes low for a fixed pulse width on the trailing edge of video input sync pulses. Note that for serration pulses during vertical, the back porch starts on the rising edge of the serration pulse (with propagation delay).

* Signal 1a drawing reproduced with permission from EIA.

FIGURE 1. STANDARD (NTSC INPUT) TIMING

Expanded Timing Diagrams

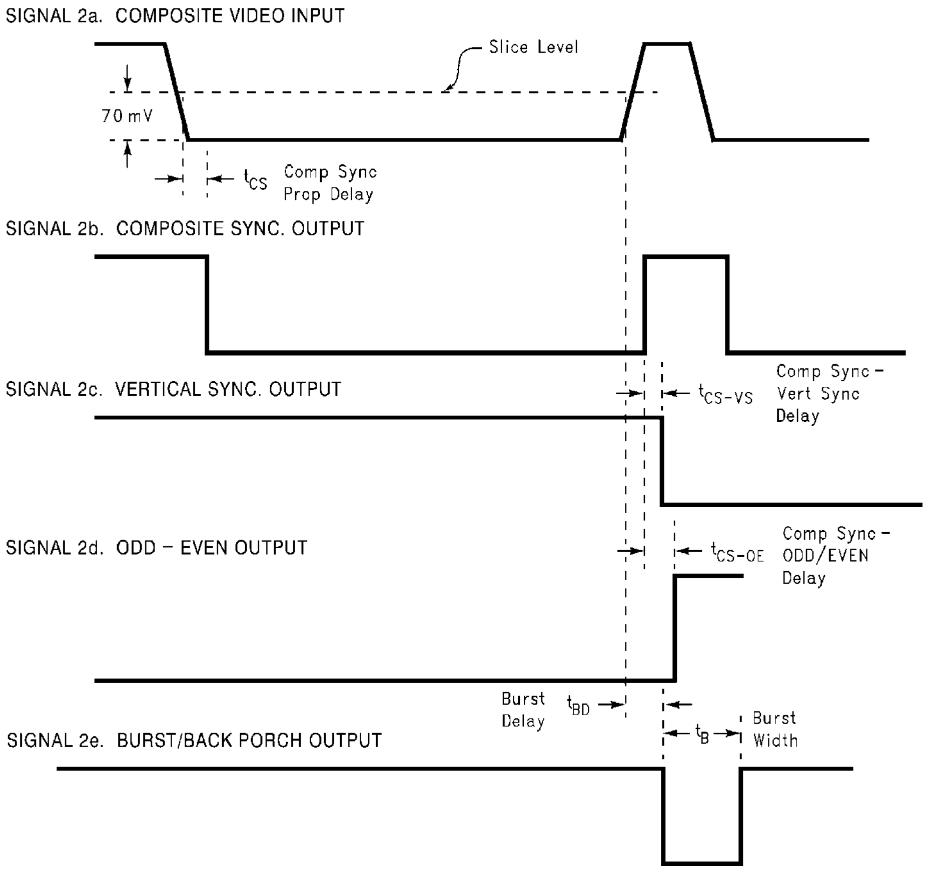


FIGURE 2. STANDARD VERTICAL TIMING

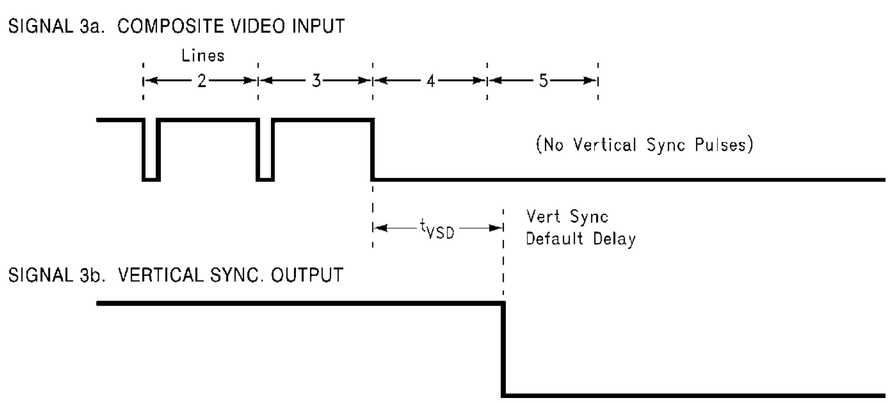


FIGURE 3. NON-STANDARD VERTICAL TIMING

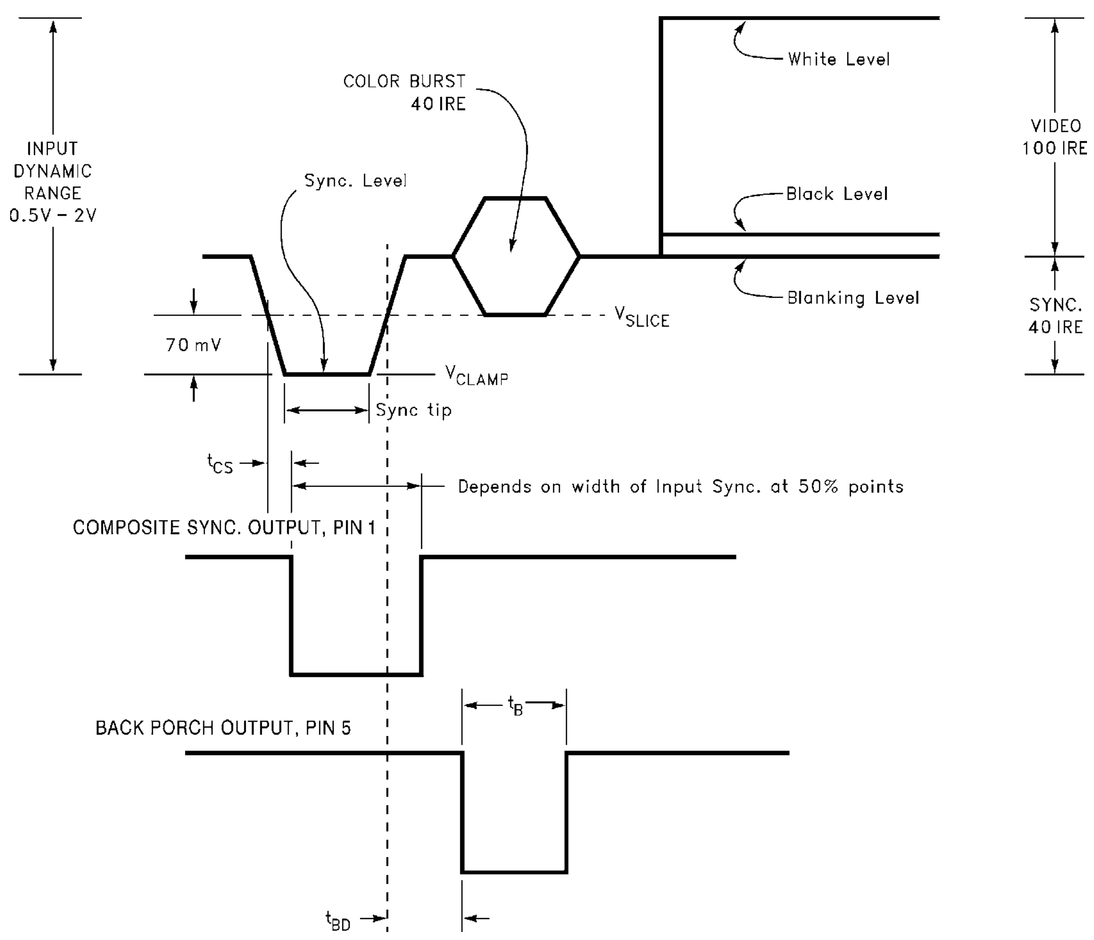


FIGURE 4. STANDARD (NTSC INPUT) H. SYNC DETAIL

Applications Information

Video In

A simplified block diagram is shown following page.

An AC coupled video signal is input to Video In pin 2 via, C_1 nominally 0.1µF. Clamp charge current will prevent the signal on pin 2 from going any more negative than Sync Tip Ref, about 1.5V. This charge current is nominally about 1mA. A clamp discharge current of about 10µA is always attempting to discharge C_1 to Sync Tip Ref, thus charge is lost between sync pulses that must be replaced during sync pulses. The droop voltage that will occur can be calculated from IT = CV, where V is the droop voltage, I is the discharge current, T is the time between sync pulses (sync period - sync tip width), and C is C_1.

An NTSC video signal has a horizontal frequency of 15.73kHz, and a sync tip width of 4.7µs. This gives a period of 63.6µs and a time T = 58.9µs. The droop voltage will then be V = 5.9mV. This is less than 2% of a nominal sync tip amplitude of 286mV. The charge represented by this droop is replaced in a time given by T = CV/I, where I = clamp charge current = 1mA. Here T = 590ns, about 12% of the sync pulse width of 4.7µs. It is important to choose C_1 large enough so that the droop voltage does not approach the switching threshold of the internal comparator.

Fixed Gain Buffer

The clamped video signal then passes to the fixed gain buffer which places the sync slice level at the equivalent level of 70mV above sync tip. The output of this buffer is presented to the comparator, along with the slice reference. The comparator output is level shifted and buffered to TTL levels, and sent out as Composite Sync to pin 1.

Burst

A low-going Burst pulse follows each rising edge of sync, and lasts approximately 3.5µs for an R_{SET} of 681kΩ.

Vertical Sync

A low-going Vertical Sync pulse is output during the start of the vertical cycle of the incoming video signal. The vertical cycle starts with a pre-equalizing phase of pulses with a duty cycle of about 93%, followed by a vertical serration phase that has a duty cycle of about 15%. Vertical Sync is clocked out of the EL1881 on the first rising edge during the vertical serration phase. In the absence of vertical serration pulses, a vertical sync pulse will be forced out after the vertical sync default delay time, approximately 60µS after the last falling edge of the vertical equalizing phase for R_{SET} = 681kΩ.

Odd/Even

Because a typical television picture is composed of two interlaced fields, there is an odd field that includes all the odd lines, and an even field that consists of the even lines. This odd/even field information is decoded by the EL1881 during the end of picture information and the beginning of vertical information. The odd/even circuit includes a T-flip-flop that is reset during full horizontal lines, but not during half lines or vertical equalization pulses. The T-flip-flop is clocked during each falling edge of these half hperiod pulses. Even fields will toggle until a low state is clocked to the odd/even pin 7 at the beginning of vertical sync, and odd fields will cause a high state to be clocked to the odd/even pin at the start of the next vertical sync pulse. Odd/even can be ignored if using non-interlaced video, as there is no change in timing from one field to the next.

R_{SET}

An external R_{SET} resistor, connected from R_{SET} pin 6 to ground, produces a reference current that is used internally as the timing reference for vertical sync width, vertical sync default delay, burst gate delay and burst width. Decreasing the value of R_{SET} increases the reference current, which in turn decreases reference times and pulse widths. A higher frequency video input necessitates a lower R_{SET} value.

Chroma Filter

A chroma filter is suggested to increase the S/N ratio of the incoming video signal. Use of the optional chroma filter is shown in Figure 5. It can be implemented very simply and inexpensively with a series resistor of 620Ω and a parallel capacitor of 500pF, which gives a single pole roll-off frequency of about 500kHz. This sufficiently attenuates the 3.58MHz (NTSC) or 4.43MHz (PAL) color burst signal, yet passes the approximately 15kHz sync signals without appreciable attenuation. A chroma filter will increase the propagation delay from the composite input to the outputs.

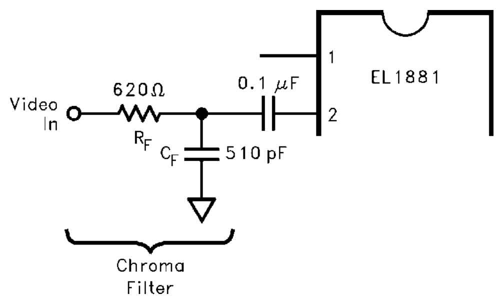
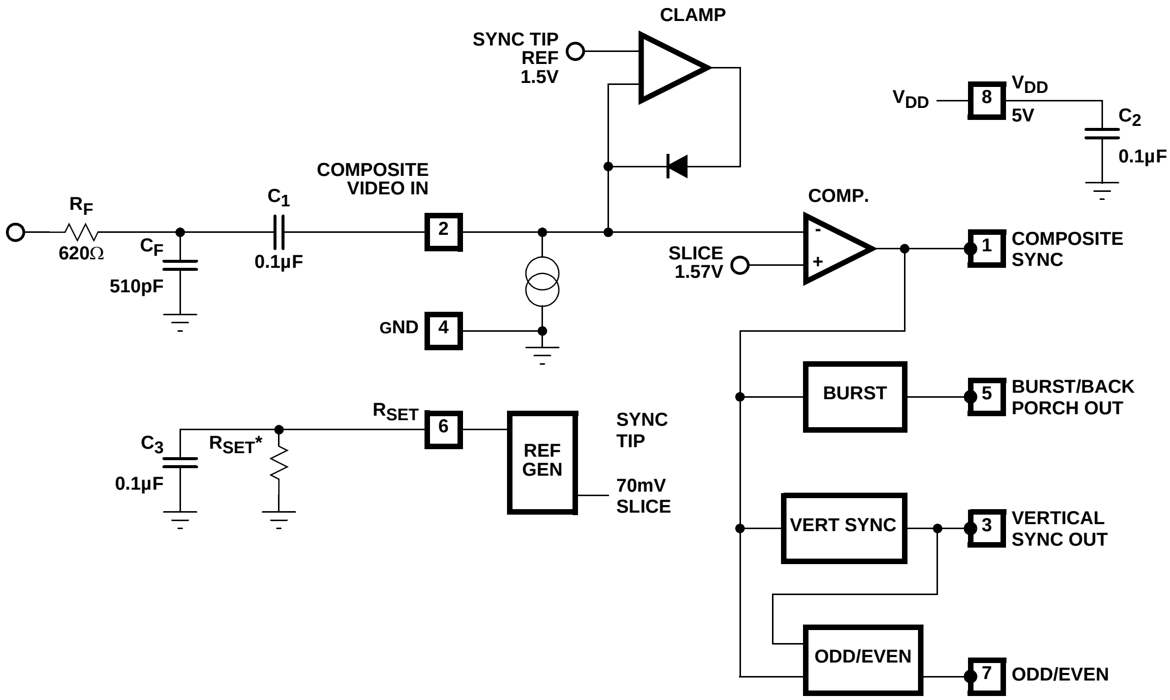


FIGURE 5.

Simplified Block Diagram



NOTE: * R_{SET} MUST BE AT 1% RESISTOR

FIGURE 6.