

## 74AC251 • 74ACT251

### 8-Input Multiplexer with 3-STATE Output

#### General Description

The AC/ACT251 is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It can be used as universal function generator to generate any logic function of four variables. Both true and complementary outputs are provided.

#### Features

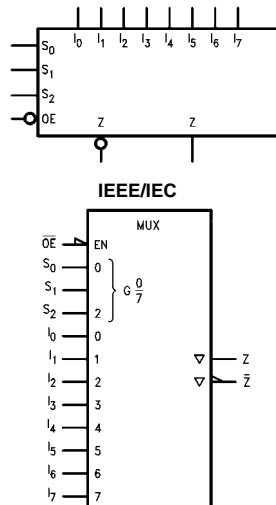
- $I_{CC}$  reduced by 50%
- Multifunctional capability
- On-chip select logic decoding
- Inverting and noninverting 3-STATE outputs
- Outputs source/sink 24 mA
- ACT251 has TTL-compatible inputs

#### Ordering Code:

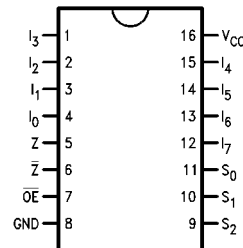
Order Number	Package Number	Package Description
74AC251SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
74AC251SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC251MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC251PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT251SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
74ACT251MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT251PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

#### Logic Symbols



#### Connection Diagram



#### Pin Descriptions

Pin Names	Description
$S_0-S_2$	Select Inputs
$\overline{OE}$	3-STATE Output Enable Input
$I_0-I_7$	Multiplexer Inputs
Z	3-STATE Multiplexer Output
$\bar{Z}$	Complementary 3-STATE Multiplexer Output

FACT™ is a trademark of Fairchild Semiconductor Corporation.

## Functional Description

This device is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs,  $S_0$ ,  $S_1$ ,  $S_2$ . Both true and complementary outputs are provided. The Output Enable input ( $\overline{OE}$ ) is active LOW. When it is activated, the logic function provided at the output is:

$$Z = \overline{OE} \cdot (I_0 \cdot \overline{S_0} \cdot \overline{S_1} \cdot \overline{S_2} + I_1 \cdot S_0 \cdot \overline{S_1} \cdot \overline{S_2} + I_2 \cdot \overline{S_0} \cdot S_1 \cdot \overline{S_2} + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S_2} + I_4 \cdot \overline{S_0} \cdot \overline{S_1} \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S_1} \cdot S_2 + I_6 \cdot \overline{S_0} \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$$

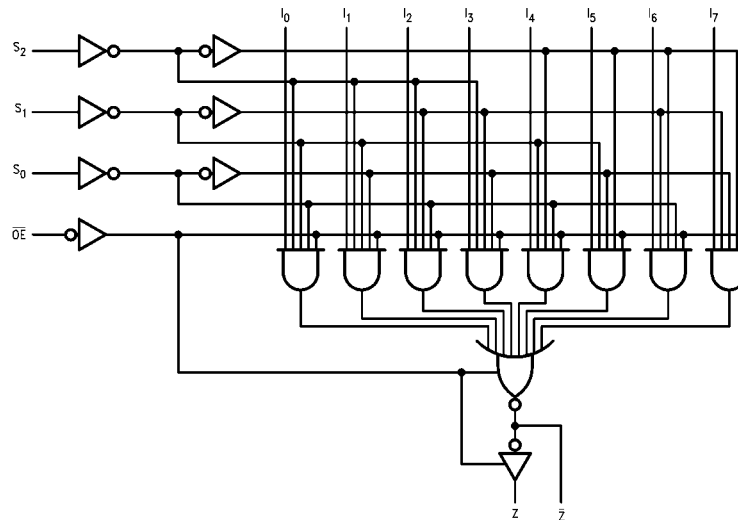
When the Output Enable is HIGH, both outputs are in the high impedance (High Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the 3-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active-LOW portion of the enable voltages.

## Truth Table

$\overline{OE}$	Inputs			Outputs	
	$S_2$	$S_1$	$S_0$	$\overline{Z}$	Z
H	X	X	X	Z	Z
L	L	L	L	$\overline{I_0}$	$I_0$
L	L	L	H	$\overline{I_1}$	$I_1$
L	L	H	L	$\overline{I_2}$	$I_2$
L	L	H	H	$\overline{I_3}$	$I_3$
L	H	L	L	$\overline{I_4}$	$I_4$
L	H	L	H	$\overline{I_5}$	$I_5$
L	H	H	L	$\overline{I_6}$	$I_6$
L	H	H	H	$\overline{I_7}$	$I_7$

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings**(Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 50$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Junction Temperature ( $T_J$ )	
PDIP	140°C

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	
AC	2.0V to 6.0V
ACT	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
AC Devices	
$V_{IN}$ from 30% to 70% of $V_{CC}$	
$V_{CC}$ @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
ACT Devices	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

**DC Electrical Characteristics for AC**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Typ	Guaranteed Limits				
$V_{IH}$	Minimum HIGH Level Input Voltage	3.0	1.5	2.1	2.1		V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
$V_{IL}$	Maximum LOW Level Input Voltage	3.0	1.5	0.9	0.9		V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
$V_{OH}$	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9		V	$I_{OUT} = -50 \mu A$
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46		V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -12$ mA $I_{OH} = -24$ mA $I_{OH} = -24$ mA (Note 2)
		4.5		3.86	3.76			
		5.5		4.86	4.76			
$V_{OL}$	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1		V	$I_{OUT} = 50 \mu A$
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44		V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 12$ mA $I_{OL} = 24$ mA $I_{OL} = 24$ mA (Note 2)
		4.5		0.36	0.44			
		5.5		0.36	0.44			
$I_{IN}$ (Note 4)	Maximum Input Leakage Current	5.5		$\pm 0.1$	$\pm 1.0$		$\mu A$	$V_I = V_{CC}, GND$
$I_{OZ}$	Maximum 3-STATE Current	5.5		$\pm 0.25$	$\pm 2.5$		$\mu A$	$V_I$ (OE) = $V_{IL}, V_{IH}$ $V_I = V_{CC}, V_{GND}$ $V_O = V_{CC}, GND$
$I_{OLD}$	Minimum Dynamic	5.5			75		mA	$V_{OLD} = 1.65V$ Max
$I_{OHD}$	Output Current (Note 3)	5.5			-75		mA	$V_{OHD} = 3.85V$ Min
$I_{CC}$ (Note 4)	Maximum Quiescent Supply Current	5.5		4.0	40.0		$\mu A$	$V_{IN} = V_{CC}$ or GND

**Note 2:** All outputs loaded; thresholds on input associated with output under test.

**Note 3:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 4:**  $I_{IN}$  and  $I_{CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{CC}$ .

## DC Electrical Characteristics for ACT

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits				
V <sub>IH</sub>	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	
		5.5	1.5	2.0	2.0			
V <sub>IL</sub>	Maximum LOW Level Input Voltage	4.5	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	
		5.5	1.5	0.8	0.8			
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4	V	I <sub>OUT</sub> = -50 μA	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = -24 mA I <sub>OH</sub> = -24 mA (Note 5)	
		5.5		4.86	4.76			
V <sub>OL</sub>	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1	V	I <sub>OUT</sub> = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 24 mA I <sub>OL</sub> = 24 mA (Note 5)	
		5.5		0.36	0.44			
I <sub>IN</sub>	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND	
I <sub>OZ</sub>	Maximum 3-STATE Current	5.5		±0.5	±5.0	μA	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> V <sub>O</sub> = V <sub>CC</sub> , GND	
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input	5.5	0.6		1.5	mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1V	
I <sub>OLD</sub>	Minimum Dynamic	5.5			75	mA	V <sub>OLD</sub> = 1.65V Max	
I <sub>OHD</sub>	Output Current (Note 6)	5.5			-75	mA	V <sub>OHD</sub> = 3.85V Min	
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5		4.0	40.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	

**Note 5:** All outputs loaded; thresholds on input associated with output under test.

**Note 6:** Maximum test duration 2.0 ms, one output loaded at a time.

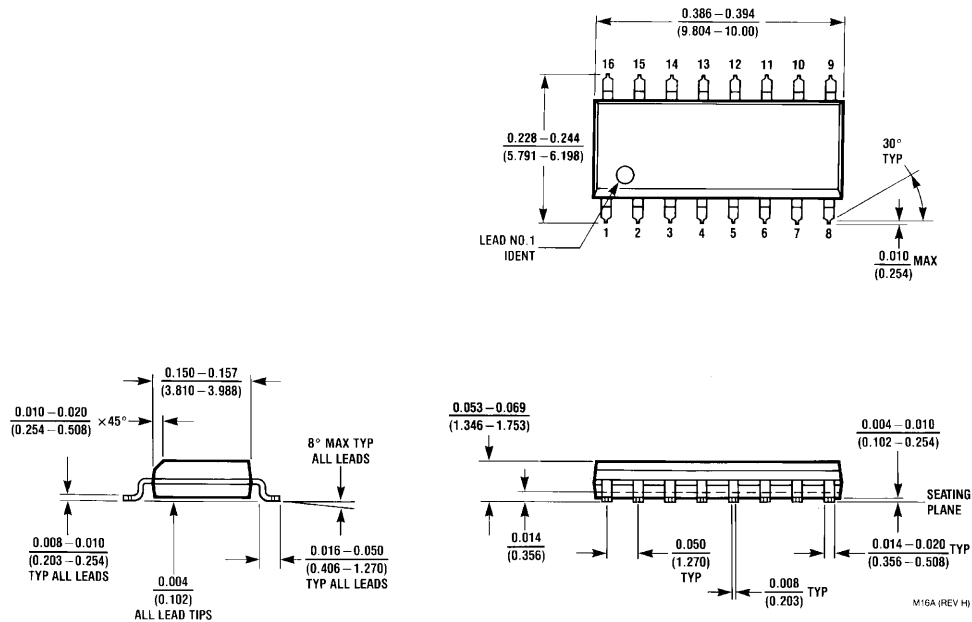
## AC Electrical Characteristics for AC

Symbol	Parameter	V <sub>CC</sub> (V) (Note 7)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay S <sub>n</sub> to Z or $\bar{Z}$	3.3	1.5	11.5	17.5	1.5	19.0	ns
		5.0	1.5	8.5	12.5	1.5	13.5	
t <sub>PHL</sub>	Propagation Delay S <sub>n</sub> to Z or $\bar{Z}$	3.3	1.5	11.0	17.5	1.5	19.0	ns
		5.0	1.5	8.0	12.5	1.5	13.5	
t <sub>PLH</sub>	Propagation Delay I <sub>n</sub> to Z or $\bar{Z}$	3.3	1.5	10.0	14.0	1.5	15.5	ns
		5.0	1.5	7.0	10.0	1.5	11.0	
t <sub>PHL</sub>	Propagation Delay I <sub>n</sub> to Z or $\bar{Z}$	3.3	1.5	9.0	14.0	1.5	15.5	ns
		5.0	1.5	6.5	10.0	1.5	11.0	
t <sub>PZH</sub>	Output Enable Time $\overline{OE}$ to Z or $\bar{Z}$	3.3	1.5	7.5	11.0	1.5	12.0	ns
		5.0	1.5	5.5	8.0	1.5	9.0	
t <sub>PZL</sub>	Output Enable Time $\overline{OE}$ to Z or $\bar{Z}$	3.3	1.5	7.5	11.0	1.5	12.0	ns
		5.0	1.5	5.5	8.0	1.5	9.0	
t <sub>PHZ</sub>	Output Disable Time $\overline{OE}$ to Z or $\bar{Z}$	3.3	1.5	8.5	11.5	1.5	13.0	ns
		5.0	1.5	7.0	9.5	1.5	10.0	
t <sub>PLZ</sub>	Output Disable Time $\overline{OE}$ to Z or $\bar{Z}$	3.3	1.5	7.0	11.0	1.5	12.0	ns
		5.0	1.5	5.5	8.0	1.5	8.5	

**Note 7:** Voltage Range 3.3 is 3.3V ± 0.3V.  
Voltage Range 5.0 is 5.0V ± 0.5V

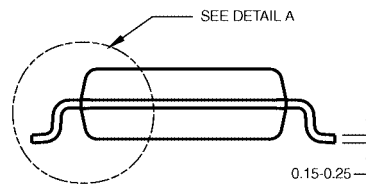
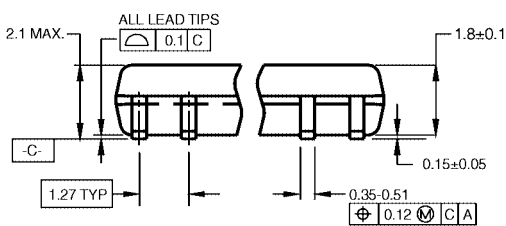
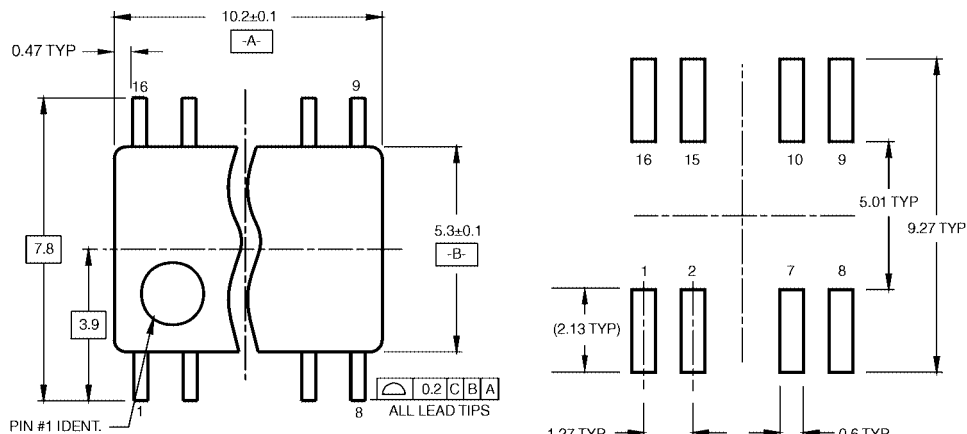
AC Electrical Characteristics for ACT								
Symbol	Parameter	V <sub>CC</sub> (V) (Note 8)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay S <sub>n</sub> to Z or $\bar{Z}$	5.0	2.5	7.0	15.5	2.0	17.0	ns
t <sub>PHL</sub>	Propagation Delay S <sub>n</sub> to Z or $\bar{Z}$	5.0	2.5	7.5	16.5	2.5	18.5	ns
t <sub>PLH</sub>	Propagation Delay I <sub>n</sub> to Z or $\bar{Z}$	5.0	2.5	5.5	12.0	2.0	13.0	ns
t <sub>PHL</sub>	Propagation Delay I <sub>n</sub> to Z or $\bar{Z}$	5.0	2.5	6.5	12.5	2.5	14.0	ns
t <sub>PZH</sub>	Output Enable Time $\overline{OE}$ to Z or $\bar{Z}$	5.0	1.5	5.0	8.5	1.5	9.0	ns
t <sub>PZL</sub>	Output Enable Time OE to Z or $\bar{Z}$	5.0	1.5	4.5	8.5	1.5	9.5	ns
t <sub>PHZ</sub>	Output Disable Time $\overline{OE}$ to Z or $\bar{Z}$	5.0	2.0	6.0	12.0	2.0	13.0	ns
t <sub>PLZ</sub>	Output Disable Time OE to Z or $\bar{Z}$	5.0	1.5	4.5	8.5	1.5	9.0	ns
<b>Note 8:</b> Voltage Range 5.0 is 5.0V ±0.5V								
Capacitance								
Symbol	Parameter	Typ	Units	Conditions				
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN				
C <sub>PD</sub>	Power Dissipation Capacitance	70.0	pF	V <sub>CC</sub> = 5.0V				

**Physical Dimensions** inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body  
Package Number M16A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

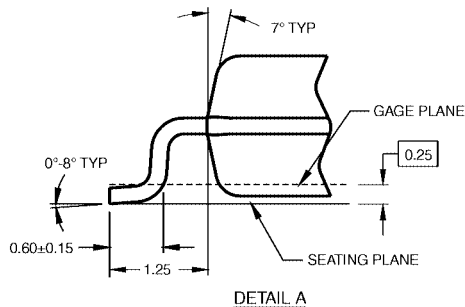


DIMENSIONS ARE IN MILLIMETERS

NOTES:

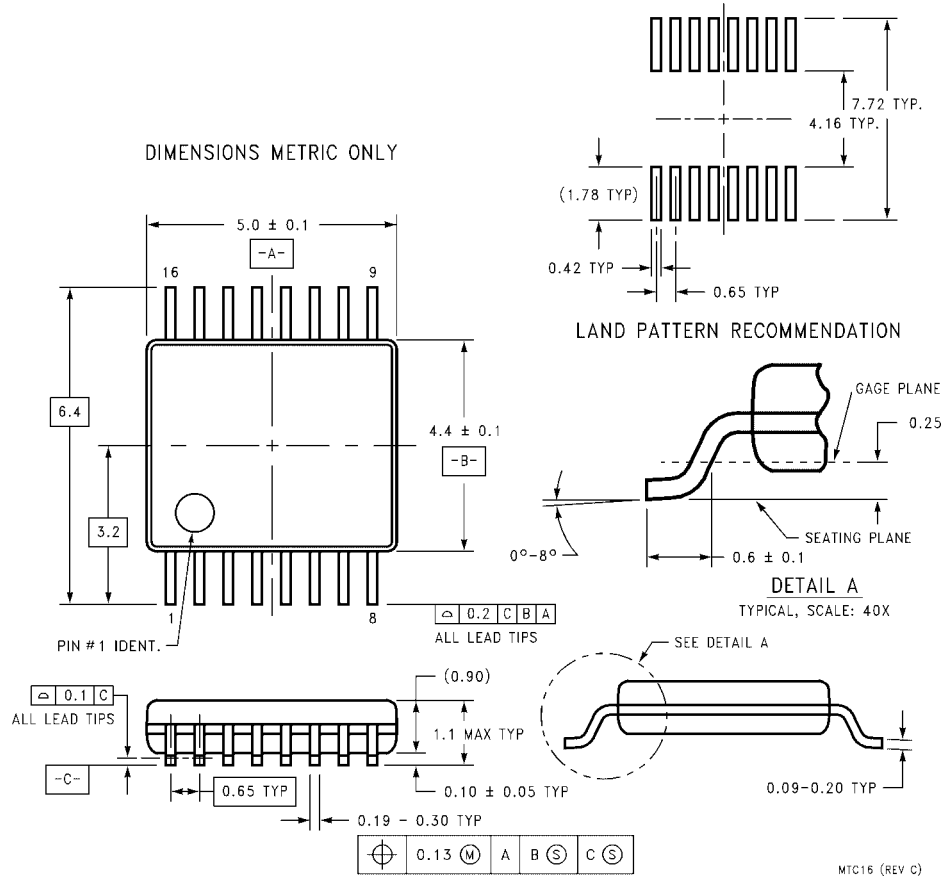
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1



**16-Lead Small Outline Package (SOP), EIAJ Type II, 5.3mm Wide  
Package Number M16D**

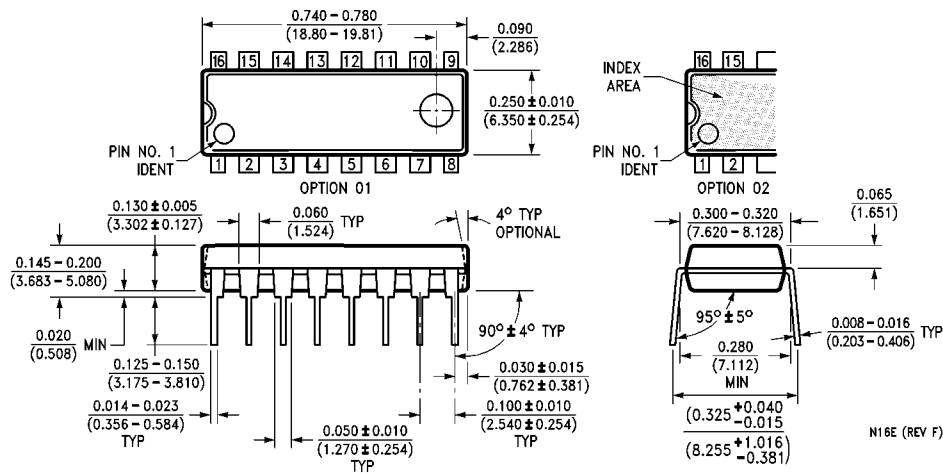
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC16**



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)