FAIRCHILD SEMICONDUCTOR®

March 2007

74ACQ245, 74ACTQ245
Quiet Series™ Octal Bidirectional Transceiver with 3-STATE Inputs/Outputs

Features

- I_{CC} and I_{OZ} reduced by 50%
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- 3-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24mA
- Faster prop delays than the standard ACT245

General Description

The ACQ/ACTQ245 contains eight non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 24mA at both the A and B ports. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A Ports to B Ports; Receive (active-LOW) enables data from B Ports to A Ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition.

The ACQ/ACTQ utilizes Fairchild Quiet Series™ technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Ordering Information

Order Number	Package Number	Package Description
74ACQ245SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ACQ245SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACTQ245SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ACTQ245SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACTQ245QSC	MQA20	20-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide
74ACTQ245MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74ACTQ245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACTQ245MTCX_NL(1)	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.
Pb-Free package per JEDEC J-STD-020B.

Note:
1. Device available in Tape and Reel only.

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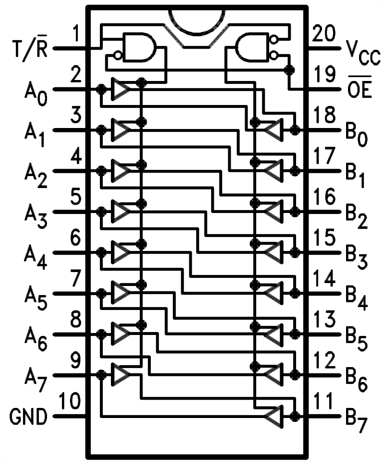
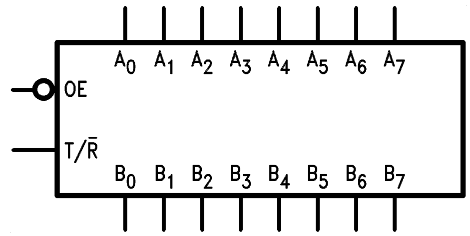
Connection Diagram



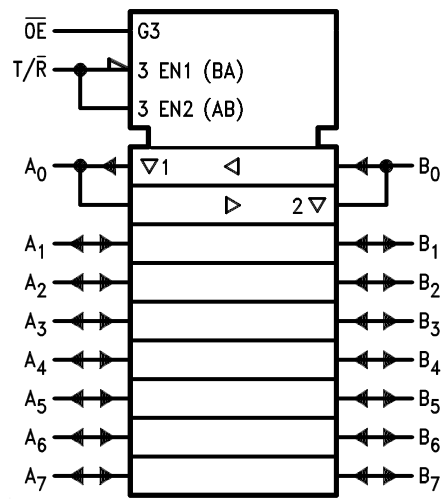
Pin Description

Pin Names	Description
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A 3-STATE Inputs or 3-STATE Outputs
B_0–B_7	Side B 3-STATE Inputs or 3-STATE Outputs

Logic Symbol



IEEE/IEC



Truth Table

Inputs		Outputs
OE	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
I_{IK}	DC Input Diode Current $V_I = –0.5V$ $V_I = V_{CC} + 0.5V$	 –20mA +20mA
V_I	DC Input Voltage	–0.5V to V_{CC} + 0.5V
I_{OK}	DC Output Diode Current $V_O = –0.5V$ $V_O = V_{CC} + 0.5V$	 –20mA +20mA
V_O	DC Output Voltage	–0.5V to V_{CC} + 0.5V
I_O	DC Output Source or Sink Current	±50mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Output Pin	±50mA
T_{STG}	Storage Temperature	–65°C to +150°C
	DC Latch-Up Source or Sink Current	±300mA
T_J	Junction Temperature	140°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage ACQ ACTQ	 2.0V to 6.0V 4.5V to 5.5V
V_I	Input Voltage	0V to V_{CC}
V_O	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	–40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACQ Devices: V_{IN} from 30% to 70% of V_{CC}, V_{CC} @ 3.0V, 4.5V, 5.5V	125mV/ns
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACTQ Devices: V_{IN} from 0.8V to 2.0V, V_{CC} @ 4.5V, 5.5V	125mV/ns

DC Electrical Characteristics for ACQ

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = +25°C$		$T_A = –40°C$ to $+85°C$	Units
				Typ.	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage	3.0	$V_{OUT} = 0.1V$ or $V_{CC} – 0.1V$	1.5	2.1	2.1	V
		4.5		2.25	3.15	3.15	
		5.5		2.75	3.85	3.85	
V_{IL}	Maximum LOW Level Input Voltage	3.0	$V_{OUT} = 0.1V$ or $V_{CC} – 0.1V$	1.5	0.9	0.9	V
		4.5		2.25	1.35	1.35	
		5.5		2.75	1.65	1.65	
V_{OH}	Minimum HIGH Level Output Voltage	3.0	$I_{OUT} = –50μA$	2.99	2.9	2.9	V
		4.5		4.49	4.4	4.4	
		5.5		5.49	5.4	5.4	
			$V_{IN} = V_{IL}$ or V_{IH}:				
		3.0	$I_{OH} = –12mA$		2.56	2.46	
		4.5	$I_{OH} = –24mA$		3.86	3.76	
		5.5	$I_{OH} = –24mA$(2)		4.86	4.76	
V_{OL}	Maximum LOW Level Output Voltage	3.0	$I_{OUT} = 50μA$	0.002	0.1	0.1	V
		4.5		0.001	0.1	0.1	
		5.5		0.001	0.1	0.1	
			$V_{IN} = V_{IL}$ or V_{IH}:				
		3.0	$I_{OL} = 12mA$		0.36	0.44	
		4.5	$I_{OL} = 24mA$		0.36	0.44	
		5.5	$I_{OL} = 24mA$(2)		0.36	0.44	
I_{IN}(4)	Maximum Input Leakage Current	5.5	$V_I = V_{CC}$, GND		±0.1	±1.0	μA
I_{OLD}	Minimum Dynamic Output Current(3)	5.5	$V_{OLD} = 1.65V$ Max.			75	mA
I_{OHD}		5.5	$V_{OHD} = 3.85V$ Min.			–75	mA
I_{CC}(4)	Maximum Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND		4.0	40.0	μA
I_{OZT}	Maximum I/O Leakage Current	5.5	V_I (OE) $= V_{IL}, V_{IH}$; $V_I = V_{CC}$, GND; $V_O = V_{CC}$, GND		±0.3	±3.0	μA
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	Figures 1 & 2(5)	1.1	1.5		V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	Figures 1 & 2(5)	–0.6	–1.2		V
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	5.0	(6)	3.1	3.5		V
V_{ILD}	Maximum LOW Level Dynamic Input Voltage	5.0	(6)	1.9	1.5		V

Notes:

2. All outputs loaded; thresholds on input associated with output under test.
3. Maximum test duration 2.0ms, one output loaded at a time.
4. I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
5. Max number of outputs defined as (n). Data Inputs are driven 0V to 5V; one output @ GND.
6. Max number of Data Inputs (n) switching. (n–1) Inputs switching 0V to 5V (ACQ). Input-under-test switching: 5V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

DC Electrical Characteristics for ACTQ

				$T_A = +25°C$		$T_A = –40°C$ to $+85°C$	
Symbol	**Parameter**	**V_{CC} (V)**	**Conditions**	**Typ.**	**Guaranteed Limits**		**Units**
V_{IH}	Minimum HIGH Level Input Voltage	4.5	$V_{OUT} = 0.1V$ or $V_{CC} – 0.1V$	1.5	2.0	2.0	V
		5.5		1.5	2.0	2.0	
V_{IL}	Maximum LOW Level Input Voltage	4.5	$V_{OUT} = 0.1V$ or $V_{CC} – 0.1V$	1.5	0.8	0.8	V
		5.5		1.5	0.8	0.8	
V_{OH}	Minimum HIGH Level Output Voltage	4.5	$I_{OUT} = –50μA$	4.49	4.4	4.4	V
		5.5		5.49	5.4	5.4	
		4.5	$V_{IN} = V_{IL}$ or V_{IH}: $I_{OH} = –24mA$		3.86	3.76	
		5.5	$I_{OH} = –24mA$(7)		4.86	4.76	
V_{OL}	Maximum LOW Level Output Voltage	4.5	$I_{OUT} = 50μA$	0.001	0.1	0.1	V
		5.5		0.001	0.1	0.1	
		4.5	$V_{IN} = V_{IL}$ or V_{IH}: $I_{OL} = 24mA$		0.36	0.44	
		5.5	$I_{OL} = 24mA$(7)		0.36	0.44	
I_{IN}	Maximum Input Leakage Current	5.5	$V_I = V_{CC}$, GND		±0.1	±1.0	µA
I_{OZT}	Maximum 3-STATE Leakage Current	5.5	$V_I = V_{IL}$, V_{IH}, $V_O = V_{CC}$, GND		±0.3	±3.0	µA
I_{CCT}	Maximum I_{CC}/Input	5.5	$V_I = V_{CC} – 2.1V$	0.6		1.5	mA
I_{OLD}	Minimum Dynamic	5.5	$V_{OLD} = 1.65V$ Max.			75	mA
I_{OHD}	Output Current(8)	5.5	$V_{OHD} = 3.85V$ Min.			–75	mA
I_{CC}	Maximum Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND		4.0	40.0	µA
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	Figures 1 & 2(9)	1.1	1.5		V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	Figures 1 & 2(9)	–0.6	–1.2		V
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	5.0	(10)	1.9	2.2		V
V_{ILD}	Maximum LOW Level Dynamic Input Voltage	5.0	(10)	1.2	0.8		V

Notes:

7. All outputs loaded; thresholds on input associated with output under test.
8. Maximum test duration 2.0ms, one output loaded at a time.
9. Max number of outputs defined as (n). n–1 Data Inputs are driven 0V to 3V; one output @ GND.
10. Max number of Data Inputs (n) switching. (n–1) Inputs switching 0V to 3V (ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}) f = 1 MHz.

AC Electrical Characteristics for ACQ

Symbol	Parameter	V_{CC} (V)(11)	T_A = +25°C, C_L = 5 pF			T_A = –40°C to +85°C, C_L = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
t_{PHL}, t_{PLH}	Propagation Delay, Data to Output	3.3	2.0	7.5	10.0	2.0	10.5	ns
		5.0	1.5	5.0	6.5	1.5	7.0	
t_{PZL}, t_{PZH}	Output Enable Time	3.3	3.0	8.5	13.0	3.0	13.5	ns
		5.0	2.0	6.0	8.5	2.0	9.0	
t_{PHZ}, t_{PLZ}	Output Disable Time	3.3	1.0	8.5	14.5	1.0	15.0	ns
		5.0	1.0	7.5	9.5	1.0	10.0	
t_{OSHL}, t_{OSLH}	Output to Output Skew, Data to Output(12)	3.3		1.0	1.5		1.5	ns
		5.0		0.5	1.0		1.0	

Notes:

11. Voltage range 5.0 is 5.0V ± 0.5V. Voltage range 3.3 is 3.3V ± 0.3V.
12. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Electrical Characteristics for ACTQ

Symbol	Parameter	V_{CC} (V)(13)	T_A = +25°C, C_L = 50pF			T_A = –40°C to +85°C, C_L = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
t_{PHL}, t_{PLH}	Propagation Delay, Data to Output	5.0	1.5	5.5	7.0	1.5	7.5	ns
t_{PZL}, t_{PZH}	Output Enable Time	5.0	2.0	7.0	9.0	2.0	9.5	ns
t_{PHZ}, t_{PLZ}	Output Disable Time	5.0	1.0	8.0	10.0	1.0	10.5	ns
t_{OSHL}, t_{OSLH}	Output to Output Skew, Data to Output(14)	5.0		0.5	1.0		1.0	ns

Notes:

13. Voltage range 5.0 is 5.0V ± 0.5V
14. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{CC} = OPEN	4.5	pF
$C_{I/O}$	Input/Output Capacitance	V_{CC} = 5.0V	15	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 5.0V	80.0	pF

FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

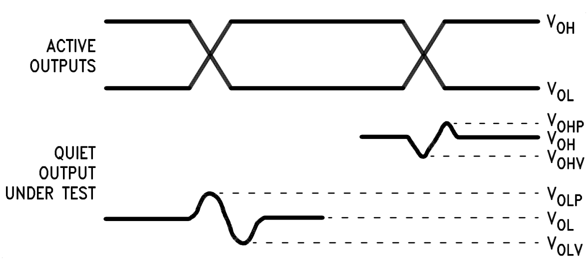
Hewlett Packard Model 8180A Word Generator

PC-163A Test Fixture

Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50pF, 500Ω.
2. Deskew the HFS generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. It is important to deskew the HFS generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set the HFS generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and effect the results of the measurement.
5. Set the HFS generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with an oscilloscope.



Notes:

15. V_{OHV} and V_{OLP} are measured with respect to ground reference.

16. Input pulses have the following characteristics: $f = 1MHz$, $t_r = 3ns$, $t_f = 3ns$, skew < 150ps.

Figure 1. Quiet Output Noise Voltage Waveforms

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV}:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V_{OLP} and V_{OLV} on the quiet output during the worst case transition for active and enable. Measure V_{OHP} and V_{OHV} on the quiet output during the worst case active and enable transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD}:

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL}, until the output begins to oscillate or steps out a min of 2ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD}.
- Next decrease the input HIGH voltage level, V_{IH}, until the output begins to oscillate or steps out a min of 2ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD}.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

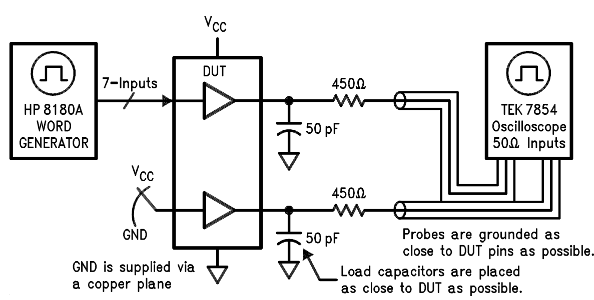


Figure 2. Simultaneous Switching Test Circuit

Physical Dimensions

Dimensions are in inches (millimeters) unless otherwise noted.

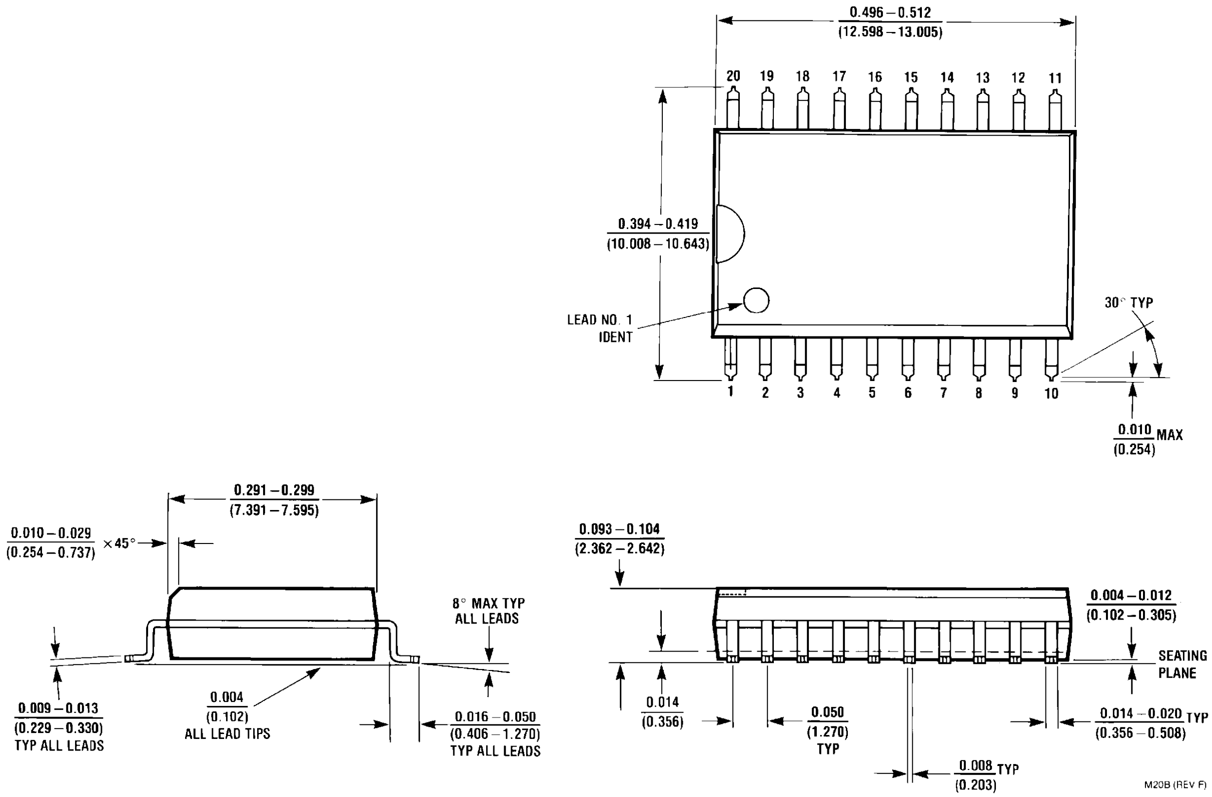


Figure 3. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Package Number M20B

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.

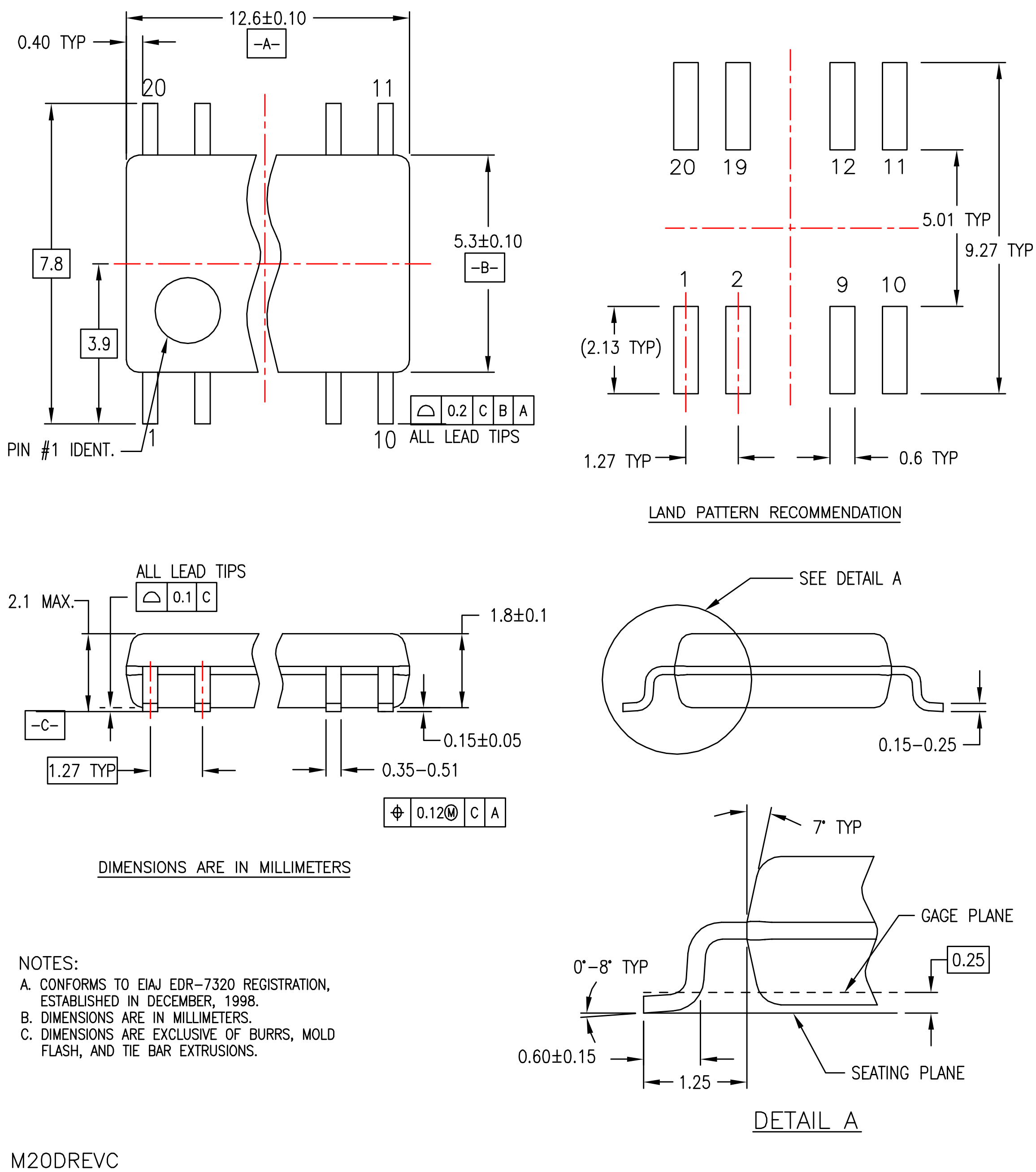


Figure 4. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M20D

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.

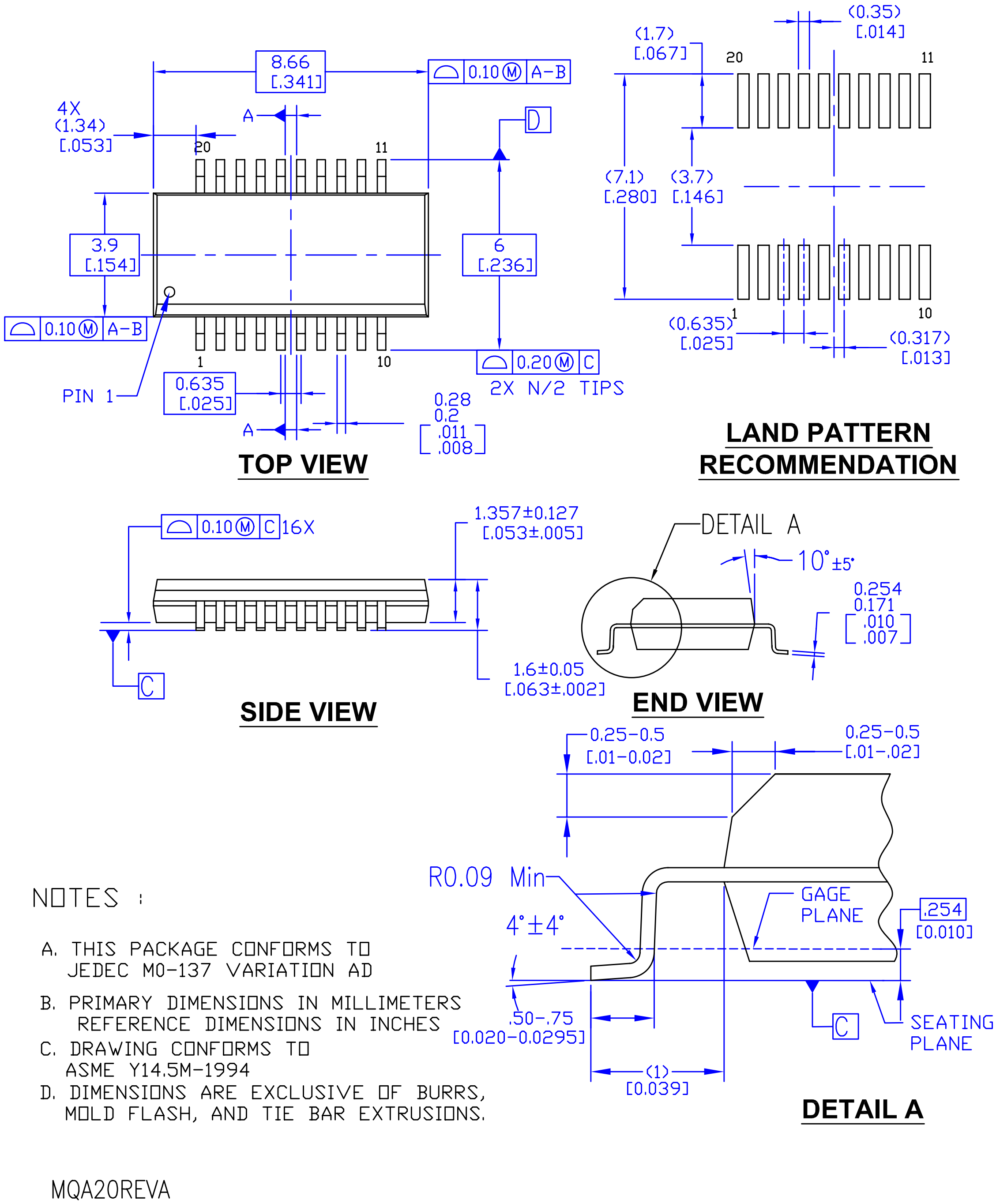


Figure 5. 20-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide Package Number MQA20

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.

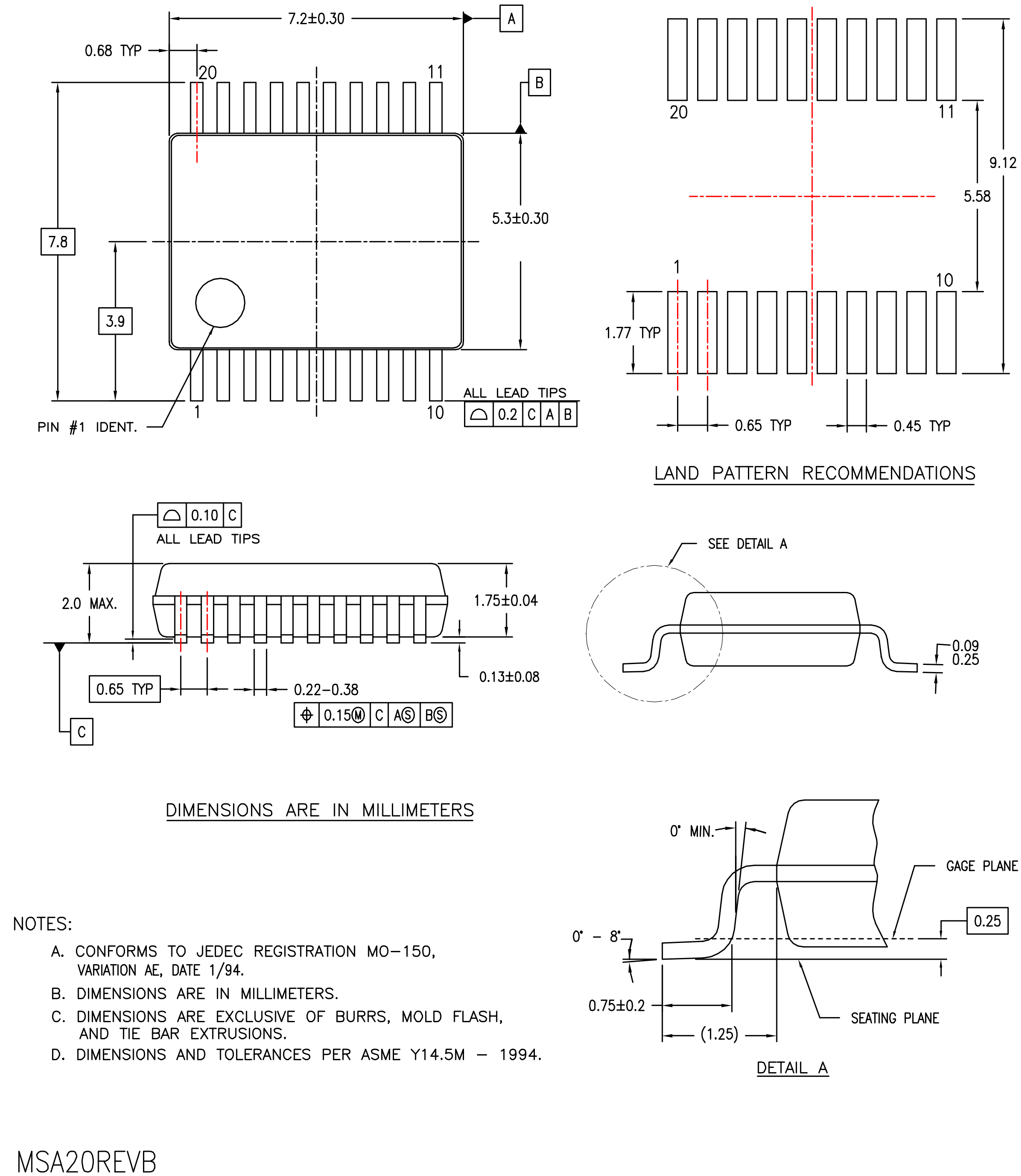
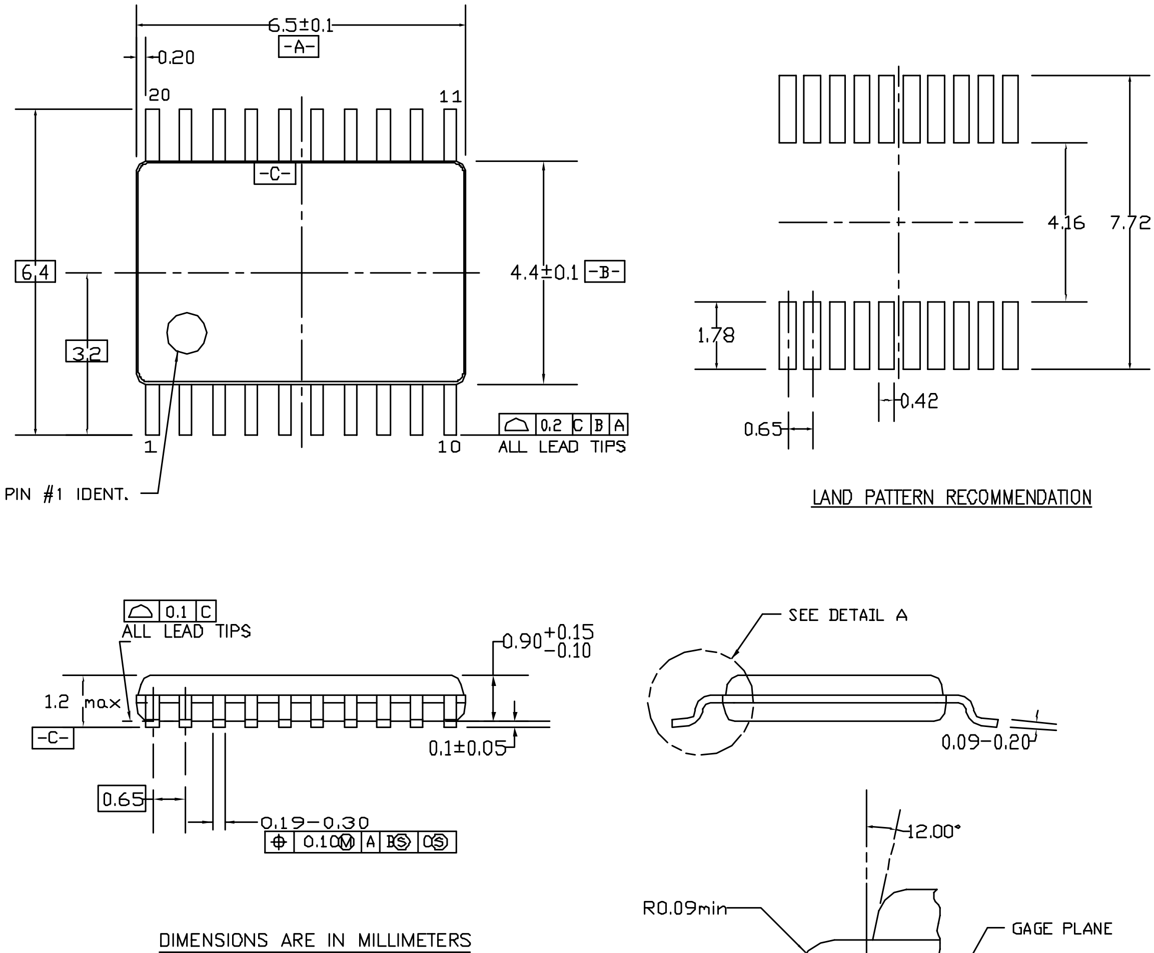
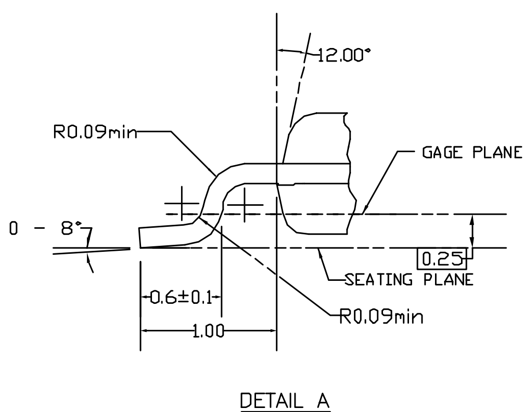


Figure 6. 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide Package Number MSA20

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.





NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

Figure 7. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC20

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SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SyncFET™
TCM™
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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

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Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

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