National Semiconductor

LM49200

Boomer® Audio Power Amplifier Series

May 21, 2009

Stereo Class AB Audio Subsystem with a True Ground Headphone Amplifier

General Description

The LM49200 is a fully integrated audio subsystem with a stereo power amplifier capable of delivering 500mW of continuous average power per channel into 8Ω with 1% THD+N using a 3.3V supply. The LM49200 includes a separate stereo headphone amplifier that can deliver 35mW per channel into 32Ω.

The LM49200 has three input channels. A pair of single-ended inputs and a fully differential input channel. The LM49200 features a 32-step digital volume control on the input stage and an 8-step digital volume control on the headphone output stage.

The digital volume control and output modes are programmed through a two-wire I2C compatible interface that allows flexibility in routing and mixing audio channels.

The LM49200 is designed for cellular phone, PDA, and other portable handheld applications. The high level of integration minimizes external components. The True Ground headphone amplifier eliminates the physically large DC blocking output capacitors reducing required board space and reducing cost.

Key Specifications

- Supply Voltage (V_{DD}) — $2.7V \leq V_{DD} \leq 5.5V$
- I2C Supply Voltage — $1.7V \leq I2CV_{DD} \leq 5.5V$
- Output power at V_{DD} = 5V, 1% THD+N
  - R_L = 8Ω speaker — 1.25W (typ)
  - R_L = 32Ω headphone — 38mW (typ)
- Output power at V_{DD} = 3.3V, 1% THD+N
  - R_L = 8Ω speaker — 520W (typ)
  - R_L = 32Ω headphone — 38mW (typ)
- PSRR:
  - V_{DD} = 3.3V, 217Hz ripple, Mono In — 95dB (typ)
- Shutdown power supply current — 0.02µA (typ)

Features

- Differential mono input and stereo single-ended input
- 32-step digital volume control (-80 to +18dB)
- Three independent volume channels (Left, Right, Mono)
- Separate headphone volume control
- Flexible output for speaker and headphone output
- True Ground headphone amplifier eliminates large DC blocking capacitors reducing PCB space and cost
- Receiver pass-through capability
- Soft enable function
- RF immunity topology
- "Click and Pop" suppression circuitry
- Thermal shutdown protection
- Micro-power shutdown
- I2C control interface
- Available in space-saving microSMD package

Applications

- Portable electronic devices
- Mobile Phones
- PDAs

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Typical Application

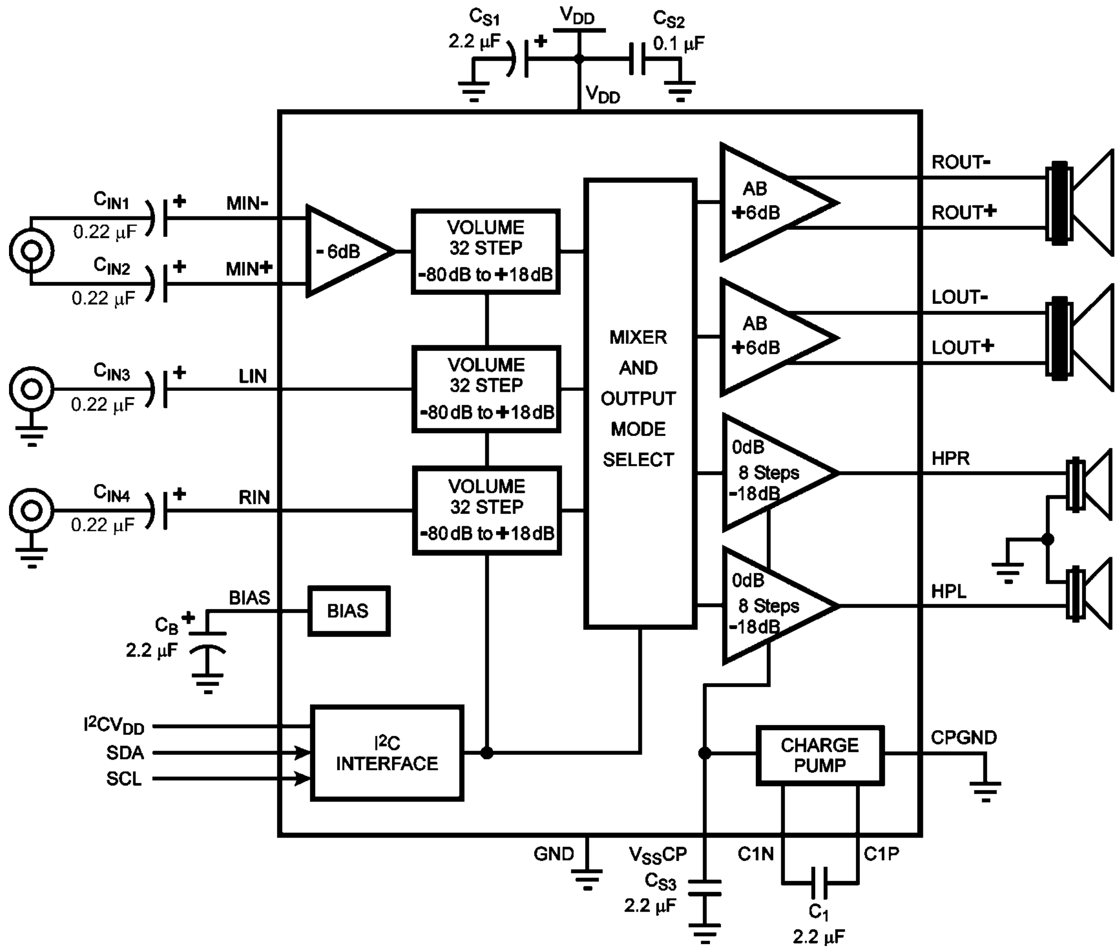
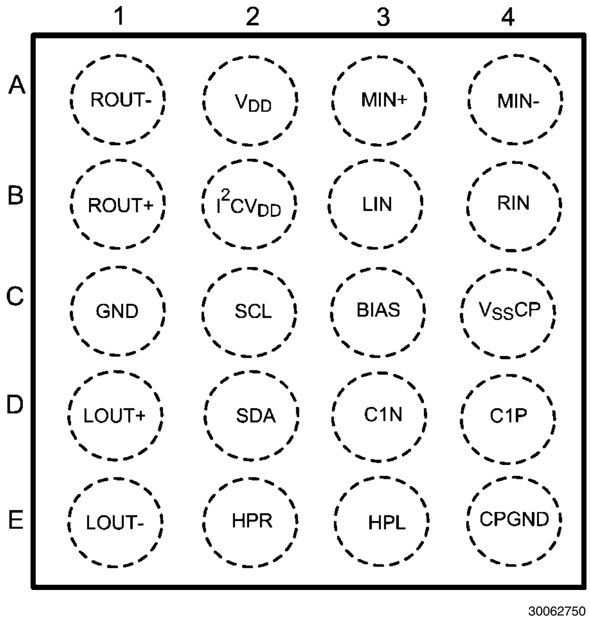


FIGURE 1. Typical Audio Application Circuit

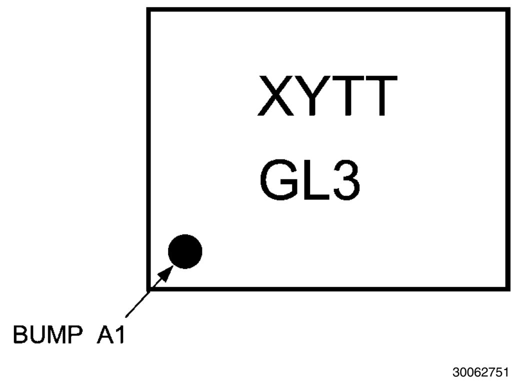
Connection Diagrams

20 Bump micro SMD Package



Top View
(Bump Side Down)
Order Number LM49200TL, LM49200TLX
See NS Package Number TLA20BBA

micro SMD Markings



Top View
XY - Date Code
TT - Die Traceability
G- Boomer Family
L3 - LM49200TL

Ordering Information

Order Number	Package	Package DWG #	Transport Media	MSL Level	Green Status
LM49200TL	20 Bump micro SMD	TLA20BBA	250 units on tape and reel	1	RoHS and no sB/Br
LM49200TLX	20 Bump micro SMD	TLA20BBA	3000 units on tape and reel	1	RoHS and no sB/Br

Bump Descriptions

Bump	Name	Pin Function	Type
A1	ROUT-	Right Loudspeaker Negative Output	Analog Output
A2	VDD	Power Supply	Power Input
A3	MIN+	Differential Mono Positive Input	Analog Input
A4	MIN-	Differential Mono Negative Input	Analog Input
B1	ROUT+	Right Loudspeaker Positive Output	Analog Output
B2	I^2CV_{DD}	I^2C power supply	Power Input
B3	LIN	Single-ended Left Input	Analog Input
B4	RIN	Single-ended Right Input	Analog Input
C1	GND	Power Ground	Ground
C2	SCL	I^2C Clock	Digital Input
C3	BIAS	Half-Supply Bias point, capacitor bypassed	Analog Output
C4	VSSCP	Negative Charge Pump Power Supply	Analog Output
D1	LOUT+	Left Loudspeaker Negative Output	Analog Output
D2	SDA	I^2C Data	Digital Input
D3	CIN	Negative Terminal Charge Pump Flying Capacitor	Analog Output
D4	CIP	Positive Terminal Charge Pump Flying Capacitor	Analog Output
E1	LOUT-	Left Loudspeaker Positive Output	Analog Output
E2	HPR	Right Headphone Output	Analog Output
E3	HPL	Left Headphone Output	Analog Output
E4	CPGND	Charge Pump Ground	Ground

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 1)	6.0V
Storage Temperature	−65°C to +150°C
Voltage at Any Input Pin	GND – 0.3 to V_{DD} + 0.3V
Power Dissipation (Note 3)	Internally Limited
ESD Rating (Note 4)	2000V
ESD Rating (Note 5)	200V
Junction Temperature (T_{JMAX})	150°C
Soldering Information	
Vapor Phase (60sec.)	215°C
Infrared (15sec.)	220°C
See AN-1112 "Micro SMD Wafer Level Chip Scale Package"	
Thermal Resistance	
$θ_{JA}$	45.1°C/W

Operating Ratings

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le 85°C$
Supply Voltage (V_{DD})	$2.7V \le V_{DD} \le 5.5V$
Supply Voltage (I^2CV_{DD})	$1.7V \le I^2CV_{DD} \le 5.5V$
	$I^2CV_{DD} \le V_{DD}$

Electrical Characteristics V_{DD} = 3.3V (Notes 1, 2)

The following specifications apply for V_{DD} = 3.3V, T_A = 25°C, all volume controls set to 0dB, unless otherwise specified.

LS = Loudspeaker, HP = Headphone.

Symbol	Parameter	Conditions	LM49200		Units (Limits)
			Typical (Note 6)	Limits (Note 7)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0, No Loads			
		EP Receiver (Output Mode Bit D4 = 1)	1.2	1.7	mA (max)
		Stereo LS only (Mode 2)	4	5.5	mA (max)
		Stereo HP only (Mode 8)	4.5	6.4	mA (max)
		Stereo LS + Stereo HP (Mode 10)	7.0	9.8	mA (max)
I_{SD}	Shutdown Current		0.02	1	µA (max)
V_{OS}	Output Offset Voltage	V_{IN} = 0V, Mode 10 LS output, R_L = 8Ω BTL HP output, R_L = 32Ω SE	 2.5 1.4	 15 5	 mV (max) mV (max)
P_O	Output Power	LS output, Mode 2, R_L = 8Ω BTL THD+N = 1%, f = 1kHz	520	450	mW (min)
		HP output, Mode 8, R_L = 32Ω SE THD+N = 1%, f = 1kHz	38	35	mW (min)
THD+N	Total Harmonic Distortion + Noise	LS output, f = 1kHz, R_L = 8Ω BTL P_O = 250mW, Mode 2	0.05		%
		HP output, f = 1kHz, R_L = 32Ω SE P_O = 12mW, Mode 8	0.02		%
SNR	Signal-to-Noise Ratio	LS output, f = 1kHz, V_{REF} = V_{OUT} (1%THD+N) Gain = 0dB, A-weighted LIN & RIN AC terminated	105		dB
		HP output, f = 1kHz, V_{REF} = V_{OUT} (1%THD+N) Gain = 0dB, A-weighted LIN & RIN AC terminated	101		dB

Symbol	Parameter	Conditions	LM49200 Typical (Note 6)	LM49200 Limits (Note 7)	Units (Limits)
ε_{OUT}	Output Noise	A-weighted, Inputs terminated to AC GND, Output Referred			
		Right LS only, Mode 1	8		μV
		LS: Mode 1	8		μV
		LS: Mode 2	11		μV
		LS: Mode 3	14		μV
		HP: Mode 4	8		μV
		HP: Mode 8	9		μV
		HP: Mode 12	11		μV
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{PP}, f_{RIPPLE} = 217Hz, C_B = 2.2μF All inputs AC terminated to GND, output referred			
		LS: Mode 1, R_L = 8Ω BTL	95		dB
		LS: Mode 2, R_L = 8Ω BTL	75		dB
		HP: Mode 4, R_L = 32Ω SE	90		dB
		HP: Mode 8, R_L = 32Ω SE	80		dB
CMRR	Common-Mode Rejection Ratio	f = 217Hz, V_{CM} = 1V_{P-P} LS: R_L = 8Ω BTL, Mode 1 HP: R_L = 32Ω SE, Mode 4	60 66		dB dB
X_{TALK}	Crosstalk	LS: P_O = 400mW, f = 1kHz, Mode 2	80		dB
		HP: P_O = 12mW, f = 1kHz, Mode 8	70		dB
Z_{IN}	MIN, LIN, and RIN Input Impedance	Maximum Gain setting	12.5	10 15	kΩ (min) kΩ (max)
		Maximum Attenuation setting	110	90 130	kΩ (min) kΩ (max)
VOL	Digital Volume Control Range	Maximum Gain Maximum Attenuation	18 –80		dB dB
VOL	Volume Control Step Size Error		0.2		dB
T_{WU}	Wake-Up Time from Shutdown	C_B = 2.2μF, HP, Normal Turn-On Mode	29		ms
		C_B = 2.2μF, HP, Fast Turn-On Mode	16		ms

Electrical Characteristics V_{DD} = 5.0V (Notes 1, 2)

The following specifications apply for V_{DD} = 5.0V, T_A = 25°C, all volume controls set to 0dB, unless otherwise specified.

LS = Loudspeaker, HP = Headphone.

Symbol	Parameter	Conditions	LM49200 Typical (Note 6)	LM49200 Limits (Note 7)	Units (Limits)
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0, No Loads			
		EP Receiver (Output Mode Bit D4 = 1)	1.3	1.8	mA (max)
		Stereo LS only (Mode 2)	4.2	5.9	mA (max)
		Stereo HP only (Mode 8)	4.7	6.5	mA (max)
		Stereo LS + Stereo HP (Mode 10)	7.3	10.1	mA (max)
I_{SD}	Shutdown Current		0.02	1	μA (max)
V_{OS}	Output Offset Voltage	V_{IN} = 0V, Mode 10 LS output, R_L = 8Ω BTL HP output, R_L = 32Ω SE	2.5 1.4	15 5	mV (max) mV (max)

Symbol	Parameter	Conditions	LM49200 Typical (Note 6)	LM49200 Limits (Note 7)	Units (Limits)
P_O	Output Power	LS output, Mode 2, R_L = 8Ω BTL THD+N = 1%, f = 1kHz	1.25		W
		HP output, Mode 8, R_L = 32Ω SE THD+N = 1%, f = 1kHz	38		mW
THD+N	Total Harmonic Distortion + Noise	LS output, f = 1kHz, R_L = 8Ω BTL P_O = 400mW, Mode 2	0.05		%
		HP output, f = 1kHz, R_L = 32Ω SE P_O = 12mW, Mode 8	0.02		%
SNR	Signal-to-Noise Ratio	LS output, f = 1kHz, V_{REF} = V_{OUT} (1%THD+N) Gain = 0dB, A-weighted LIN & RIN AC terminated	109		dB
		HP output, f = 1kHz, V_{REF} = V_{OUT} (1%THD+N) Gain = 0dB, A-weighted LIN & RIN AC terminated	101		dB
ε_{OUT}	Output Noise	A-weighted, Inputs terminated to AC GND, Output Referred			
		Right LS only, Mode 1	8		μV
		LS: Mode 1	8		μV
		LS: Mode 2	11		μV
		LS: Mode 3	14		μV
		HP: Mode 4	8		μV
		HP: Mode 8	9		μV
		HP: Mode 12	11		μV
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{P-P}, f_{RIPPLE} = 217Hz, C_B = 2.2μF All inputs AC terminated to GND, output referred			
		LS: Mode 1, R_L = 8Ω BTL	90		dB
		LS: Mode 2, R_L = 8Ω BTL	70		dB
		HP: Mode 4, R_L = 32Ω SE	87		dB
		HP: Mode 8, R_L = 32Ω SE	77		dB
CMRR	Common-Mode Rejection Ratio	f = 217Hz, V_{CM} = 1V_{P-P} LS: R_L = 8Ω BTL, Mode 1 HP: R_L = 32Ω SE, Mode 4	60 66		dB dB
X_{TALK}	Crosstalk	LS: P_O = 1W, f = 1kHz, Mode 2	80		dB
		HP: P_O = 12mW, f = 1kHz, Mode 8	70		dB
Z_{IN}	MIN, LIN, and RIN Input Impedance	Maximum Gain setting	12.5		kΩ
		Maximum Attenuation setting	110		kΩ
VOL	Digital Volume Control Range	Maximum Gain Maximum Attenuation	18 –80		dB dB
VOL	Volume Control Step Size Error		0.2		dB
T_{WU}	Wake-Up Time from Shutdown	C_B = 2.2μF, HP, Normal Turn-On Mode	29		ms
		C_B = 2.2μF, HP, Fast Turn-On Mode	16		ms

I^2C Interface (Notes 1, 2)

The following specifications apply for V_{DD} = 5.0V and 3.3V, 2.2V ≤ $I^2C\_V_{DD}$ ≤ 5.5V, T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	LM49200 Typical (Note 4)	LM49200 Limits (Notes 7, 8)	Units (Limits)
t_1	I^2C Clock Period			2.5	μs (min)
t_2	I^2C Data Setup Time			100	ns (min)
t_3	I^2C Data Stable Time			0	ns (min)
t_4	Start Condition Time			100	ns (min)
t_5	Stop Condition Time			100	ns (min)
t_6	I^2C Data Hold Time			100	ns (min)
V_{IH}	I^2C Input Voltage High			$0.7xI^2CV_{DD}$	V (min)
V_{IL}	I^2C Input Voltage Low			$0.3xI^2CV_{DD}$	V (max)

I^2C Interface (Notes 1, 2)

The following specifications apply for V_{DD} = 5.0V and 3.3V, 1.7V ≤ $I^2C\_V_{DD}$ ≤ 2.2V, T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	LM49200 Typical (Note 6)	LM49200 Limits (Notes 7, 8)	Units (Limits)
t_1	I^2C Clock Period			2.5	μs (min)
t_2	I^2C Data Setup Time			250	ns (min)
t_3	I^2C Data Stable Time			0	ns (min)
t_4	Start Condition Time			250	ns (min)
t_5	Stop Condition Time			250	ns (min)
t_6	I^2C Data Hold Time			250	ns (min)
V_{IH}	I^2C Input Voltage High			$0.7xI^2CV_{DD}$	V (min)
V_{IL}	I^2C Input Voltage Low			$0.3xI^2CV_{DD}$	V (max)

Note 1: *"Absolute Maximum Ratings"* indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified

Note 2: The *Electrical Characteristics* tables list guaranteed specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in *Absolute Maximum Ratings*, whichever is lower.

Note 4: Human body model, applicable std. JESD22-A114C.

Note 5: Machine model, applicable std. JESD22-A115-A.

Note 6: Typical values represent most likely parametric norms at T_A = +25°C, and at the *Recommended Operation Conditions* at the time of product characterization and are not guaranteed.

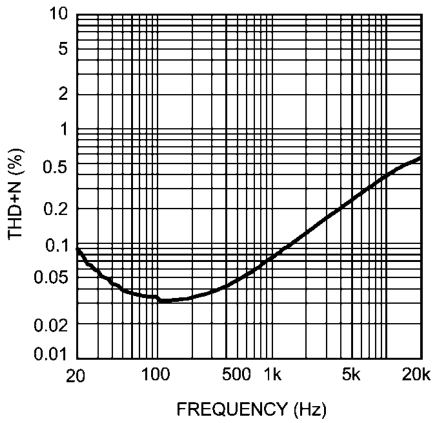
Note 7: Datasheet min/max specification limits are guaranteed by test or statistical analysis.

Note 8: Refer to the I^2C timing diagram, Figure 2.

Typical Performance Characteristics

For all performance graphs, the Output Gains are set to 0dB, unless otherwise noted.

THD+N vs Frequency
V_{DD} = 3.3V, R_L = 8Ω, P_O = 250mW
Mode 1, 80kHz BW



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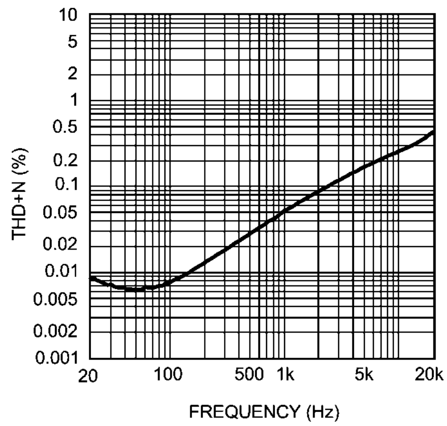
THD+N vs Frequency
V_{DD} = 3.3V, R_L = 8Ω, P_O = 250mW
Mode 2, 80kHz BW



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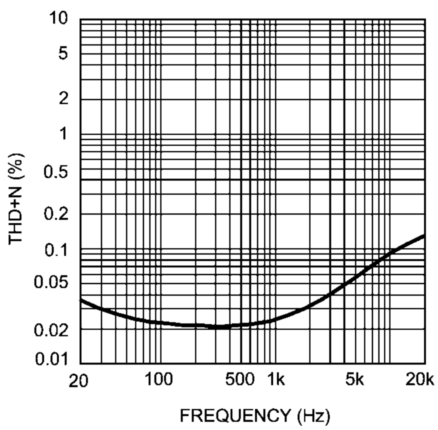
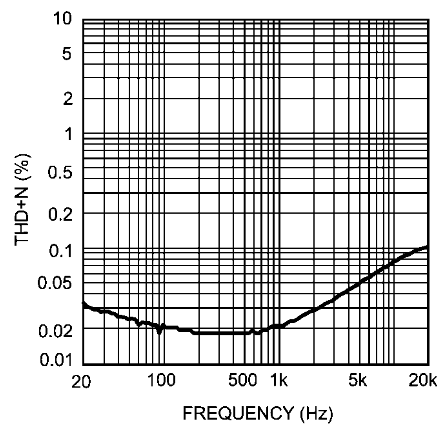
THD+N vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, P_O = 12mW/Ch
Mode 4, 80kHz BW



30062764

THD+N vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, P_O = 12mW/Ch
Mode 8, 80kHz BW



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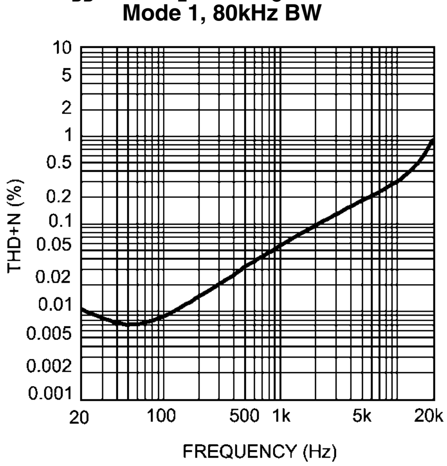
THD+N vs Frequency
V_{DD} = 5V, R_L = 8Ω, P_O = 600mW
Mode 1, 80kHz BW



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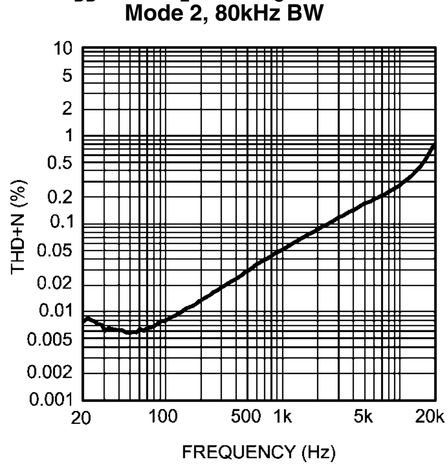
THD+N vs Frequency
V_{DD} = 5V, R_L = 8Ω, P_O = 600mW
Mode 2, 80kHz BW



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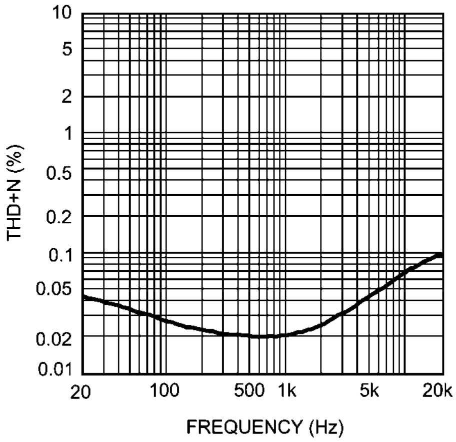
THD+N vs Frequency
V_{DD} = 5V, R_L = 32Ω, P_O = 12mW/Ch
Mode 4, 80kHz BW



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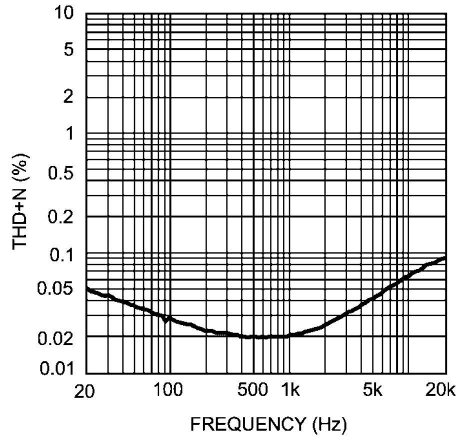
THD+N vs Frequency
V_{DD} = 5V, R_L = 32Ω, P_O = 12mW/Ch
Mode 8, 80kHz BW



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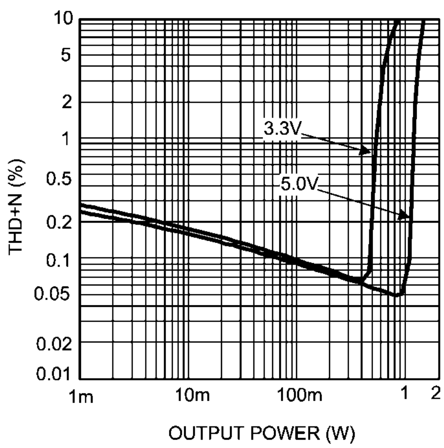
THD+N vs Output Power
V_{DD} = 3.3V & 5V, R_L = 8Ω BTL, f = 1kHz
Mode 1, 80kHz BW



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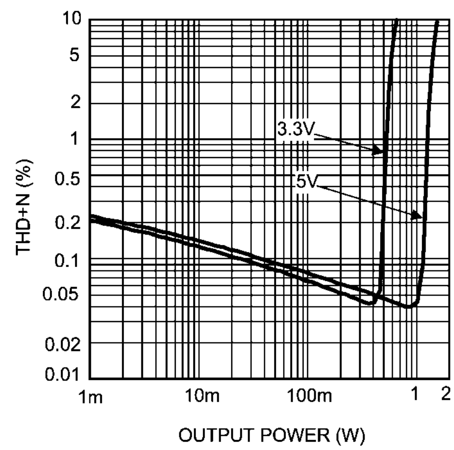
THD+N vs Output Power
V_{DD} = 3.3V & 5V, R_L = 8Ω BTL, f = 1kHz
Mode 2, 80kHz BW



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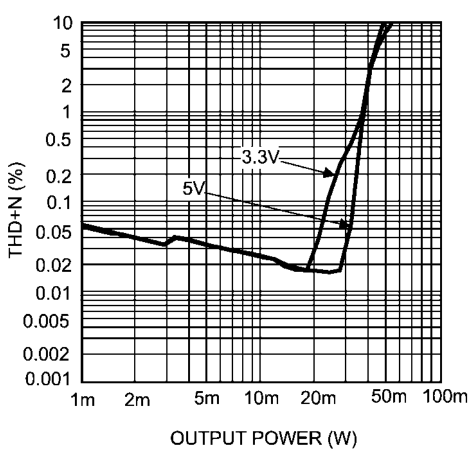
THD+N vs Output Power
V_{DD} = 3.3V & 5V, R_L = 32Ω, f = 1kHz
Mode 4, 80kHz BW



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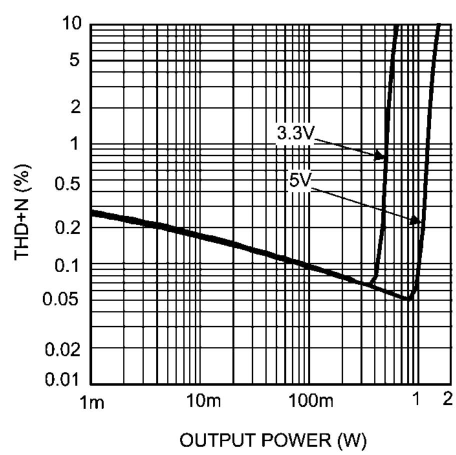
THD+N vs Output Power
V_{DD} = 3.3V & 5V, R_L = 8Ω, f = 1kHz
Mode 5, 80kHz BW



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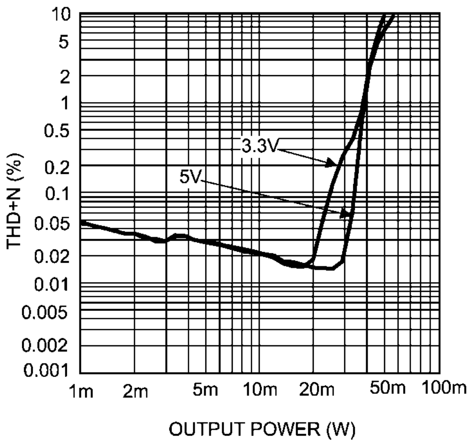
THD+N vs Output Power
V_{DD} = 3.3V & 5V, R_L = 32Ω, f = 1kHz
Mode 8, 80kHz BW



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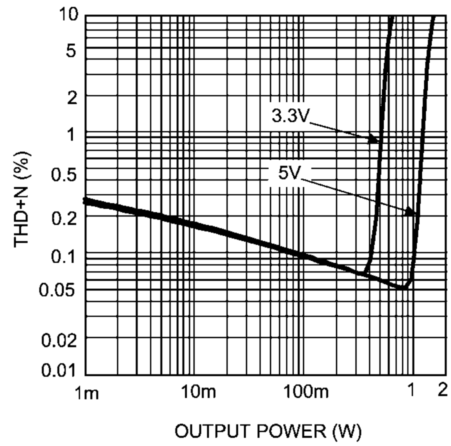
THD+N vs Output Power
V_{DD} = 3.3V & 5V, R_L = 8Ω BTL, f = 1kHz
Mode 10, 80kHz BW



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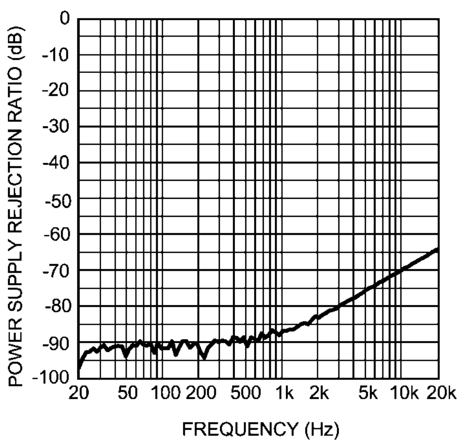
PSRR vs Frequency
V_{DD} = 3.3V, V_{RIPPLE} = 200mV_{P-P}, R_L = 8Ω
Mode 1, 80kHz BW



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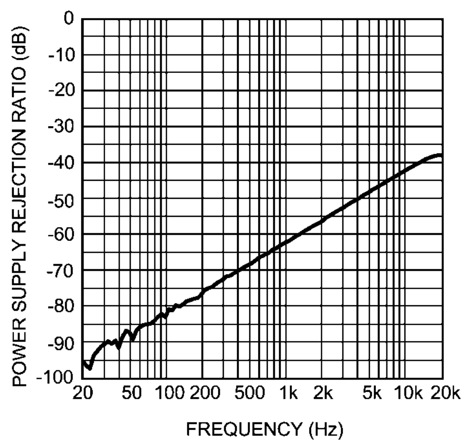
PSRR vs Frequency
V_{DD} = 3.3V, V_{RIPPLE} = 200mV_{P-P}, R_L = 8Ω
Mode 2, 80kHz BW



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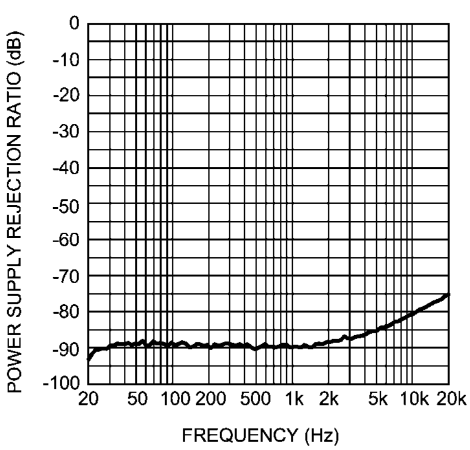
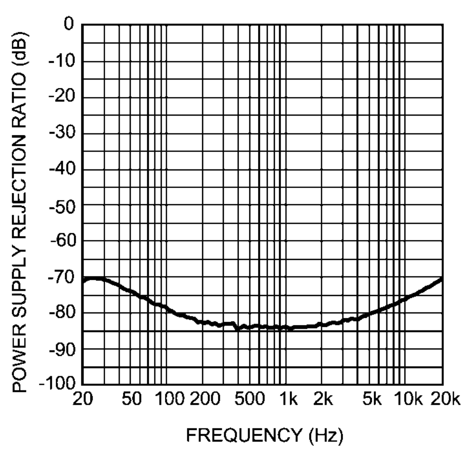
PSRR vs Frequency
V_{DD} = 3.3V, V_{RIPPLE} = 200mV_{P-P}, R_L =32Ω
Mode 4, 80kHz BW



30062756

PSRR vs Frequency
V_{DD} = 3.3V, V_{RIPPLE} = 200mV_{P-P}, R_L = 32Ω
Mode 8, 80kHz BW



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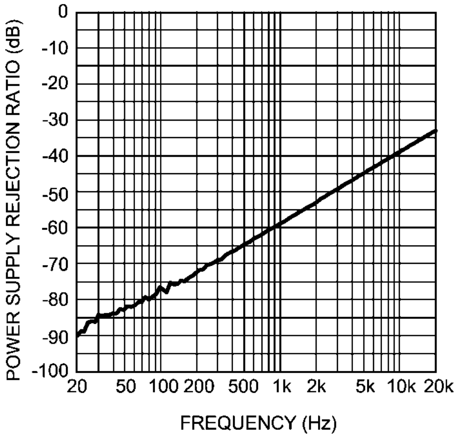
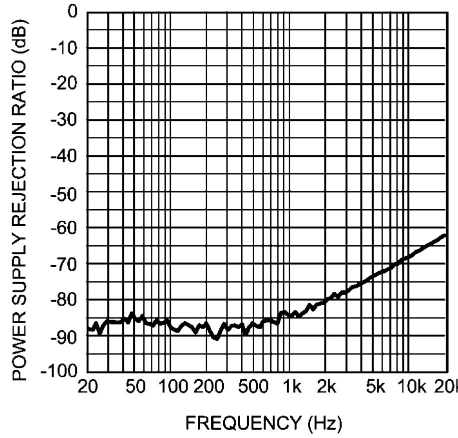
PSRR vs Frequency
V_{DD} = 5V, V_{RIPPLE} = 200mV_{P-P}, R_L = 8Ω
Mode 1, 80kHz BW



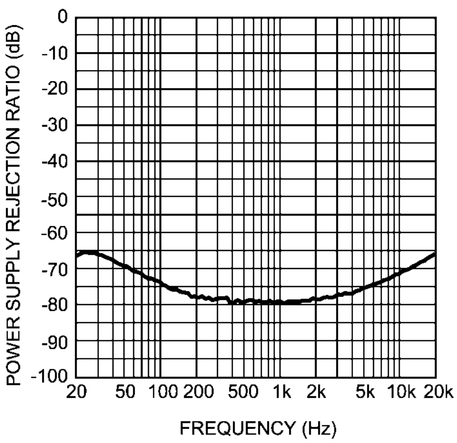
30062759

PSRR vs Frequency
V_{DD} = 5V, V_{RIPPLE} = 200mV_{P-P}, R_L = 32Ω
Mode 4, 80kHz BW



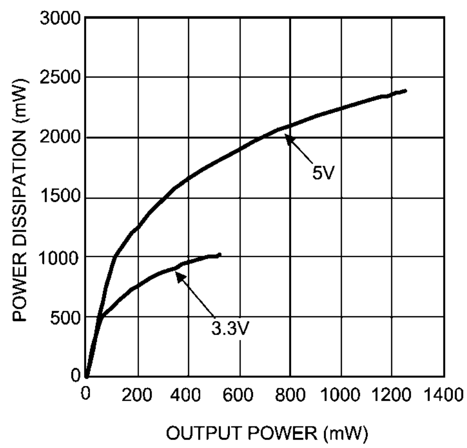
30062760

PSRR vs Frequency
V_{DD} = 5V, V_{RIPPLE} = 200mV_{P-P}, R_L = 32Ω
Mode 8, 80kHz BW



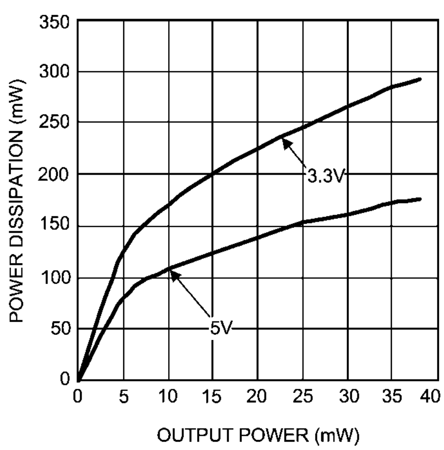
30062761

Power Dissipation vs Output Power
V_{DD} = 3.3V & 5V, R_L = 8Ω BTL
Mode 3, 80kHz BW



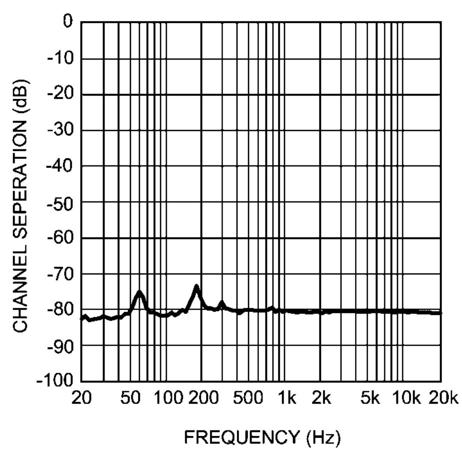
30062788

Power Dissipation vs Output Power
V_{DD} = 3.3V & 5V, R_L = 32Ω SE
Mode 12, 80kHz BW



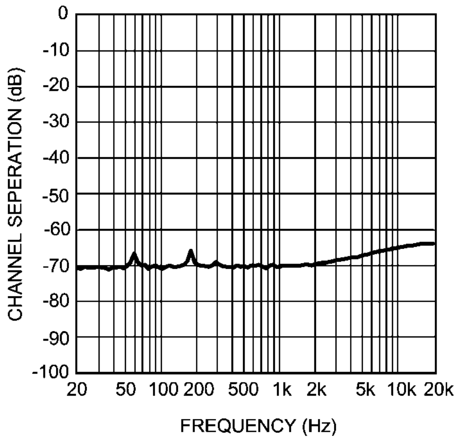
30062789

Crosstalk vs Frequency
V_{DD} = 5.0V, V_{IN} = 1V_{P-P}, R_L = 8Ω
Mode 2, 80kHz BW



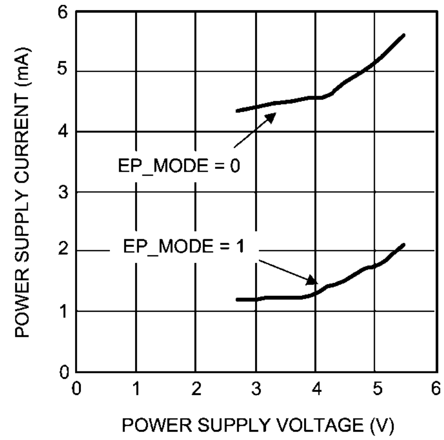
30062784

Crosstalk vs Frequency
V_{DD} = 5.0V, V_{IN} = 1V_{P-P}, R_L = 32Ω
Mode 8, 80kHz BW



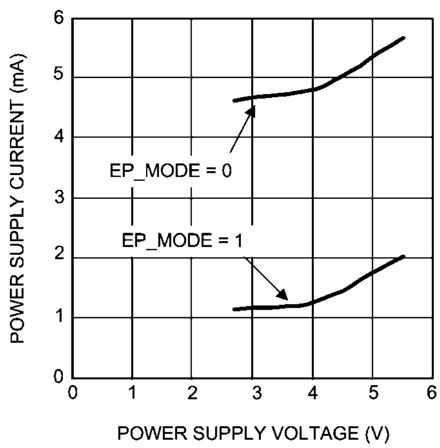
30062785

Supply Current vs Supply Voltage
No Load, Mode 3
(2 plots, output gain amps on/off)



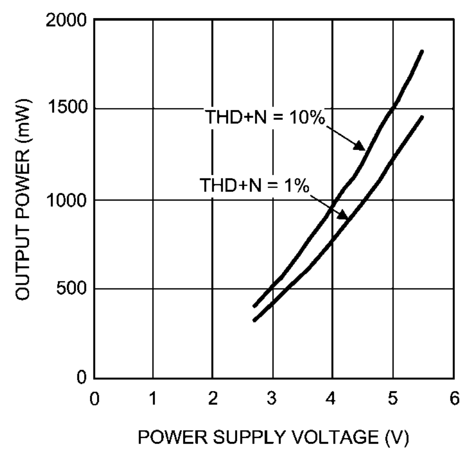
30062790

Supply Current vs Supply Voltage
No Load, Mode 12
(2 plots, output gain amps on/off)



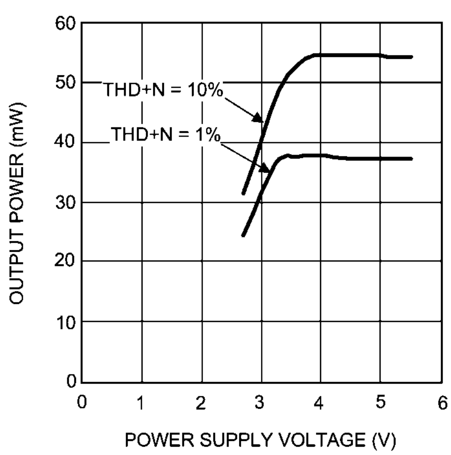
30062791

Output Power vs Supply Voltage
f = 1kHz, R_L = 8Ω BTL
Mode 2, 80kHz BW



30062786

Output Power vs Supply Voltage
f = 1kHz, R_L = 32Ω SE
Mode 8, 80kHz BW



30062787

Application Information

I²C COMPATIBLE INTERFACE

The LM49200 is controlled through an I²C compatible serial interface that consists of a serial data line (SDA) and a serial clock (SCL). The clock line is uni-directional. The data line is bi-directional (open drain). The LM49200 and the master can communicate at clock rates up to 400kHz. Figure 2 shows the I²C interface timing diagram. Data on the SDA line must be stable during the HIGH period of SCL. The LM49200 is a transmit/receive slave-only device, reliant upon the master to generate the SCL signal. Each transmission sequence is framed by a START condition and a STOP condition (Figure 3). Each data word, device address and data, transmitted over the bus is 8 bits long and is always followed by an acknowledge pulse (Figure 4). The LM49200 device address is 11111000.

I²C INTERFACE POWER SUPPLY PIN (I^2CV_{DD})

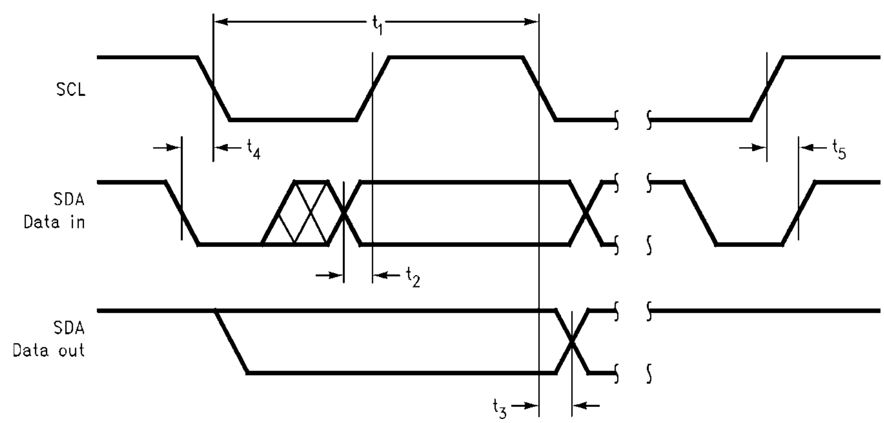
The LM49200's I²C interface is powered up through the I^2CV_{DD} pin. The LM49200's I²C interface operates at a voltage level set by the I^2CV_{DD} pin which can be set independent to that of the main power supply pin V_{DD}. This is ideal whenever logic levels for the I²C interface are dictated by a microcontroller or microprocessor that is operating at a lower supply voltage than the main battery of a portable system

I²C BUS FORMAT

The I²C bus format is shown in Figure 4. The START signal, the transition of SDA from HIGH to LOW while SCL is HIGH, is generated, alerting all devices on the bus that a device address is being written to the bus.

The 7-bit device address is written to the bus, most significant bit (MSB) first, followed by the R/$\overline{W}$ bit. R/$\overline{W}$ = 0 indicates the master is writing to the slave device, R/$\overline{W}$ = 1 indicates the master wants to read data from the slave device. Set R/$\overline{W}$ = 0; the LM49200 is a WRITE-ONLY device and will not respond to the R/$\overline{W}$ = 1. The data is latched in on the rising edge of the clock. Each address bit must be stable while SCL is HIGH. After the last address bit is transmitted, the master device releases SDA, during which time, an acknowledge clock pulse is generated by the slave device. If the LM49200 receives the correct address, the device pulls the SDA line low, generating an acknowledge bit (ACK).

Once the master device registers the ACK bit, the 8-bit register data word is sent. Each data bit should be stable while SCL is HIGH. After the 8-bit register data word is sent, the LM49200 sends another ACK bit. Following the acknowledgement of the register data word, the master issues a STOP bit, allowing SDA to go high while SCL is high.



300627s0

FIGURE 2. I²C Timing Diagram

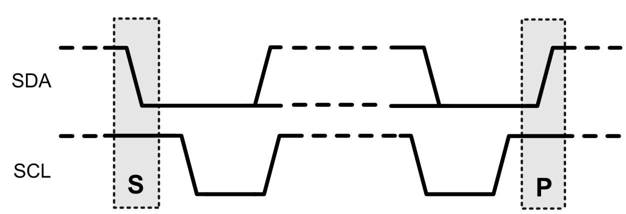


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FIGURE 3. Start and Stop Diagram

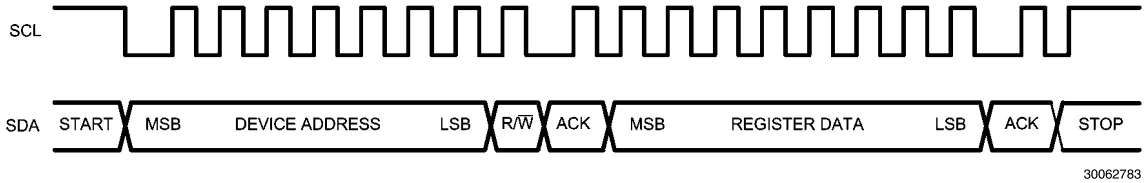


FIGURE 4. Start and Stop Diagram

TABLE 1. Chip Address

	A7	A6	A5	A4	A3	A2	A1	A0
Chip Address	1	1	1	1	1	0	0	0

TABLE 2. Control Registers

Register	D7	D6	D5	D4	D3	D2	D1	D0
Shutdown Control	0	0	0	HPR_SD (1)	0	I^2CV_{DD}_SD(2)	Turn_On _Time (3)	Power_On (4)
Output Mode Control	0	1	0	EP_Mode(5)	Mode_Control (6)			
Headphone Output Gain Control	1	0	0	0	0	HP_Gain (7)		
Mono Input Volume Control	1	0	1	Mono_Vol (8)				
Left Input Volume Control	1	1	0	Left_Vol (8)				
Right Input Volume Control	1	1	1	Right_Vol (8)				

Notes: All registers default to 0 on initial power-up.

1. HPR_SD: Right channel shutdown control. See Table 3.
2. I^2CV_{DD}_SD: Control Enable Function. I^2CV_{DD} can be used to act as a hardware reset input. See Table 3.
3. Turn_On_Time: Reduces the turn on time for faster activation. See Table 3.
4. Power_On: Master Power on bit. See Table 3.
5. EP_Mode: EP (Receiver) Mode control. Right loudspeaker channel can be used as earpiece path. See Table 4.
6. Mode_Control: Sets the output mode. See Tables 4.
7. HP_Gain: Sets the headphone amplifier output gain. See Table 5
8. Mono_Vol/Left_Vol/Right_Vol: Sets the input volume for Mono, Left and Right inputs. See Table 6.

TABLE 3. Shutdown Control Register

Bit	Name	Value	Description
0	Power_On	This bit is a master shutdown control bit and sets the device to be on or off.	
		Value	Status
		0	Master power off, device disable.
		1	Master power on, device enable.
1	Turn_On_Time	This bit sets the turn on time of the device.	
		Value	Status
		0	Normal Turn-on time
		1	Fast Turn-on time
2	I^2CV_{DD}_SD	This bit allows the I^2C supply voltage to be used as a reset signal.	
		Value	Status
		0	I^2CV_{DD} acts as an active low reset input. If I^2CV_{DD} drops below 1.1V, the device resets and the I^2C registers are restored to their default state.
		1	Normal Operation. I^2CV_{DD} voltage does not reset the device.
4	HPR_SD	This bit is used when only one channel of the headphone amplifier is needed.	
		0	Normal headphone operation.
		1	Mono headphone output at left channel, right headphone in shutdown.

TABLE 4. Output Mode Control Register (see key below table)

Bits	Field	Description					
3:0	Mode_Control	These bits determine how the input signals are mixed and routed to the outputs.					
		Value	Mode	Left Loudspeaker	Right Loudspeaker	Left Headphone	Right Headphone
		0000	0	SD	SD	SD	SD
		0001	1	G_M x M	G_M x M	Mute	Mute
		0010	2	G_L x L	G_L x L	Mute	Mute
		011	3	G_L x L + G_M x M	G_R x R + G_M x M	Mute	Mute
		0100	4	SD	SD	G_M x M/2	G_M x M/2
		0101	5	G_M x M	G_M x M	G_M x M/2	G_M x M/2
		0110	6	G_L x L	G_R x R	G_M x M/2	G_M x M/2
		0111	7	G_L x L + G_M x M	G_L x L + G_M x M	G_M x M/2	G_M x M/2
		1000	8	SD	SD	G_L x L	G_R x R
		1001	9	G_M x M	G_M x M	G_L x L	G_R x R
		1010	10	G_L x L	G_R x R	G_L x L	G_R x R
		1011	11	G_L x L + G_M x M	G_R x R + G_M x M	G_L x L	G_R x R
		1100	12	SD	SD	G_L x L + G_M x M/2	G_R x R + G_M x M/2
		1101	13	G_M x M	G_M x M	G_L x L + G_M x M/2	G_R x R + G_M x M/2
		1110	14	G_L x L	G_R x R	G_L x L + G_M x M/2	G_R x R + G_M x M/2
		1111	15	G_L x L + G_M x M	G_R x R + G_M x M	G_L x L + G_M x M/2	G_R x R + G_M x M/2
4	EP Mode	This bit sets the loudspeaker amplifiers for earpiece mode.					
		Value	Status				
		0	Normal loudspeaker operation, control determined by bits 3:0.				
		1	Bit overrides bits 3:0. Right loudspeaker amplifier bias current reduced for low power operation. Left loudspeaker amplifier shutdown. Mono input path active and signal routed to right loudspeaker output. Left & right input gain amplifiers shutdown for reduced power consumption.				

M : MIN, Mono differential input

L : LIN, Left single-ended input
R : RIN, Right single-ended input
SD : Shutdown
G_M : Mono_Vol setting determined by the Mono Input Volume Control register, See Table 6.
G_L : Left_Vol setting determined by the Left Input Volume Control register, See Table 6.
G_R : Right_Vol setting determined by the Right Input Volume Control register, See Table 6.

TABLE 5. Output Gain Control Register

Bits	Field	Description	
2:0	HP_GAIN	These bits set the gain of the headphone output amplifiers.	
		Value	Gain (dB)
		000	0
		001	–1.2
		010	–2.5
		011	–4.0
		100	–6.0
		101	–8.5
		110	–12
		111	–18

TABLE 6. Input Volume Control Registers

Bits	Fields	Description		
4:0	Mono_Vol Right_Vol Left_Vol	These bits set the input volume for each input volume register listed.		
		Volume Step	Value	Gain (dB)
		1	00000	–80.0
		2	00001	–46.5
		3	00010	–40.5
		4	00011	–34.5
		5	00100	–30.0
		6	00101	–27.0
		7	00110	–24.0
		8	00111	–21.0
		9	01000	–18.0
		10	01001	–15.0
		11	01010	–13.5
		12	01011	–12.0
		13	01100	–10.5
		14	01101	–9.0
		15	01110	–7.5
		16	01111	–6.0
		17	10000	–4.5
		18	10001	–3.0
		19	10010	–1.5
		20	10011	0.0
		21	10100	1.5
		22	10101	3.0
		23	10110	4.5
		24	10111	6.0
		25	11000	7.5
		26	11001	9.0
		27	11010	10.5
		28	11011	12.0
		29	11100	13.5
		30	11101	15.0
		31	11110	16.5
		32	11111	18.0

TURN_ON_TIME BIT

The Turn_On_Time bit determines the delay time from the Power_On bit set to '1' and the internal circuits ready. For input capacitor values up to 0.47μF the Turn_On_Time bit can be set to fast mode by setting the bit to a '1'. When the input capacitor values are larger than 0.47μF then the Turn_On_Time bit should be set to '0' for normal turn-on time and higher delay. This allows sufficient time to charge the input capacitors to the ½ V_{DD}LS bias voltage.

POWER_ON BIT

The Power_On bit is the master control bit to activate or deactivate the LM49200. All registers can be loaded independent of the Power_On bit setting as long as the IC is powered correctly. Cycling the Power_On bit does not change the values of any registers nor return all bits to the default power on value of zero. The Power_On bit only determines whether the IC is on or off.

HPR_SD BIT

The HPR_SD bit will deactivate the right headphone output amplifier. This bit is provided to reduce power consumption when only one headphone output is needed.

MODE_CONTROL BITS

In the LM49200 OUTPUT MODE CONTROL register (Table 4), Bit B5 (EP Bypass) controls the operation of the Earpiece Bypass path. If EP Bypass = 0, it would act under normal output mode operation set by bits B3, B2, B1, and B0. If EP Bypass = 1, it overrides the B3, B2, B1, and B0 Bits and enables the Receiver Bypass path, a class AB amplifier, to the speaker output.

Bit B4 (HPR_SD) of the OUPUT MODE CONTROL register controls the right headphone shutdown. If HPR_SD = 1, the right headphone output is disabled.

The LM49200 includes a comprehensive mixer multiplexer controlled through the I²C interface. The mixer/multiplexer allows any input combination to appear on any output of LM49200. Multiple input paths can be selected simultaneously. Under these conditions, the selected inputs are mixed together and output on the selected channel. Table 5 shows how the input signals are mixed together for each possible input selection.

HP_GAIN BITS

The headphone outputs have an additional, single volume control set by the three HP_Gain bits in the Output Gain Control register. The HP_Gain volume setting controls the output level for both the left and the right headphone outputs.

LS (EP_MODE) BIT

The LS (EP_Mode) bit selects the amount of bias current in the loudspeaker amplifier. Setting the LS (EP_Mode) bit to a '1' will reduce the amount of current from the V_{DD}LS supply by approximately 0.5mA. The THD performance of the loudspeaker amplifier will be reduced as a result of lower bias current. See the performance graphs in the Typical Performance Characteristics section above.

VOLUME CONTROL BITS

The LM49200 has three independent 32-step volume controls, one for each of the inputs. The five bits of the Volume Control registers sets the volume for the specified input channel.

SHUTDOWN FUNCTION

The LM49200 features the following shutdown controls.

Bit B4 (GAMP_SD) of the SHUTDOWN CONTROL register controls the gain amplifiers. When GAMP_SD = 1, it disables the gain amplifiers that are not in use. For example, in Modes 1, 4 and 5, the Mono inputs are in use, so the Left and Right input gain amplifiers are disabled, causing the I_{DD} to be minimized.

Bit B0 (PWR_On) of the SHUTDOWN CONTROL register is the global shutdown control for the entire device. Set PWR_On = 0 for normal operation. PWR_On = 1 overrides any other shutdown control bit.

DIFFERENTIAL AMPLIFIER EXPLANATION

The LM49200 features a differential input stage, which offers improved noise rejection compared to a single-ended input amplifier. Because a differential input amplifier amplifies the difference between the two input signals, any component common to both signals is cancelled. An additional benefit of the differential input structure is the possible elimination of the DC input blocking capacitors. Since the DC component is common to both inputs, and thus cancelled by the amplifier, the LM49200 can be used without input coupling capacitors when configured with a differential input signal.

BRIDGE CONFIGURATION EXPLAINED

By driving the load differentially through the MONO outputs, an amplifier configuration commonly referred to as “bridged mode” is established. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of the load is connected to ground.

A bridge amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped.

A bridge configuration, such as the one used in LM49200, also creates a second advantage over single-ended amplifiers. Since the differential outputs are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor, the half-supply bias across the load would result in both increased internal IC power dissipation and also possible loudspeaker damage.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. The power dissipation of the LM49200 varies with the mode selected. The maximum power dissipation occurs in modes where all inputs and outputs are active (Modes 6, 7, 8, 9, 10, 11, 13, 14, 15). The power dissipation is dominated by the Class AB amplifier. The maximum power dissipation for a given application can be derived from the power dissipation graphs or from Equation 1.

$$P_{DMAX} = 4*(V_{DD})^2 / (2\pi^2 R_L) \quad (1)$$

It is critical that the maximum junction temperature (T_{JMAX}) of 150°C is not exceeded. T_{JMAX} can be determined from the power derating curves by using P_{DMAX} and the PC board foil area. By adding additional copper foil, the thermal resistance of the application can be reduced from the free air value, resulting in higher P_{DMAX}. Additional copper foil can be added to any of the leads connected to the LM49200. It is especially effective when connected to V_{DD}, GND, and the output pins. Refer to the application information on the LM49200 reference design board for an example of good heat sinking. If T_{JMAX} still exceeds 150°C, then additional changes must be made. These changes can include reduced supply voltage, higher load impedance, or reduced ambient temperature. Internal power dissipation is a function of output power. Refer to the **Typical Performance Characteristics** curves for power dissipation information for different output powers and output loading.

POWER SUPPLY BYPASSING

As with any amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. Typical applications employ a 5V regulator with 10µF tantalum or electrolytic capacitor and a ceramic bypass capacitor which aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the LM49200. The selection of a bypass capacitor, especially C_B, is dependent upon PSRR requirements, click and pop performance, system cost, and size constraints.

GROUND REFERENCED HEADPHONE AMPLIFIER

The LM49200 features a low noise inverting charge pump that generates an internal negative supply voltage. This allows the headphone outputs to be biased about GND instead of a nominal DC voltage, like traditional headphone amplifiers. Because there is no DC component, the large DC blocking capacitors (typically 220µF) are not necessary. The coupling capacitors are replaced by two small ceramic charge pump capacitors, saving board space and cost. Eliminating the output coupling capacitors also improves low frequency response. In traditional headphone amplifiers, the headphone impedance and the output capacitor from a high-pass filter that not only blocks the DC component of the output, but also attenuates low frequencies, impacting the bass response. Because the LM49200 does not require the output coupling capacitors, the low frequency response of the device is not degraded by external components. In addition to eliminating the output coupling capacitors, the ground referenced output nearly doubles the available dynamic range of the LM49200 headphone amplifiers when compared to a traditional headphone amplifier operating from the same supply voltage.

INPUT CAPACITOR SELECTION

Input capacitors may be required for some applications, or when the audio source is single-ended. Input capacitors block the DC component of the audio signal, eliminating any conflict between the DC component of the audio source and the bias voltage of the LM49200. The input capacitors create a high-pass filter with the input resistors R_{IN}. The -3dB point of the high-pass filter is found using equation below.

$$f = 1 / 2\pi R_{IN} C_{IN} \quad \text{(Hz)} \qquad (2)$$

Where the value of R_{IN} is given in the Electrical Characteristics Table.

High-pass filtering the audio signal helps protect the speakers. When the LM49200 is using a single-ended source, power supply noise on the ground is seen as an input signal. Setting the high-pass filter point above the power supply noise frequencies, 217Hz in a GSM phone, for example, filters out the noise such that it is not amplified and heard on the output. Capacitors with a tolerance of 10% or better are recommended for impedance matching and improved CMRR and PSRR.

CHARGE PUMP FLYING CAPACITOR (C_1)

The flying capacitor (C1), see Figure 1, affects the load regulation and output impedance of the charge pump. A C1 value that is too low results in a loss of current drive, leading to a loss of amplifier headroom. A higher valued C1 improves load regulation and lowers charge pump output impedance to an extent. Above 2.2µF, the $R_{DS(ON)}$ of the charge pump switches and the ESR of C1 and Cs5 dominate the output impedance. A lower value capacitor can be used in systems with low maximum output power requirements.

CHARGE PUMP HOLD CAPACITOR (C_{S3})

The value and ESR of the hold capacitor (Cs5) directly affects the ripple on CPV_{SS}. Increasing the value of Cs5 reduces output ripple. Decreasing the ESR of Cs5 reduces both output ripple and charge pump output impedance. A lower value capacitor can be used in systems with low maximum output power requirements.

Demo Board Circuit

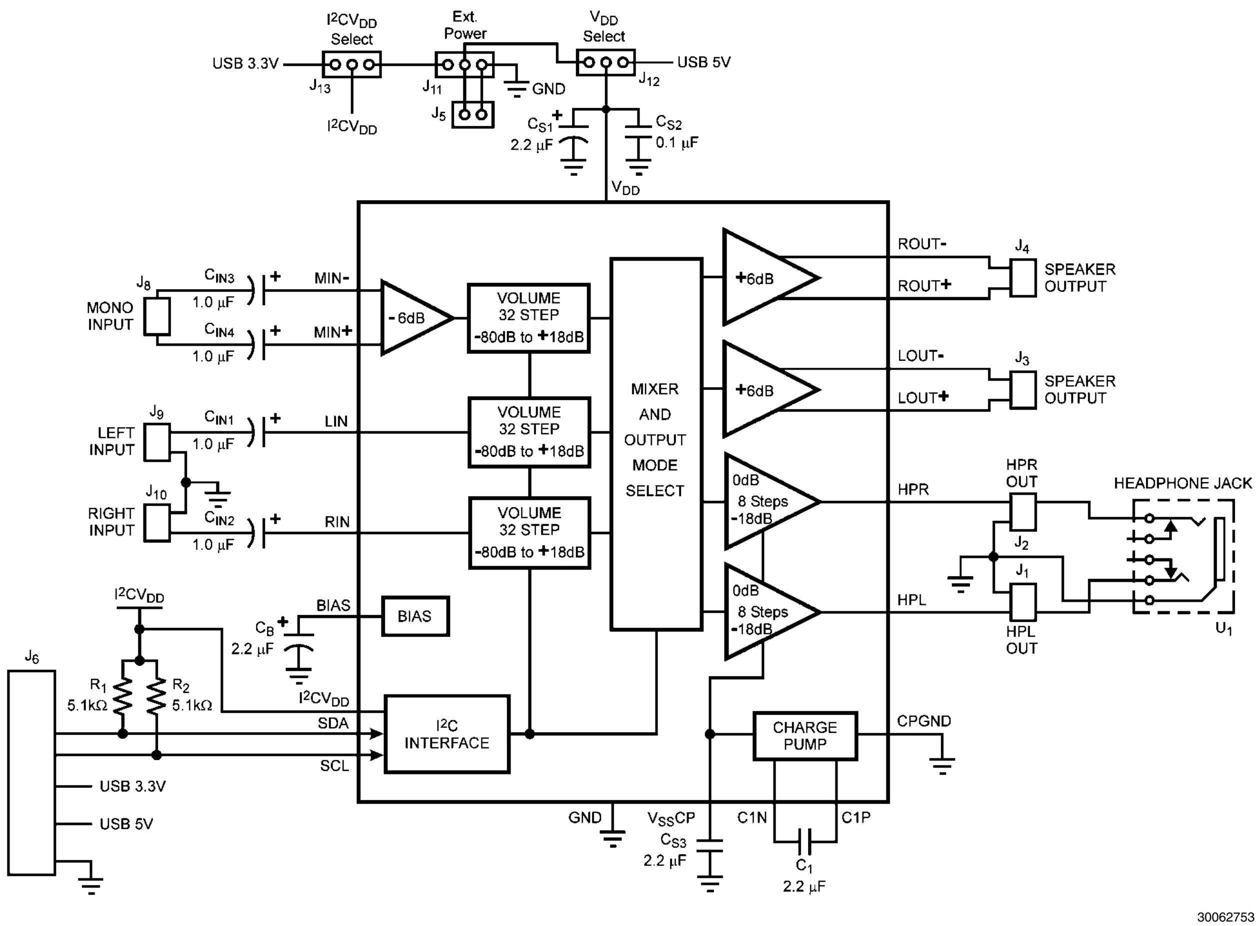


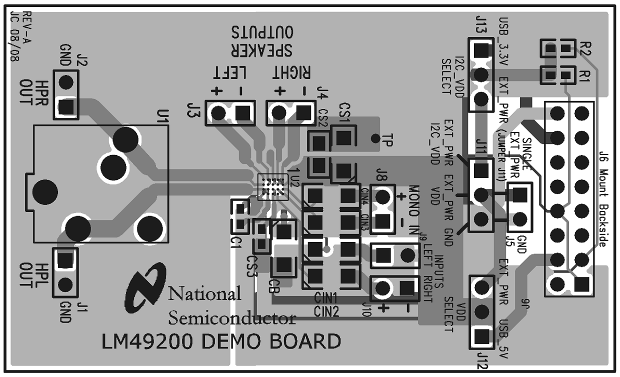
FIGURE 5. Demo Board Circuit

Demonstration Board

The demonstration board (see Figure 5) has connection and jumper options to be powered from the USB bus, from external power supplies or a combination of both. Additional options are to power I^2CV_{DD} and V_{DD} from a single power supply or separate power supplies, as long as the voltage limits for each power supply are not exceeded. See the Operating Ratings for each supply's limit range. When powered from the USB bus the I^2CV_{DD} will be set to 3.3V and the V_{DD} will be set to 5V. Jumper headers J13 and J12 must be set accordingly. If a single power supply for I^2CV_{DD} and V_{DD} is desired then header J5 should be used with a jumper added to header J11 to connect $I2CV_{DD}$ to the external supply voltage connected to J5.

Connection headers J1 and J2 are provided along with the stereo headphone jack J4 for easily connection and monitoring of the headphone outputs.

LM49200 microSMD Demo Board Views



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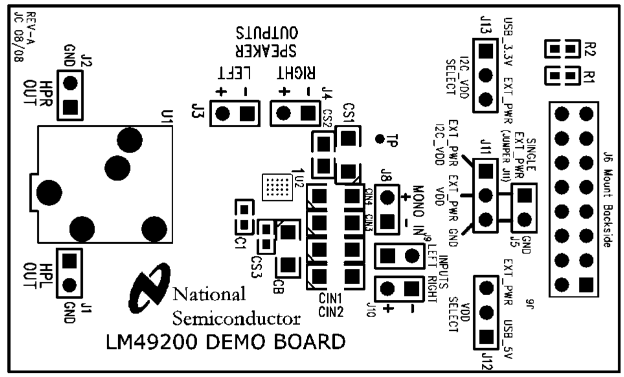
Composite View



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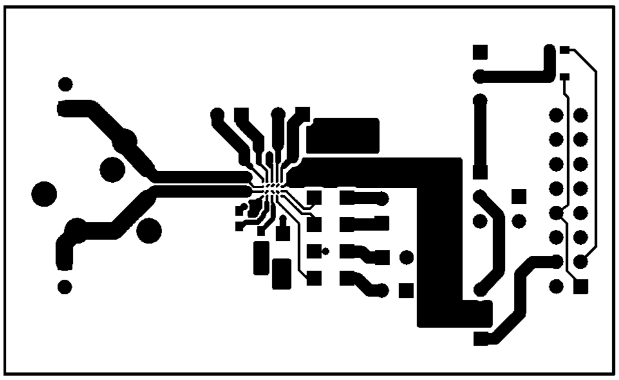
Silk Screen



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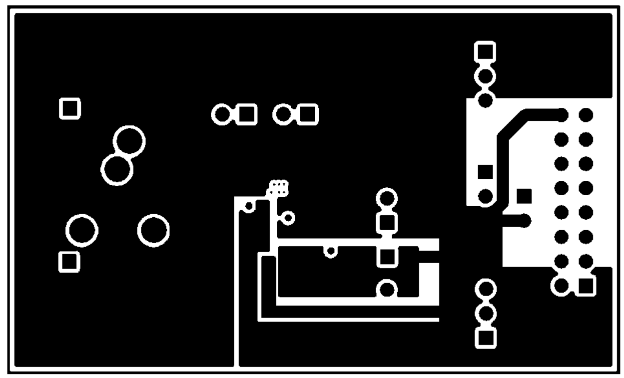
Top Layer



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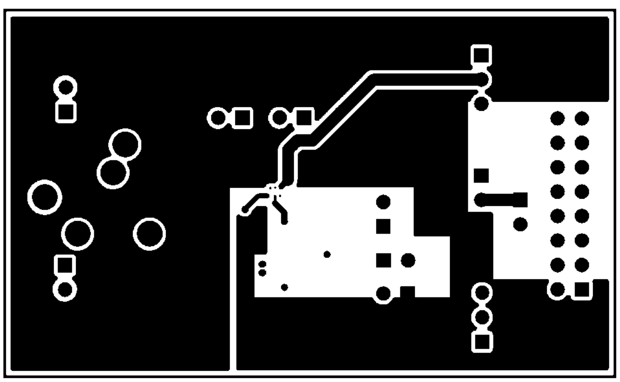
Internal Layer 1



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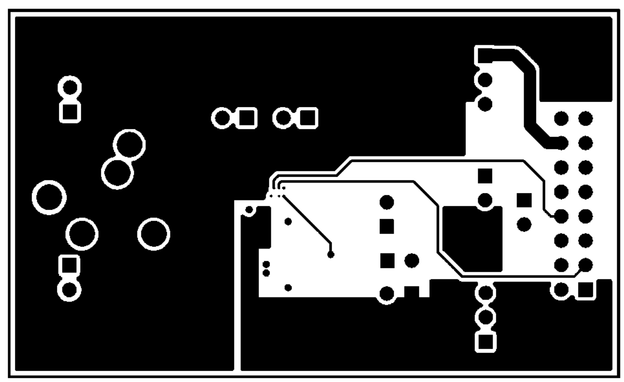
Internal Layer 2



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Bottom Layer

LM49200 Reference Demo Board Bill Of Materials

TABLE 7. Bill Of Materials

Designator	Vlaue	Tolerance	Part Description	Comment
R_1, R_2	5.1kΩ	5%	1/10W, 0603 Resistors	
C_{IN1}, C_{IN2} C_{IN3}, C_{IN4}	1µF	10%	1206, X7R Ceramic Capacitor	
C_{S1}, C_B	2.2µF	10%	Size A, Tantalum Capacitor	
C_{S2}	0.1µF	10%	0805, 16V, X7R Ceramic Capacitor	
C_{S3}, C_1	2.2µF	10%	0603, 10V, X7R Ceramic Capacitor	
U_2			LM49200TL	
J_1, J_2, J_3 J_4, J_5, J_8 J_9, J_{10}			0.100" 1x2 header, vertical mount	Input, Output, V_{DD}, GND
J_{11}, J_{12}, J_{13}			0.100" 1x3 header, vertical mount	V_{DD} Selects, V_{DD}, I^2CV_{DD}, GND
J_6			16 pin header	I^2C Connector
U_1			Headphone Jack	

PCB Layout Guidelines

This section provides practical guidelines for mixed signal PCB layout that involves various digital/analog power and ground traces. Designers should note that these are only "rule-of-thumb" recommendations and the actual results will depend heavily on the final layout.

General Mixed Signal Layout Recommendations

SINGLE-POINT POWER AND GROUND CONNECTIONS

The analog power traces should be connected to the digital traces through a single point (link). A "Pi-filter" can be helpful in minimizing high frequency noise coupling between the analog and digital sections. It is further recommended to put digital and analog power traces over the corresponding digital and analog ground traces to minimize noise coupling.

PLACEMENT OF DIGITAL AND ANALOG COMPONENTS

All digital components and high-speed digital signals traces should be located as far away as possible from analog components and circuit traces.

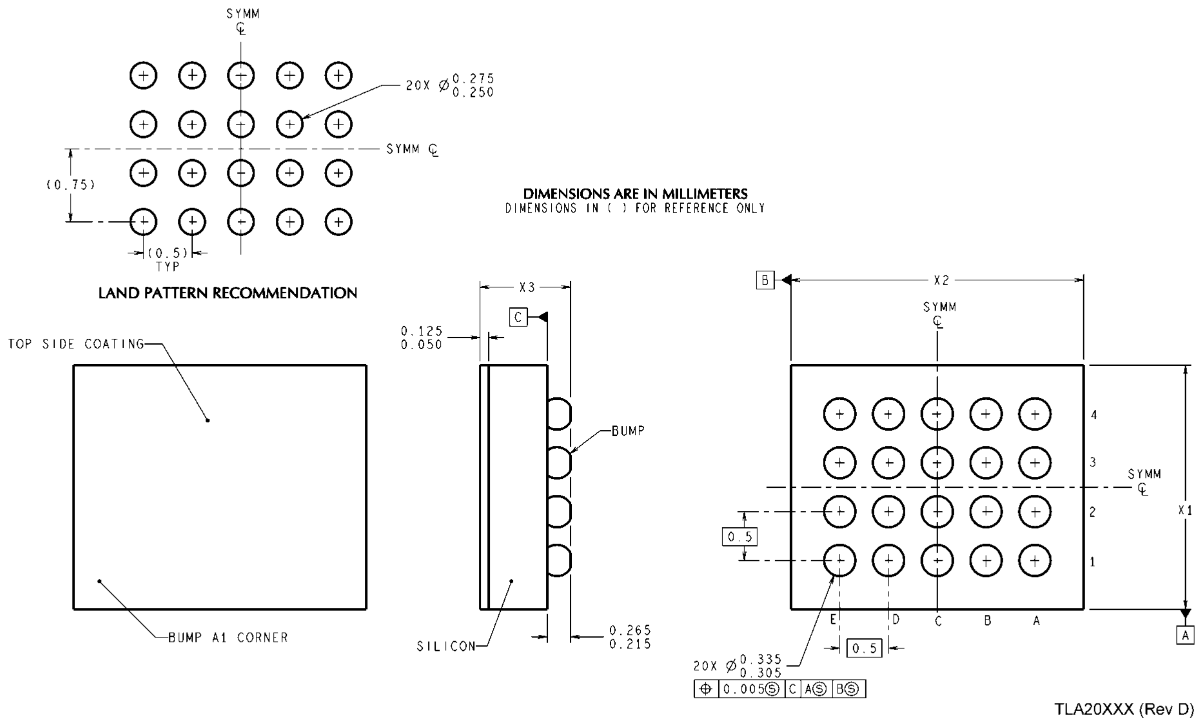
AVOIDING TYPICAL DESIGN AND LAYOUT PROBLEMS

Avoid ground loops or running digital and analog traces parallel to each other (side-by-side) on the same PCB layer. When traces must cross over each other do it at 90 degrees. Running digital and analog traces at 90 degrees to each other from the top to the bottom side as much as possible will minimize capacitive noise coupling and cross talk.

Revision History

Rev	Date	Description
1.0	05/21/09	Initial release.

Physical Dimensions inches (millimeters) unless otherwise noted



20 Bump micro SMD Package
NS Package Number TLA20BBA
X_1 = 2.022±0.030mm X_2 = 2.517±0.030mm, X_3 = 0.600±0.075mm

Notes

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Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Solutions	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
Temperature Sensors	www.national.com/tempsensors	SolarMagic™	www.national.com/solarmagic
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