National Semiconductor

LM4911QMM

Boomer® Audio Power Amplifier Series

October 22, 2010

Stereo Headphone Amplifier for Automotive

General Description

The LM4911QMM stereo headphone amplifier provides up to 145mW per channel of output power. Intended for automotive applications, it is AEC-Q100 grade 2 qualified and packaged in a 10–pin MSOP package.

A low power mute mode features a fast turn on time of 1ms. An ultra low current shutdown mode has a supply current of less than 2μA.

Key Specifications

V_{CC} = 5V, R_L = 16Ω

■ P_{OUT}, THD+N = 1%	145mW
■ THD+N @30mW	0.1%
■ Shutdown Current	2μA
■ ESD, HBM	2kV
■ Temperature Range	–40°C to +105°C

Features

- Mute Mode with Fast Turn On
- 10–Pin MSOP package
- Q grade Level 2 qualified

Block Diagram

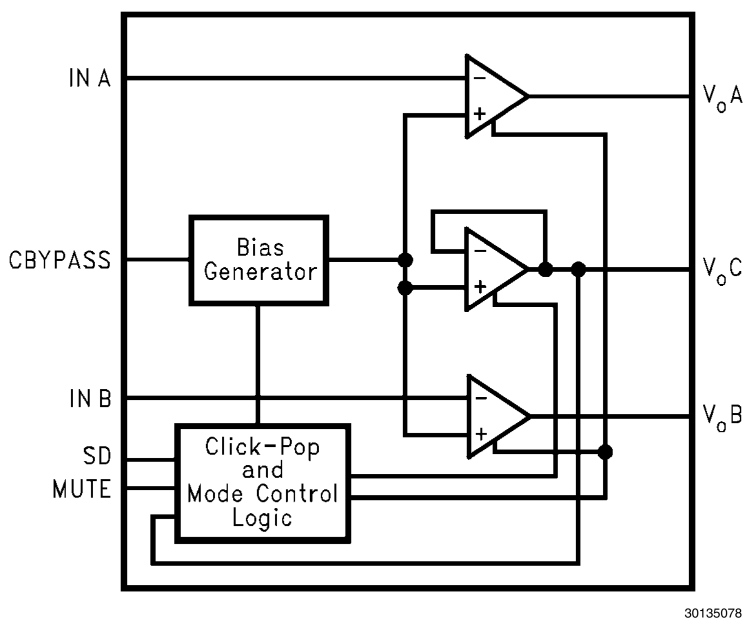

FIGURE 1. Block Diagram

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Typical Application

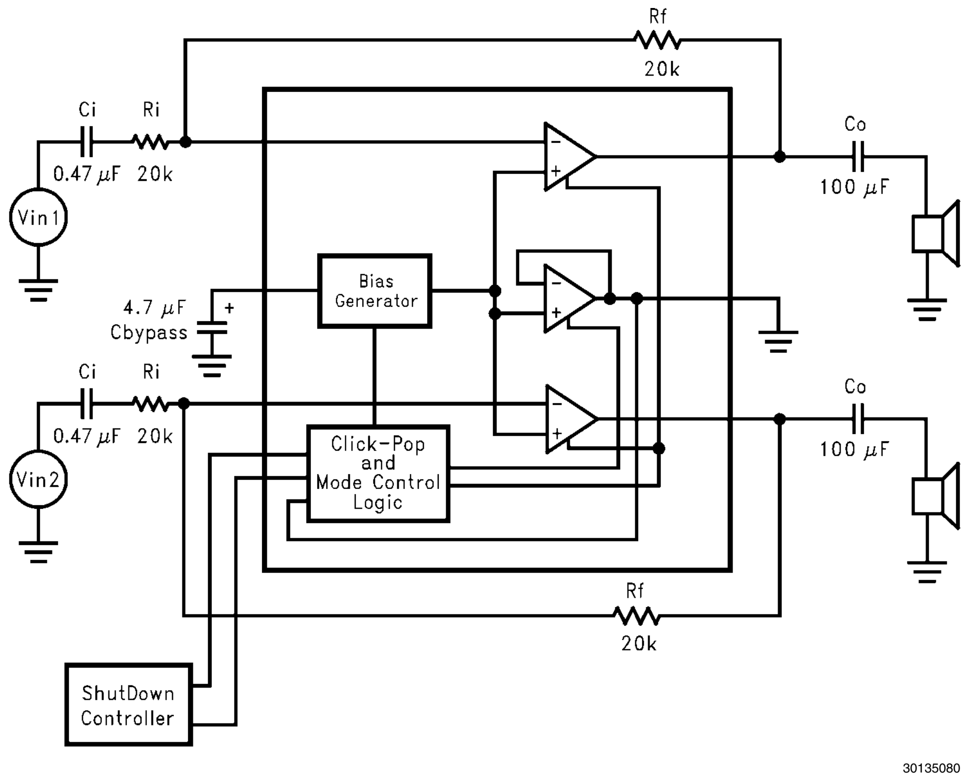

FIGURE 2. Typical Capacitive Coupled Output Configuration Circuit

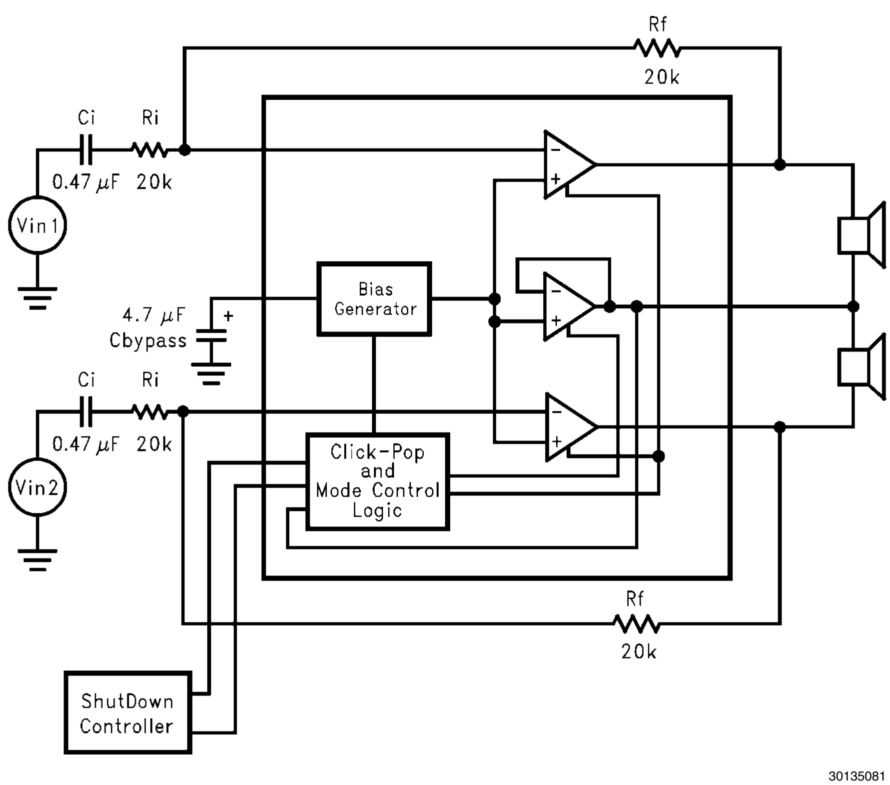

FIGURE 3. Typical OCL Output Configuration Circuit

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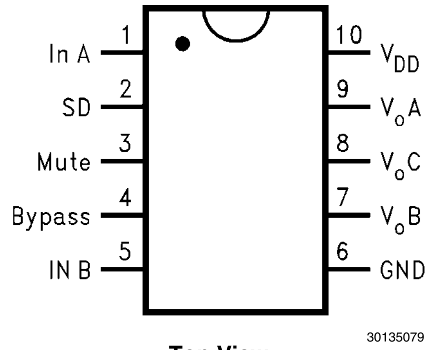
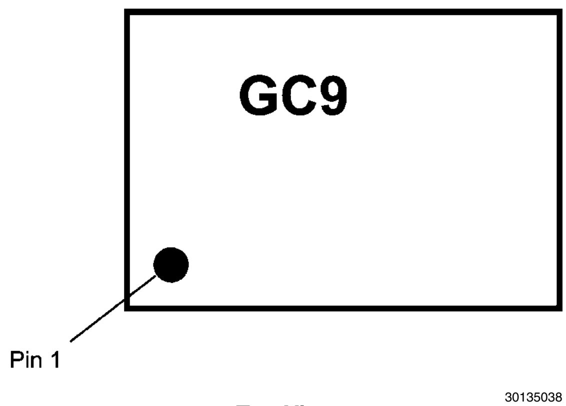
Connection Diagrams

MSOP Package



Top View
Order Number LM4911QMM
See NS Package Number MUB10A

MSOP Marking



Top View
G - Boomer Family
C9 - LM4911QMM

Ordering Information

Order Number	Package	Package Marking	NSC Drawing #	Transport Media
LM4911QMM	10–Pin MSOP	GC9	MUB10A	1k units Tape and Reel
LM4911QMMX	10–Pin MSOP	GC9	MUB10A	3.5k units Tape and Reel

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Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	6.0V
Storage Temperature	–65°C to +150°C
Input Voltage	-0.3V to V_{DD} + 0.3V
Power Dissipation (Note 3)	Internally Limited
Junction Temperature	150°C
ESD Ratings (VOA, VOB, VOC)	
HBM	2000V
Contact Discharge	750v
Machine Model	200V
Thermal Resistance	
θ_{JC} (MSOP)	56°C/W
θ_{JA} (MSOP)	190°C/W

Operating Ratings

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le 105°C$
Supply Voltage (V_{DD})	$4.5V \le V_{CC} \le 5.5V$

Electrical Characteristics V_{DD} = 5.0V (Note 1, Note 2)

Unless otherwise specified, all limits are guaranteed for T_A = +25°C, V_{DD} = 5V, f_{OUT} = 1kHz, R_L = 16Ω, C-CUPL mode

Symbol	Parameter	Conditions	LM4911QMM			Units (Limits)
			MIn	Typ (Note 6)	Limit (Note 7)	
I_{DD}	Supply Current	T_A = +25°C		2	5	mA
		T_A = –40°C to +105°C			6	mA
I_{SD}	Shutdown Current	$\overline{SHUTDOWN}$ = 0V		0.1	2.0	µA
I_M	Mute Current	$V_{MUTE} = V_{DD}$		50	100	µA
P_O	Output Power	THD+N = 1%		145		
		T_A = +25°C	134			mW
		T_A = –40°C to +105°C	**130**			mW
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{P-P} f = 1kHz		65		dB
THD+N	Total Harmonic Distortion +Noise	P_O = 15.3mW		0.1	0.5	%
t_{WU}	Wake Up Time			2		s
t_{UM}	Un Mute Time			10		ms
V_{OS}	Output Offset	Change from SD low to high			1	mV
ε_{OS}	Output Noise	BW = 20 to 20kHz, A-weighted		10		µV
V_{IH}	Input High Voltage	SD, Mute T_A = –40C to +105C	**1.8**			V
V_{IL}	Input Low Voltage	SD, Mute T_A = –40C to +105C			**0.4**	V

Note 1: All voltages are measured with respect to the GND pin unless otherwise specified.

Note 2: : Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: : The maximum power dissipation must be derated at elevated temperatures and is dictated by TJMAX, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/ \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4911QMM, see power derating currents for more information.

Note 4: Human body model, 100pF discharged through a 1.5kΩ resistor.

Note 5: Machine Model, 220pF-240pF discharged through all pins.

Note 6: Typicals are measured at 25°C and represent the parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

Note 9: 10Ω Terminated input.

Note 10: The limit is guaranteed over the temperature range of –40°C to +105°C.

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External Components Description

(*Figure 2*)

Components		Functional Description
1.	R_I	Inverting input resistance which sets the closed-loop gain in conjunction with R_f. This resistor also forms a high-pass filter with C_i at $f_c = 1/(2\pi R_i C_i)$.
2.	C_I	Input coupling capacitor which blocks the DC voltage at the amplifier's input terminals. Also creates a high-pass filter with R_i at $f_c = 1/(2\pi R_i C_i)$. Refer to the section **Proper Selection of External Components,** for an explanation of how to determine the value of C_i.
3.	R_f	Feedback resistance which sets the closed-loop gain in conjunction with R_i.
4.	C_S	Supply bypass capacitor which provides power supply filtering. Refer to the **Power Supply Bypassing** section for information concerning proper placement and selection of the supply bypass capacitor.
5.	C_B	Bypass pin capacitor which provides half-supply filtering. Refer to the section, **Proper Selection of Proper Components**, for information concerning proper placement and selection of C_B
6.	C_o	Output coupling capacitor which blocks the DC voltage at the amplifier's output. Forms a high pass filter with R_L at $f_o = 1/(2\pi R_L C_o)$

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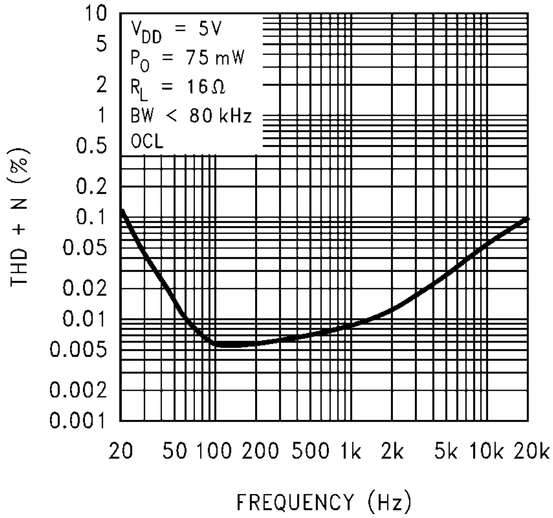
Typical Performance Characteristics

THD+N vs Frequency



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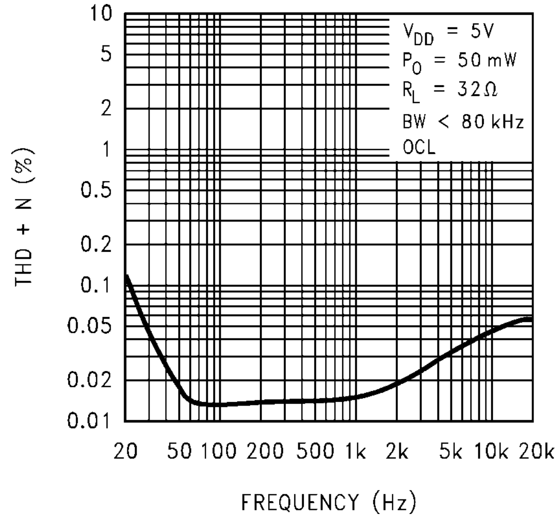
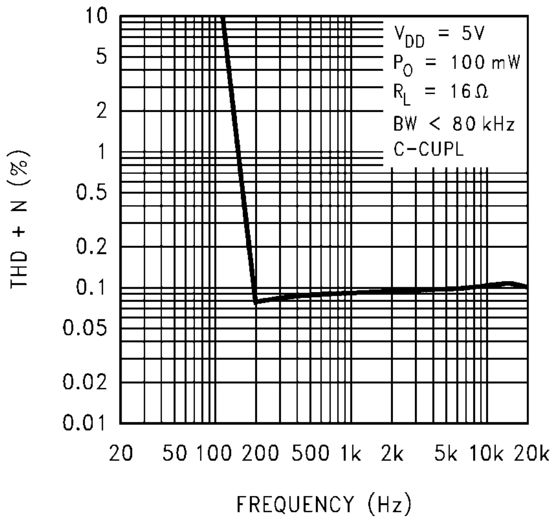
THD+N vs Frequency



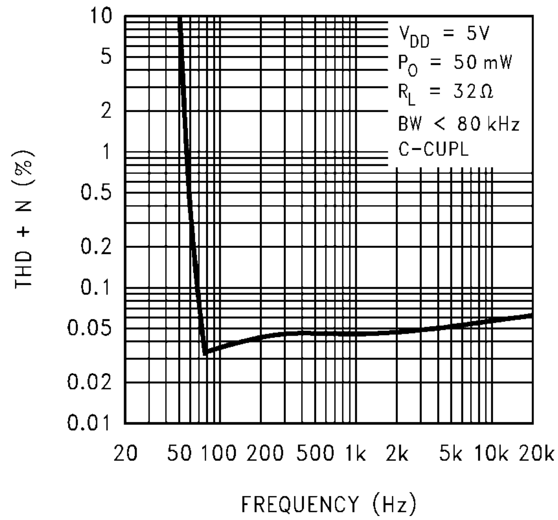
30135083

THD+N vs Frequency



30135084

THD+N vs Frequency



30135085

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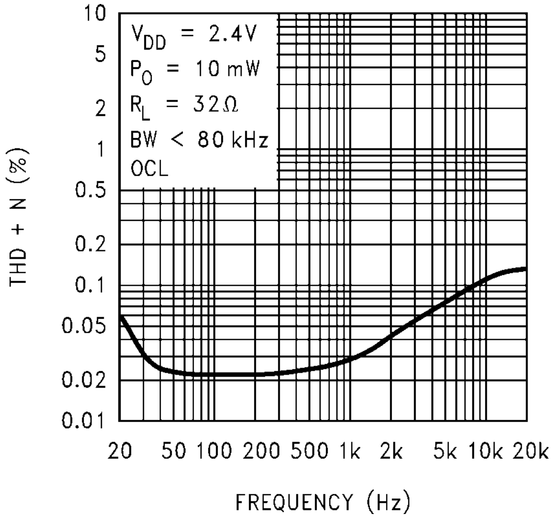
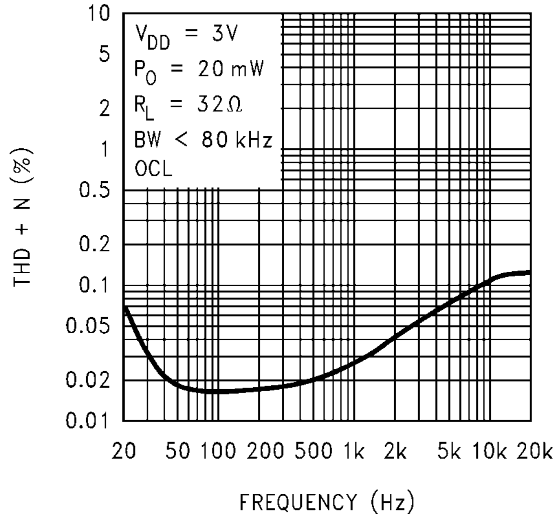
THD+N vs Frequency



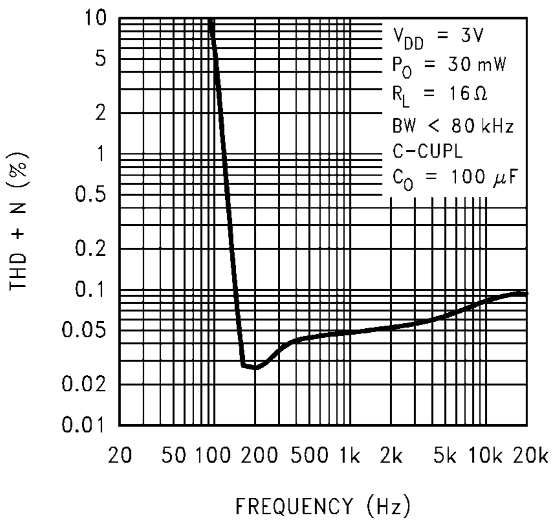
30135005

THD+N vs Frequency



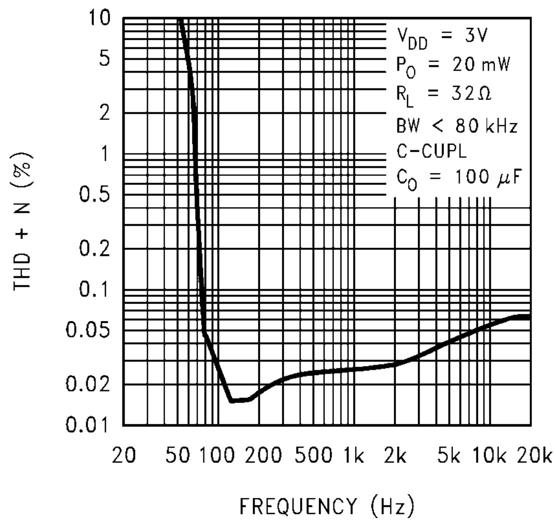
30135004

THD+N vs Frequency



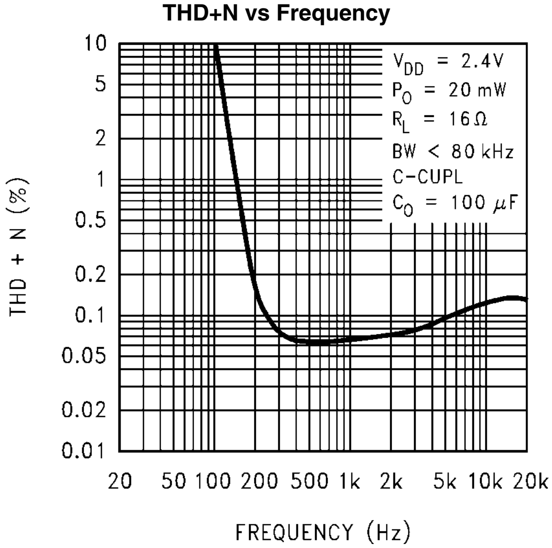
30135086

THD+N vs Frequency



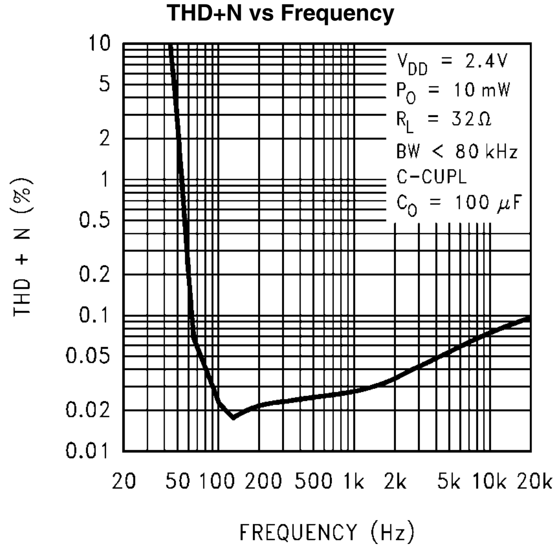
30135087

THD+N vs Frequency



30135088

THD+N vs Frequency



30135089

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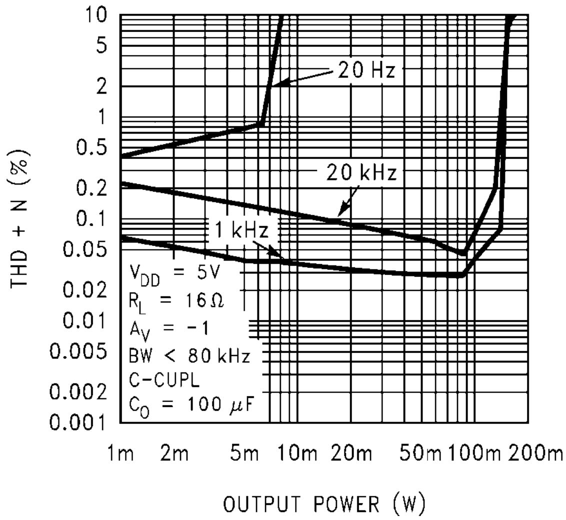
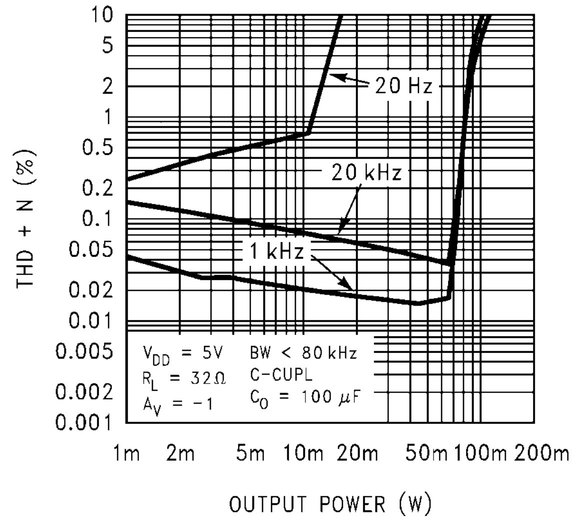
THD+N vs Output Power



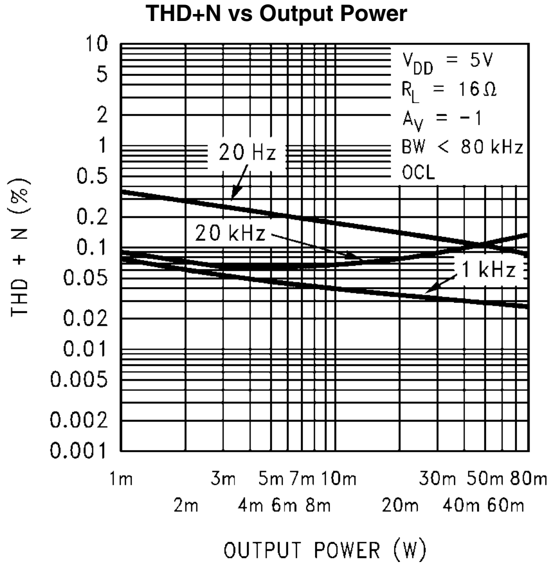
30135090

THD+N vs Output Power



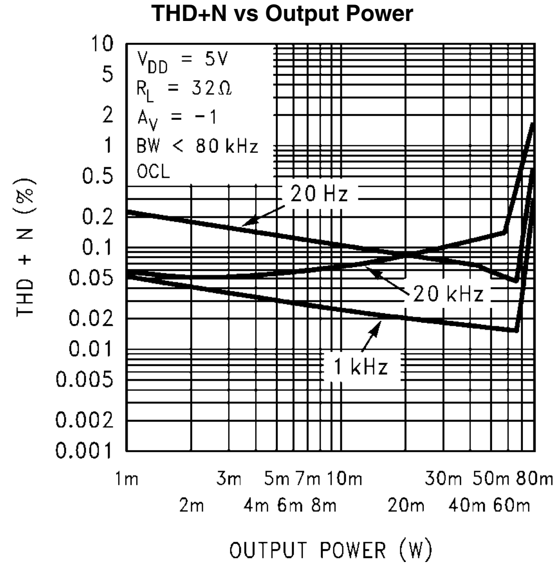
30135091

THD+N vs Output Power



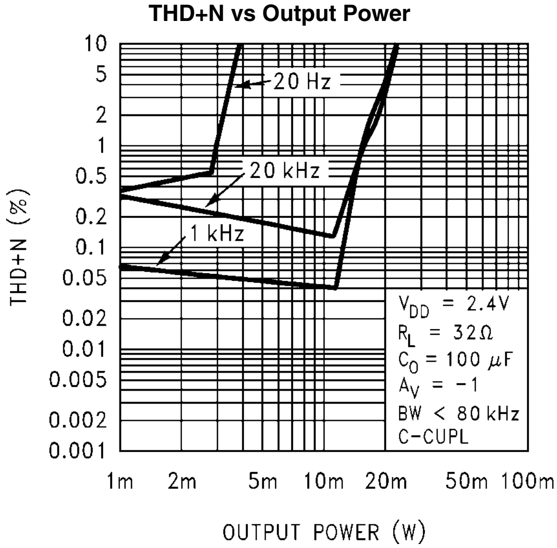
30135092

THD+N vs Output Power



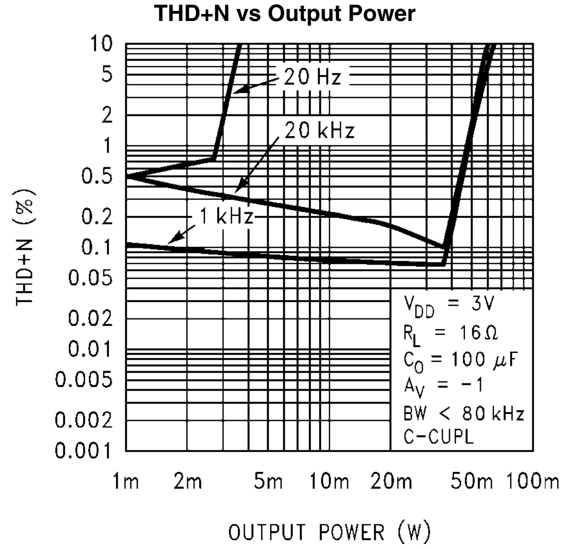
30135093

THD+N vs Output Power



30135008

THD+N vs Output Power



30135007

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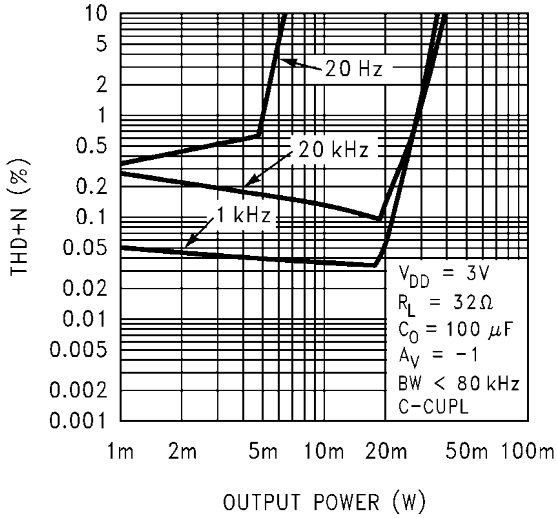
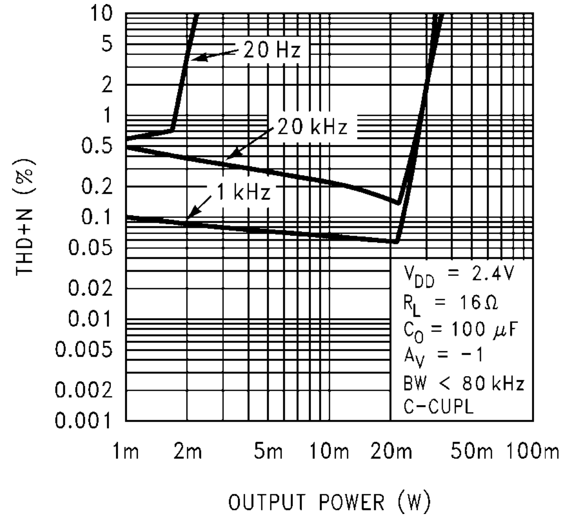
THD+N vs Output Power



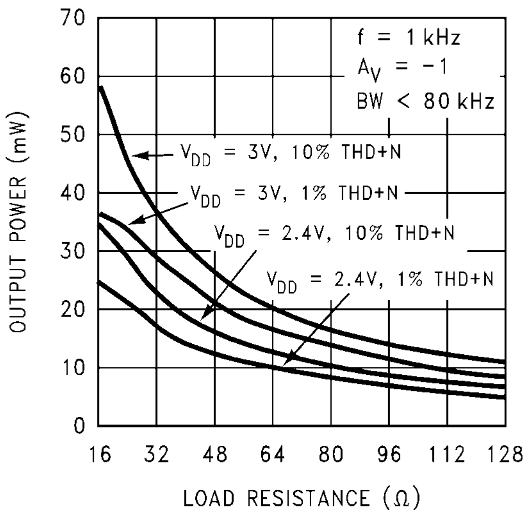
30135010

THD+N vs Output Power



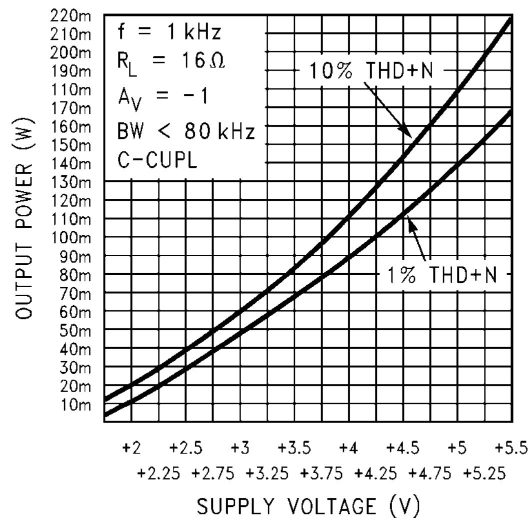
30135009

Output Resistance vs Load Resistance



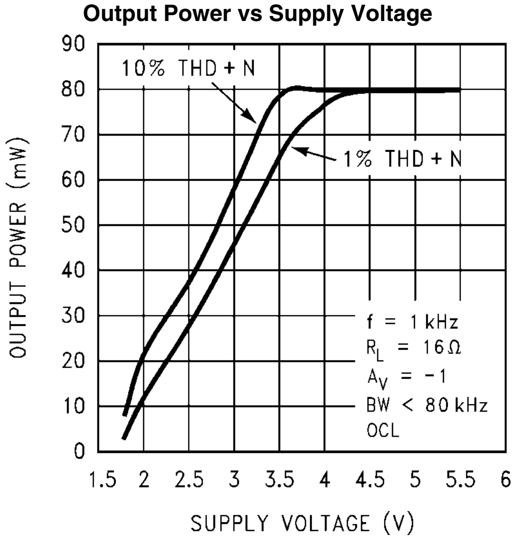
30135013

Output Power vs Supply Voltage



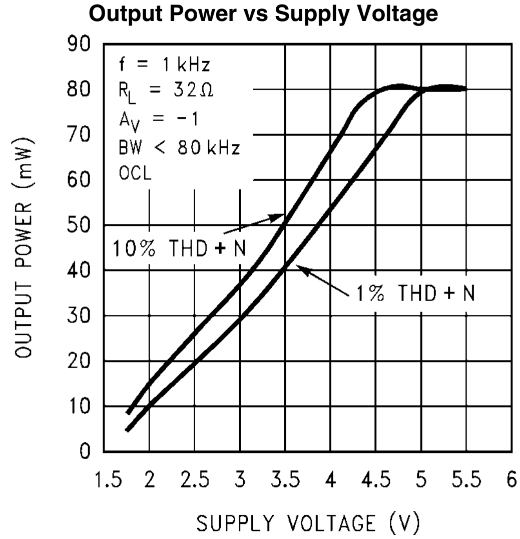
30135012

Output Power vs Supply Voltage



30135094

Output Power vs Supply Voltage



30135095

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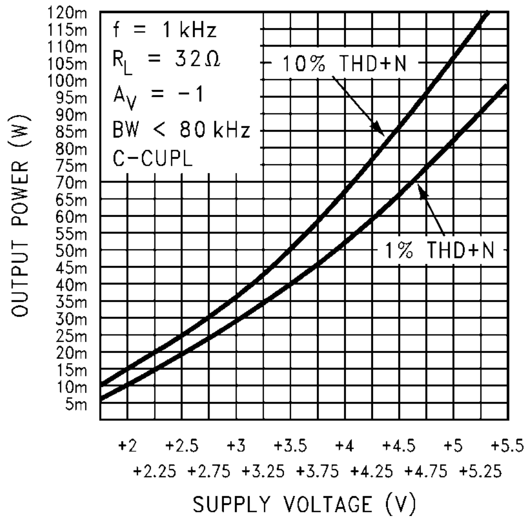
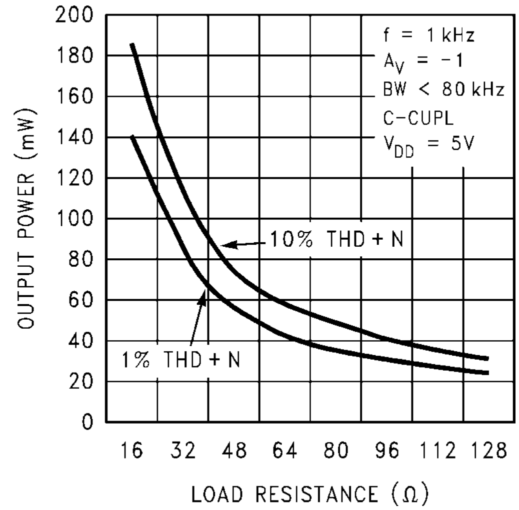
Output Power vs Supply Voltage



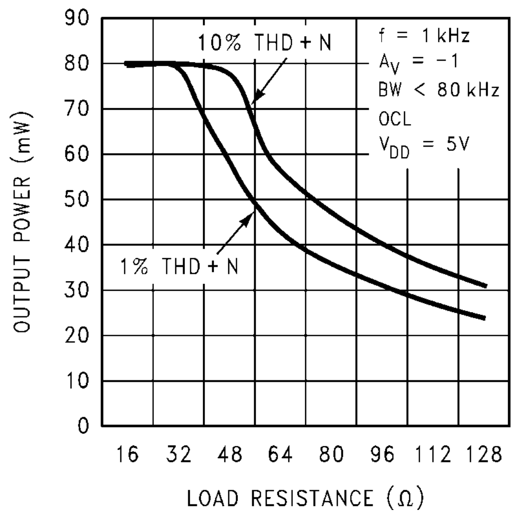
30135011

Output Power vs Load Resistance



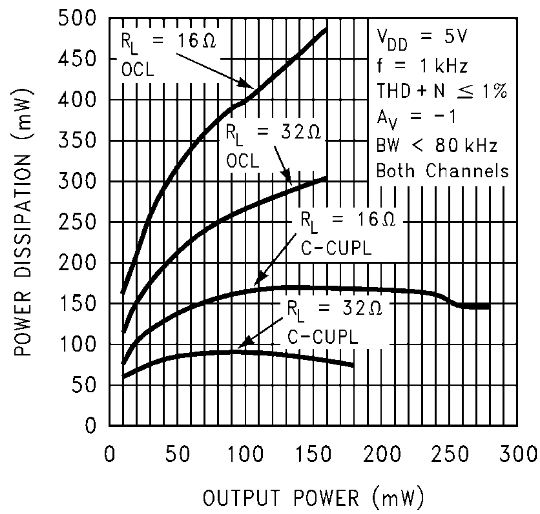
30135096

Output Power vs Load Resistance



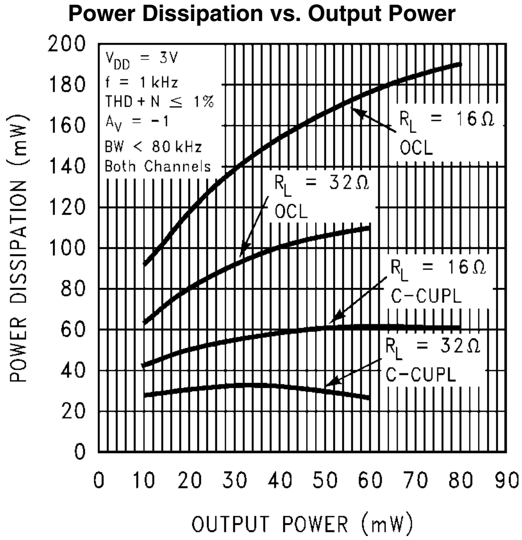
30135097

Power Dissipation vs. Output Power



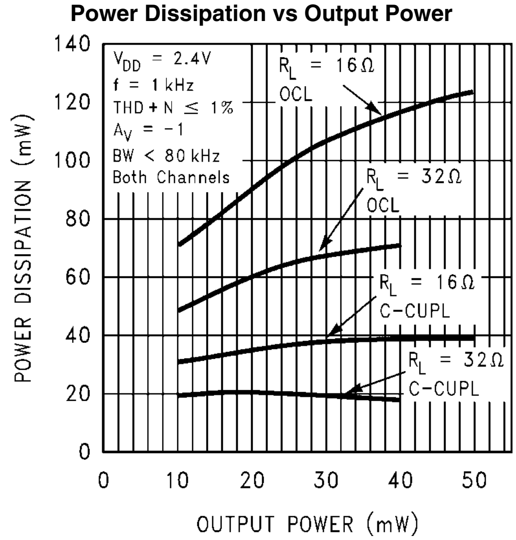
30135098

Power Dissipation vs. Output Power



30135099

Power Dissipation vs Output Power



301350a0

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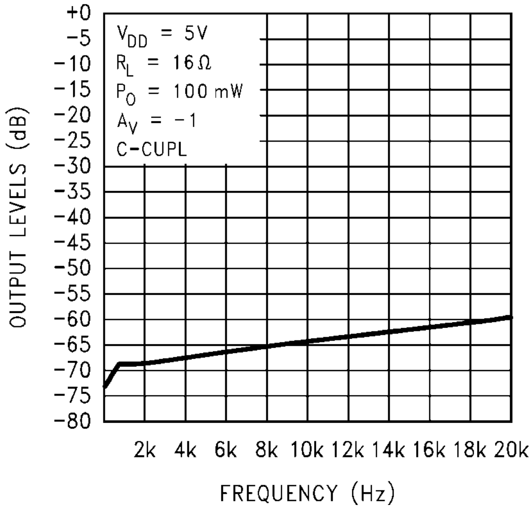
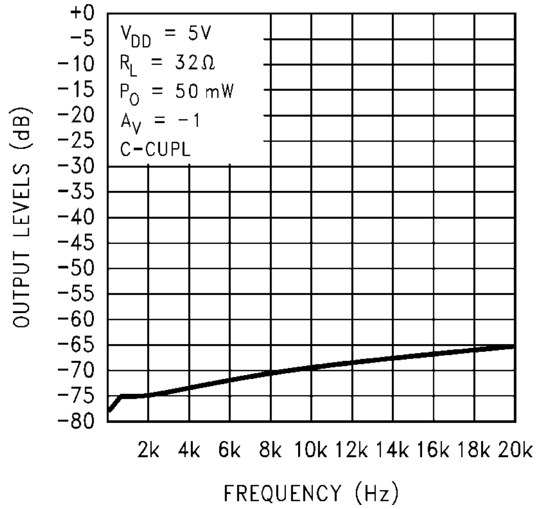
Channel Separation



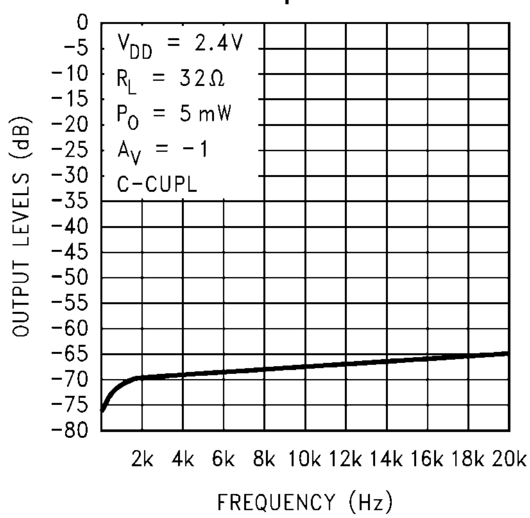
301350a1

Channel Separation



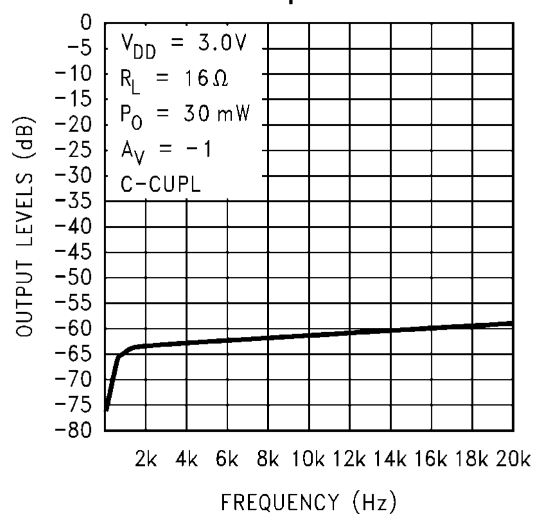
301350a2

Channel Separation



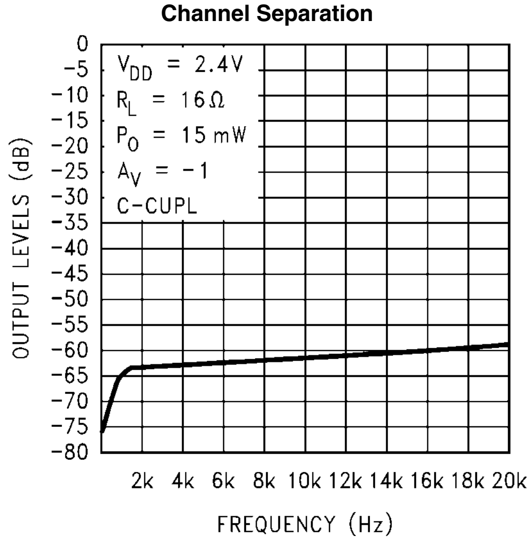
30135017

Channel Separation



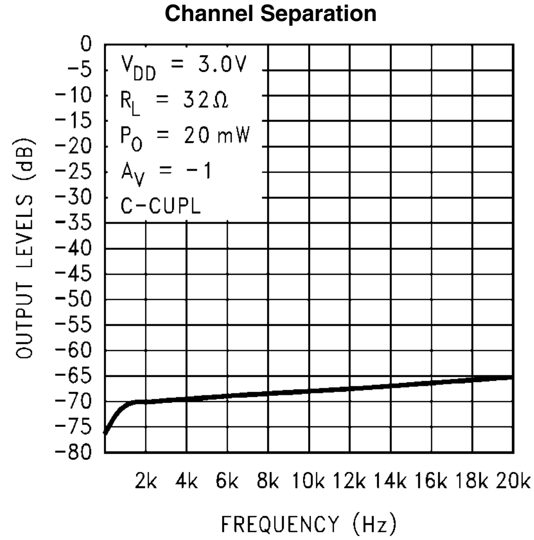
30135019

Channel Separation



30135018

Channel Separation



30135016

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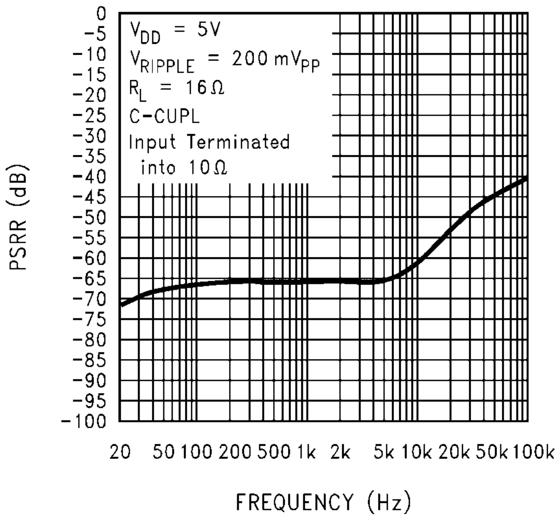
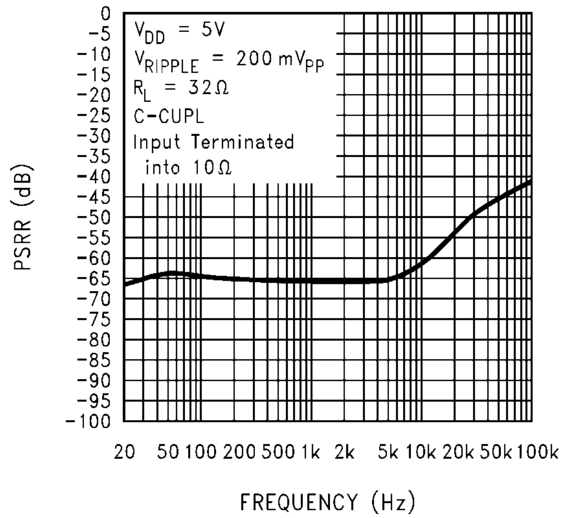
Power Supply Rejection Ratio



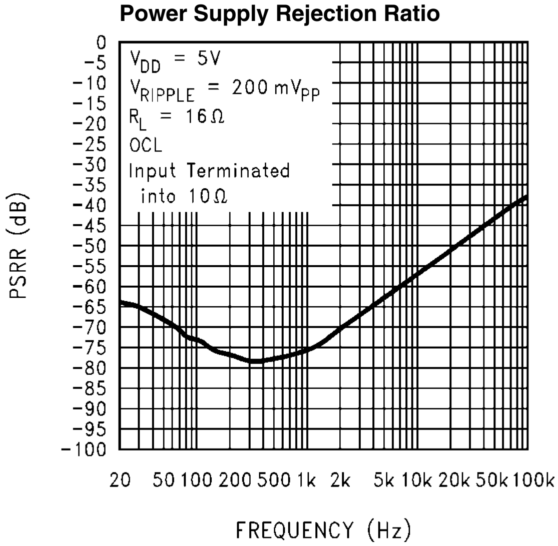
301350a3

Power Supply Rejection Ratio



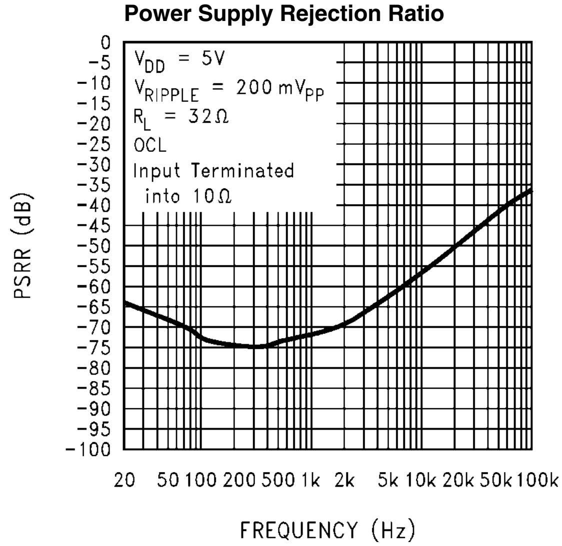
301350a4

Power Supply Rejection Ratio



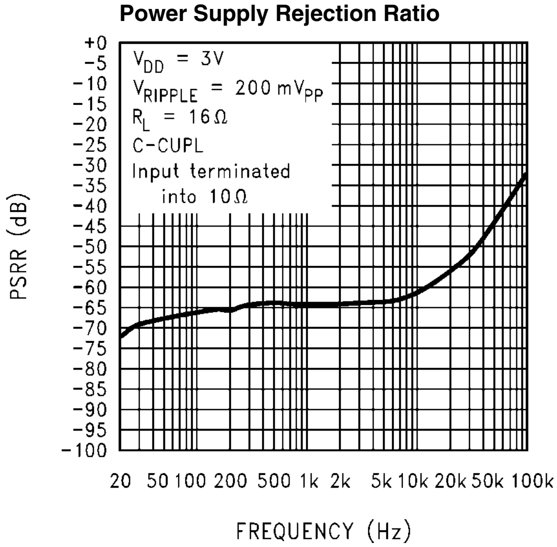
301350a5

Power Supply Rejection Ratio



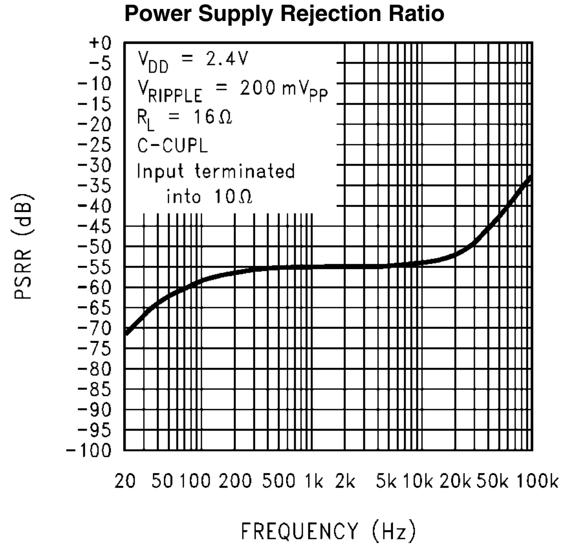
301350a6

Power Supply Rejection Ratio



30135020

Power Supply Rejection Ratio



30135023

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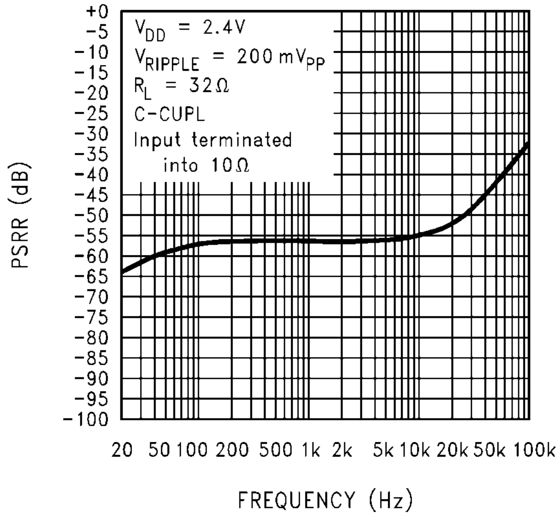
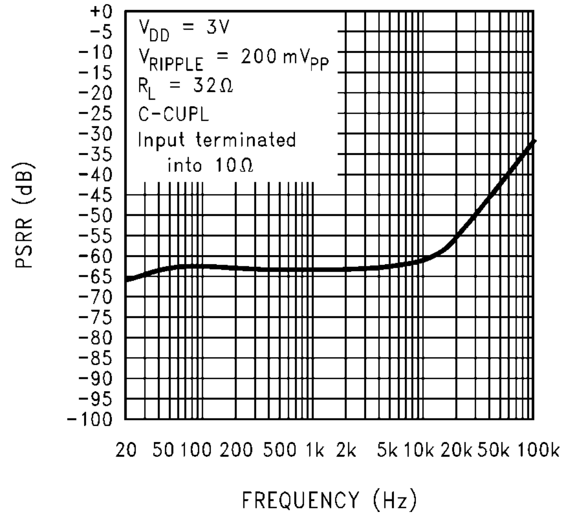
Power Supply Rejection Ratio



30135021

Power Supply Rejection Ratio



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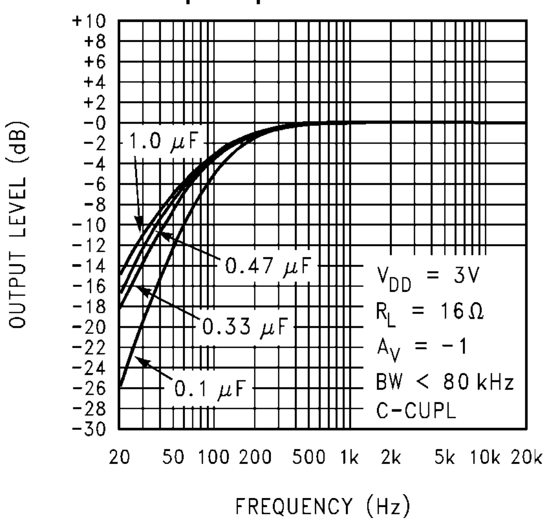
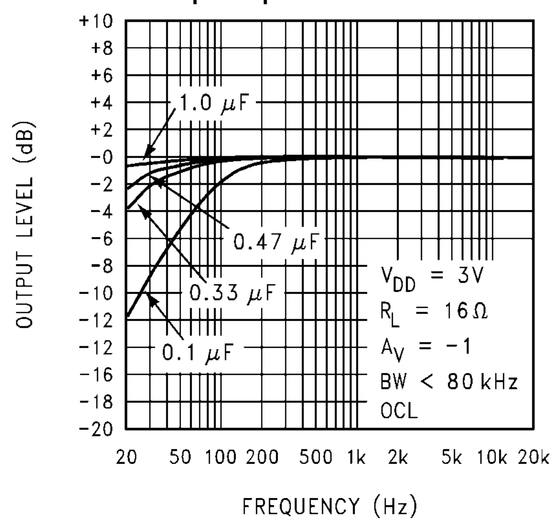
Frequency Response vs Input Capacitor Size



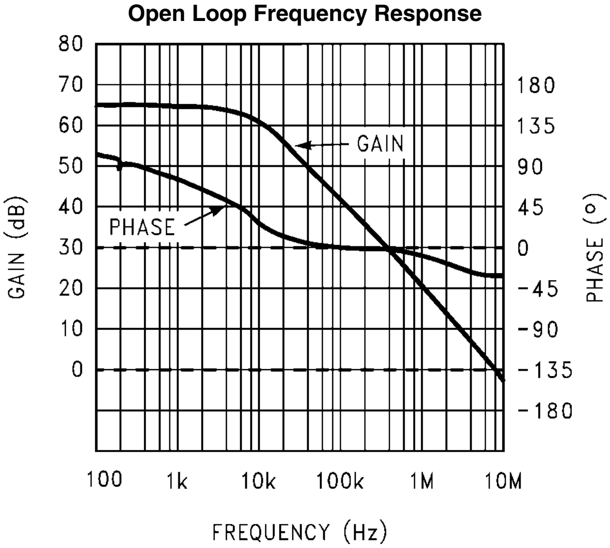
30135027

Frequency Response vs Input Capacitor Size



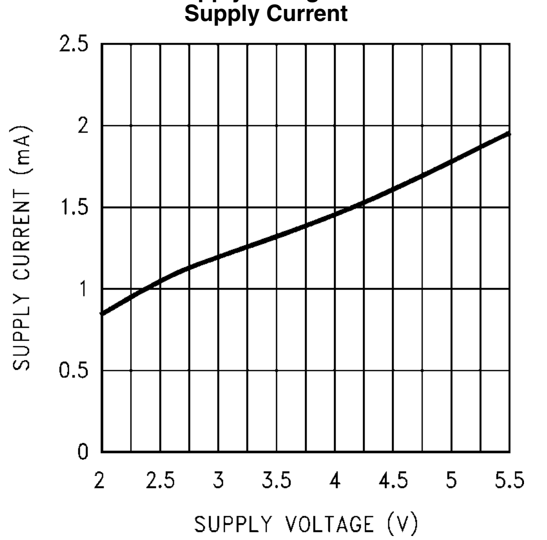
30135026

Open Loop Frequency Response



301350a7

Supply Voltage vs Supply Current



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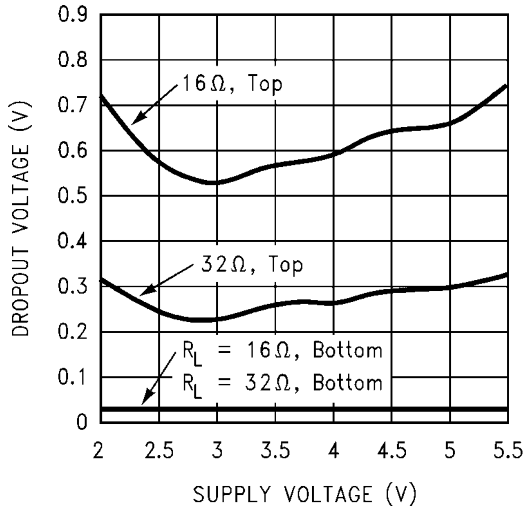
Clipping Voltage vs Supply Voltage



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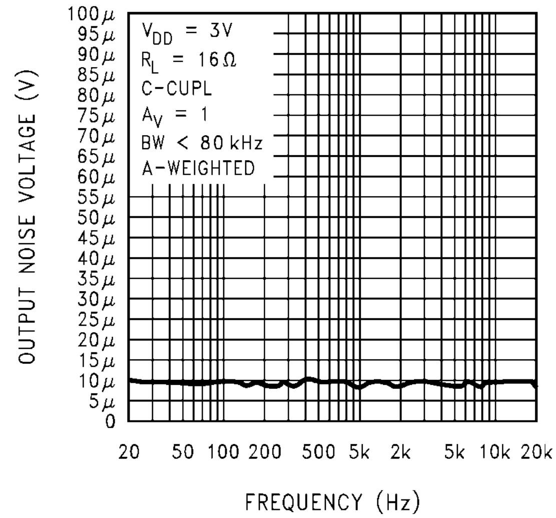
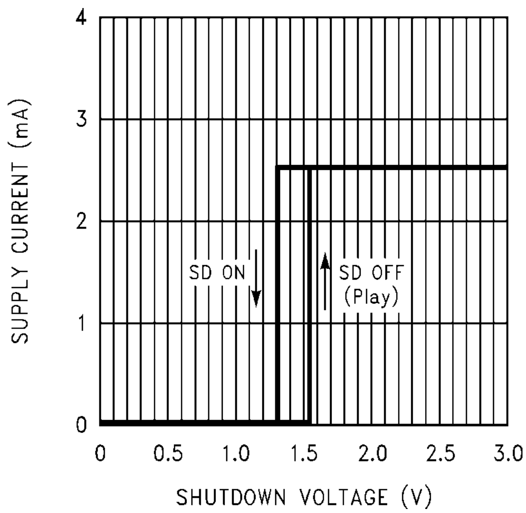
Noise Floor



301350a8

Shutdown Hysteresis Voltage, Vdd=5V



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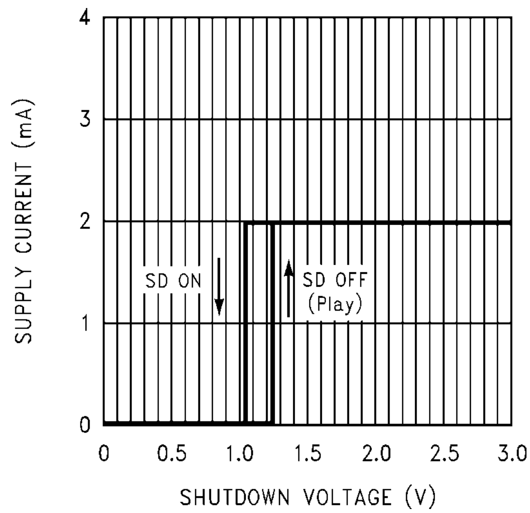
Shutdown Hysteresis Voltage, Vdd=3V



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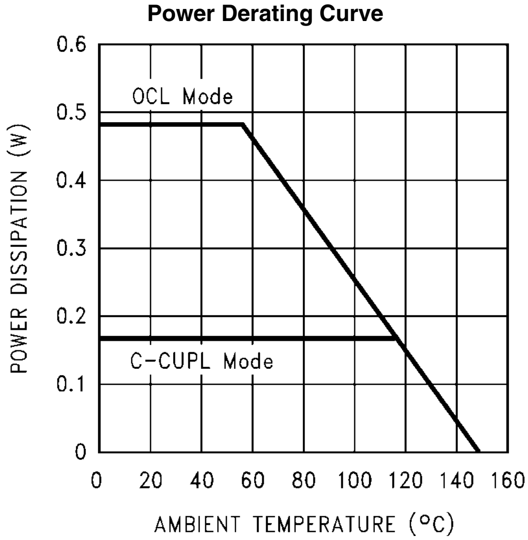
Power Derating Curve



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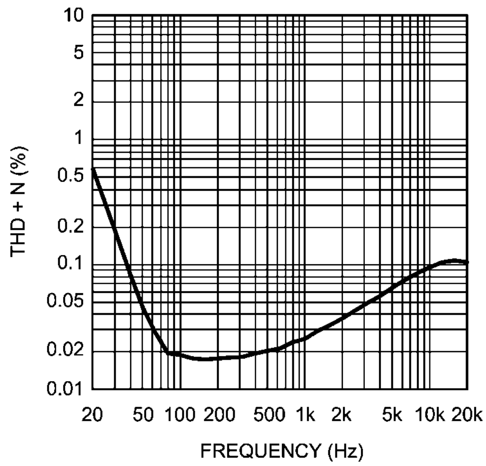
Typical Performance Characteristics

LM4911QMM Specific Characteristics (Note 10)

THD+N vs Frequency at V_{DD} = 5V, R_L = 16Ω P_O = 100mW, OCL



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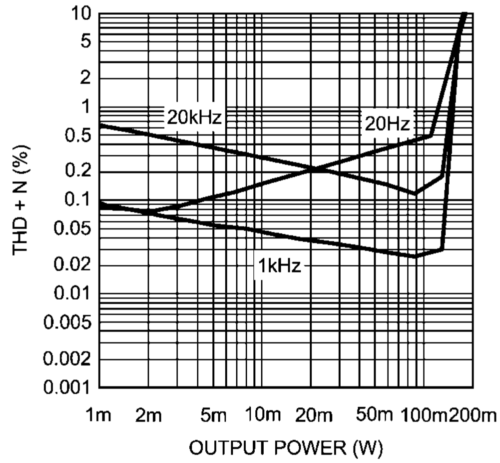
THD+N vs Output Power at V_{DD} = 5V, R_L = 16Ω, OCL



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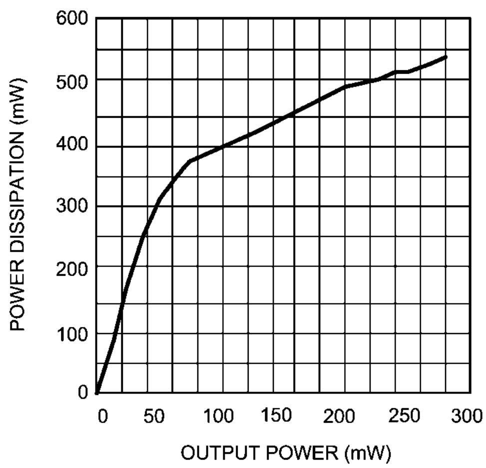
Power Dissipation vs Output Power at V_{DD} = 5V, R_L = 16Ω THD+N ≤ 1%, OCL



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Application Information

AMPLIFIER CONFIGURATION EXPLANATION

As shown in *Figure 1*, the LM4911QMM has three operational amplifiers internally. Two of the amplifier's have externally configurable gain while the other amplifier is internally fixed at the bias point acting as a unity-gain buffer. The closed-loop gain of the two configurable amplifiers is set by selecting the ratio of R_f to R_i. Consequently, the gain for each channel of the IC is

$$A_{VD} = -(R_f / R_i)$$

By driving the loads through outputs V_oA and V_oB with V_oC acting as a buffered bias voltage the LM4911QMM does not require output coupling capacitors. The classical single-ended amplifier configuration where one side of the load is connected to ground requires large, expensive output coupling capacitors.

A configuration such as the one used in the LM4911QMM has a major advantage over single supply, single-ended amplifiers. Since the outputs V_oA, V_oB, and V_oC are all biased at 1/2 V_{DD}, no net DC voltage exists across each load. This eliminates the need for output coupling capacitors which are required in a single-supply, single-ended amplifier configuration. Without output coupling capacitors in a typical single-supply, single-ended amplifier, the bias voltage is placed across the load resulting in both increased internal IC power dissipation and possible loudspeaker damage.

OUTPUT CAPACITOR vs. CAPACITOR COUPLED

The LM4911QMM is an stereo audio power amplifier capable of operating in two distinct output modes: capacitor coupled (C-CUPL) or output capacitor-less (OCL). The LM4911QMM may be run in capacitor coupled mode by using a coupling capacitor on each single-ended output (V_oA and V_oB) and connecting V_oC to ground. This output coupling capacitor blocks the half supply voltage to which the output amplifiers are typically biased and couples the audio signal to the headphones or other single-ended (SE) load. The signal return to circuit ground is through the headphone jack's sleeve.

The LM4911QMM can also eliminate these output coupling capacitors by running in OCL mode. Unless shorted to ground, VoC is internally configured to apply a ½ V_{DD} bias voltage to a stereo headphone jack's sleeve. This voltage matches the bias voltage present on V_oA and V_oB outputs that drive the headphones. The headphones operate in a manner similar to a bridge-tied load (BTL). Because the same DC voltage is applied to both headphone speaker terminals this results in no net DC current flow through the speaker. AC current flows through a headphone speaker as an audio signal's output amplitude increases on the speaker's terminal.

The headphone jack's sleeve is not connected to circuit ground when used in OCL mode. Using the headphone output jack as a line-level output will place the LM4911QMM's ½ V_{DD} bias voltage on a plug's sleeve connection. This presents no difficulty when the external equipment uses capacitively coupled inputs. For the very small minority of equipment that is DC coupled, the LM4911QMM monitors the current supplied by the amplifier that drives the headphone jack's sleeve. If this current exceeds $500mA_{PK}$, the amplifier is shutdown, protecting the LM4911QMM and the external equipment.

MODE SELECT DETAIL

The LM4911QMM may be set up to operate in one of two modes: OCL and cap-coupled. The default state of the LM4911QMM at power up is cap-coupled. During initial power up or return from shutdown, the LM4911QMM must detect the correct mode of operation (OCL or cap-coupled) by sensing the status of the V_OC pin. When the bias voltage of the part ramps up to 60mV (as seen on the Bypass pin), an internal comparator detects the status of V_OC; and at 80mV, latches that value in place. Ramp up of the bias voltage will proceed at a different rate from this point on depending upon operating mode. OCL mode will ramp up about 11 times faster than cap-coupled. Shutdown is not a valid command during this time period (T_{WU}) and should not enabled to ensure a proper power on reset (POR) signal. In addition, the slew rate of V_{DD} must be greater than 2.5V/ms to ensure reliable POR. Recommended power up timing is shown in *Figure 5* along with proper usage of Shutdown and Mute. The mode select circuit is suspended during C_B discharge time.

The circuit shown in *Figure 4* presents an applications solution to the problem of using different supply voltages with different turn-on times in a system with the LM4911QMM. This circuit shows the LM4911QMM with a 25-50kΩ pull-up resistor connected from the shutdown pin to V_{DD}. The shutdown pin of the LM4911QMM is also being driven by an open drain output of an external microcontroller on a separate supply. This circuit ensures that shutdown is disabled when powering up the LM4911QMM by either allowing shutdown to be high before the LM4911QMM powers on (the microcontroller powers up first) or allows shutdown to ramp up with V_{DD} (the LM4911QMM powers up first). This will ensure the LM4911QMM powers up properly and enters the correct mode of operation (cap-coupled or OCL).

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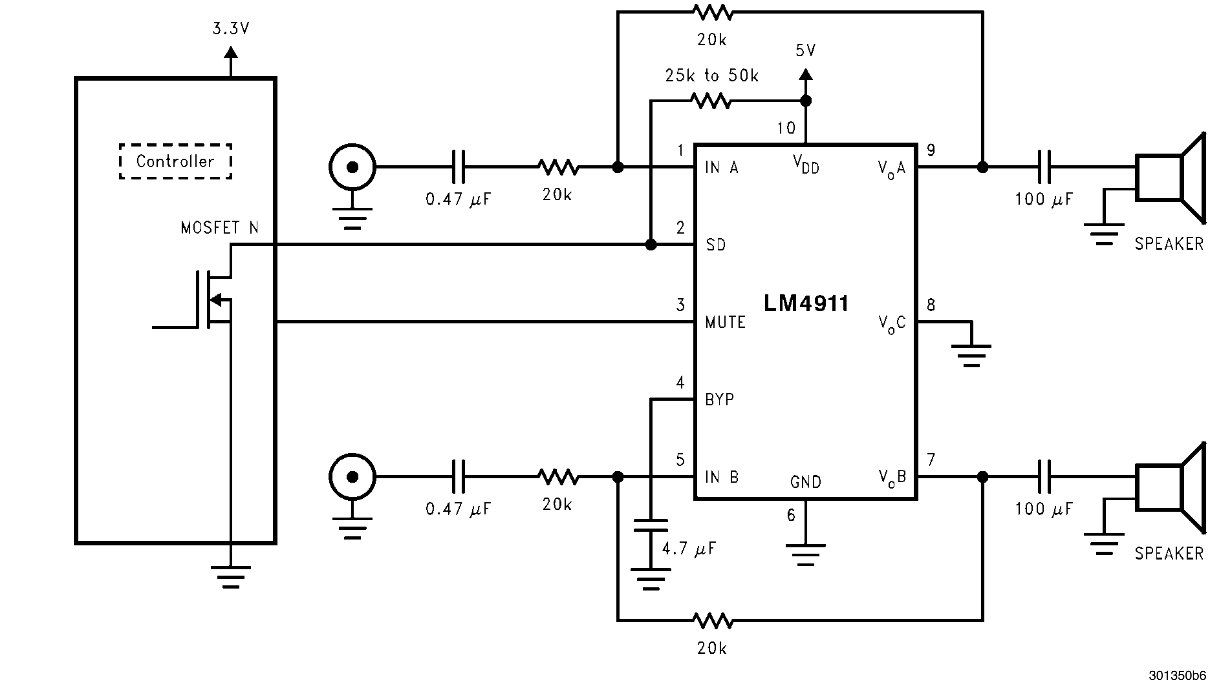

FIGURE 4. Recommended Circuit for Different Supply Turn-On Timing

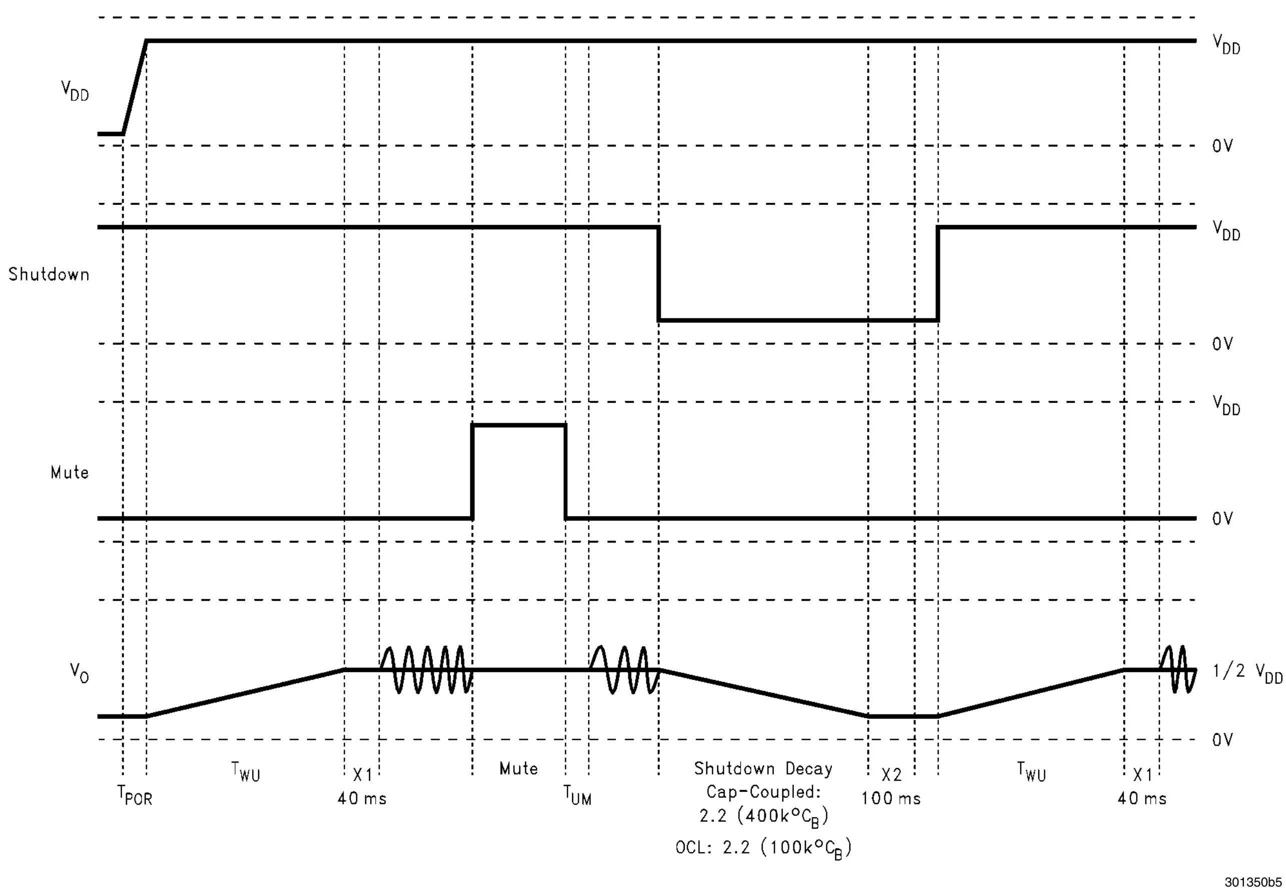

FIGURE 5. Turn-On, Shutdown, and Mute Timing for Cap-Coupled Mode

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POWER DISSIPATION

Power dissipation is a major concern when using any power amplifier and must be thoroughly understood to ensure a successful design. When operating in capacitor-coupled mode, Equation 1 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2 / (2\pi^2 R_L) \quad (1)$$

Since the LM4911QMM has two operational amplifiers in one package, the maximum internal power dissipation point is twice that of the number which results from Equation 1. From Equation 1, assuming a 3V power supply and an 32Ω load, the maximum power dissipation point is 14mW per amplifier. Thus the maximum package dissipation point is 28mW.

When operating in OCL mode, the maximum power dissipation increases due to the use of the third amplifier as a buffer and is given in Equation 2:

$$P_{DMAX} = 4(V_{DD})^2 / (\pi^2 R_L) \quad (2)$$

The maximum power dissipation point obtained from either Equation 1 or 2 must not be greater than the power dissipation that results from Equation 3:

$$P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA} \quad (3)$$

For package MUB10A, θ_{JA} = 190°C/W; for package LDA10A, θ_{JA} = 63°C/W. T_{JMAX} = 150°C for the LM4911QMM. Depending on the ambient temperature, T_A, of the system surroundings, Equation 3 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 1 or 2 is greater than that of Equation 3, then either the supply voltage must be decreased, the load impedance increased or T_A reduced. For the typical application of a 3V power supply, with a 32Ω load, the maximum ambient temperature possible without violating the maximum junction temperature is approximately 144°C provided that device operation is around the maximum power dissipation point. Thus, for typical applications, power dissipation is not an issue. Power dissipation is a function of output power and thus, if typical operation is not around the maximum power dissipation point, the ambient temperature may be increased accordingly. Refer to the Typical Performance Characteristics curves for power dissipation information for lower output powers.

EXPOSED-DAP PACKAGE PCB MOUNTING CONSIDERATIONS

The LM4911QMM's exposed-DAP (die attach paddle) package (LD) provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane, and surrounding air.

The LD package should have its DAP soldered to a copper pad on the PCB. The DAP's PCB copper pad may be connected to a large plane of continuous unbroken copper. This plane forms a thermal mass, heat sink, and radiation area. Further detailed and specific information concerning PCB layout, fabrication, and mounting an LD (LLP) package is available from National Semiconductor's Package Engineering Group under application note AN1187.

POWER SUPPLY BYPASSING

As with any amplifier, proper supply bypassing is important for low noise performance and high power supply rejection. The capacitor location on the power supply pins should be as close to the device as possible.

Typical applications employ a 3V regulator with 10mF tantalum or electrolytic capacitor and a ceramic bypass capacitor which aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the LM4911QMM. A bypass capacitor value in the range of 0.1µF to 1µF is recommended for C_S.

MICRO POWER SHUTDOWN

The voltage applied to the SHUTDOWN pin controls the LM4911QMM's shutdown function. Activate micro-power shutdown by applying a logic-low voltage to the SHUTDOWN pin. When active, the LM4911QMM's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. The trigger point varies depending on supply voltage and is shown in the Shutdown Hysteresis Voltage graphs in the Typical Performance Characteristics section. The low 0.1µA(typ) shutdown current is achieved by applying a voltage that is as near as ground as possible to the SHUTDOWN pin. A voltage that is higher than ground may increase the shutdown current. There are a few ways to control the micro-power shutdown. These include using a single-pole, single-throw switch, a microprocessor, or a microcontroller. When using a switch, connect an external 100kΩ pull-up resistor between the SHUTDOWN pin and V_{DD}. Connect the switch between the SHUTDOWN pin and ground. Select normal amplifier operation by opening the switch. Closing the switch connects the SHUTDOWN pin to ground, activating micro-power shutdown.

The switch and resistor guarantee that the SHUTDOWN pin will not float. This prevents unwanted state changes. In a system with a microprocessor or microcontroller, use a digital output to apply the control voltage to the SHUTDOWN pin. Driving the SHUTDOWN pin with active circuitry eliminates the pull-up resistor.

Shutdown enable/disable times are controlled by a combination of C_B and V_{DD}. Larger values of C_B results in longer turn on/off times from Shutdown. Smaller V_{DD} values also increase turn on/off time for a given value of C_B. Longer shutdown times also improve the LM4911QMM's resistance to click and pop upon entering or returning from shutdown. For a 2.4V supply and C_B = 4.7µF, the LM4911QMM requires about 2 seconds to enter or return from shutdown. This longer shutdown time enables the LM4911QMM to have virtually zero pop and click transients upon entering or release from shutdown.

Smaller values of C_B will decrease turn-on time, but at the cost of increased pop and click and reduced PSRR. Since shutdown enable/disable times increase dramatically as supply voltage gets below 2.2V, this reduced turn-on time may be desirable if extreme low supply voltage levels are used as this would offset increases in turn-on time caused by the lower supply voltage. This technique is not recommended for OCL mode since shutdown enable/disable times are very fast (0.5s) independent of supply voltage.

When in cap-coupled mode, some restrictions on the usage of Mute are in effect when entering or returning from shutdown. These restrictions require Mute not be toggled immediately following a return or entrance to shutdown for a brief

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period. These periods are shown as X1 and X2 and are discussed in greater detail in the **Mute** section as well as shown in *Figure 5*.

MUTE

When in C-CUPL mode, the LM4911QMM also features a mute function that enables extremely fast turn-on/turn-off with a minimum of output pop and click with a low current consumption (≤ 100µA). The mute function leaves the outputs at their bias level, thus resulting in higher power consumption than shutdown mode, but also provides much faster turn on/ off times. Mute mode is enabled by providing a logic high signal on the MUTE pin in the opposite manner as the shutdown function described above. Threshold voltages and activation techniques match those given for the shutdown function as well.

Mute may not appear to function when the LM4911QMM is used to drive high impedance loads. This is because the LM4911QMM relies on a typical headphone load (16-32Ω) to reduce input signal feedthrough through the input and feedback resistors. Mute attenuation can thus be calculated by the following formula:

$$\text{Mute Attenuation (dB)} = 20\text{Log}(R_L \,/\, (R_i+R_F))$$

Parallel load resistance may be necessary to achieve satisfactory Mute levels when the application load is known to be high impedance.

The mute function is not necessary when the LM4911QMM is operating in OCL mode since the shutdown function operates quickly in OCL mode with less power consumption than mute.

Mute may be enabled during shutdown transitions, but should not be toggled for a brief period immediately after exiting or entering shutdown. These brief time periods are labeled X1 (time after returning from shutdown) and X2 (time after entering shutdown) and are shown in the timing diagram given in *Figure 5*. X1 occurs immediately following a return from shutdown (T_{WU}) and lasts 40ms±25%. X2 occurs after the part is placed in shutdown and the decay of the bias voltage has occurred ($2.2*400k*C_B$ for cap-coupled and $2.2*100k*C_B$ for OCL) and lasts for 100ms±25%. The timing of these transition periods relative to X1 and X2 is also shown in *Figure 5*. Mute should not be toggled during these time periods, but may be made during the shutdown transitions or any other time the part is in normal operation (while in cap-coupled mode - Mute is not valid in OCL mode). Failure to operate mute correctly may result in much higher click and pop values or failure of the device to mute at all.

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical to optimize device and system performance. While the LM4911QMM is tolerant of external component combinations, consideration to component values must be used to maximize overall system quality.

The LM4911QMM is unity-gain stable which gives the designer maximum system flexibility. The LM4911QMM should be used in low gain configurations to minimize THD+N values, and maximize the signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than $1V_{rms}$ are available from sources such as audio codecs. Very large values should not be used for the gain-setting resistors. Values for R_i and R_f should be less than 1MΩ. Please refer to the section, **Audio Power Amplifier Design**, for a more complete explanation of proper gain selection

Besides gain, one of the major considerations is the closed-loop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in *Figure 2* and *Figure 3*. The input coupling capacitor, C_i, forms a first order high pass filter which limits low frequency response. This value should be chosen based on needed frequency response and turn-on time.

SELECTION OF INPUT CAPACITOR SIZE

Amplifying the lowest audio frequencies requires a high value input coupling capacitor, C_i. A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the headphones used in portable systems have little ability to reproduce signals below 60Hz. Applications using headphones with this limited frequency response reap little improvement by using a high value input capacitor.

In addition to system cost and size, turn on time is affected by the size of the input coupling capacitor C_i. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage. This charge comes from the output via the feedback Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on time can be minimized. A small value of C_i (in the range of 0.1µF to 0.39µF), is recommended.

AUDIO POWER AMPLIFIER DESIGN

A 25mW/32Ω AUDIO AMPLIFIER

Given:	
Power Output	25mWrms
Load Impedance	32Ω
Input Level	1Vrms
Input Impedance	20kΩ

A designer must first determine the minimum supply rail to obtain the specified output power. By extrapolating from the Output Power vs Supply Voltage graphs in the **Typical Performance Characteristics** section, the supply rail can be easily found.

3V is a standard voltage in most applications, it is chosen for the supply rail. Extra supply voltage creates headroom that allows the LM4911QMM to reproduce peak in excess of 25mW without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the **Power Dissipation** section.

Once the power dissipation equations have been addressed, the required gain can be determined from Equation 2.

$$A_V \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (4)$$

From Equation 4, the minimum A_V is 0.89; use A_V = 1. Since the desired input impedance is 20kΩ, and with a A_V gain of 1, a ratio of 1:1 results from Equation 1 for R_f to R_i. The values are chosen with R_i = 20kΩ and R_f = 20kΩ. The final design step is to address the bandwidth requirements which must be stated as a pair of -3dB frequency points. Five times away from a -3dB point is 0.17dB down from passband response which is better than the required ± 0.25dB specified.

f_L = 100Hz/5 = 20Hz

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f_H = 20kHz * 5 = 100kHz

As stated in the **External Components** section, R_i in conjunction with C_i creates a

$C_i \geq 1 / (2\pi * 20k\Omega * 20Hz) = 0.397\mu F$; use 0.39μF.

The high frequency pole is determined by the product of the desired frequency pole, f_H, and the differential gain, A_V. With an A_V = 1 and f_H = 100kHz, the resulting GBWP = 100kHz which is much smaller than the LM4911QMM GBWP of 10MHz. This figure displays that is a designer has a need to design an amplifier with higher differential gain, the LM4911QMM can still be used without running into bandwidth limitations.

Figure 4 shows an optional resistor connected between the amplifier output that drives the headphone jack sleeve and ground. This resistor provides a ground path that supressed power supply hum. Thishum may occur in applications such as notebook computers in a shutdown condition and connected to an external powered speaker. The resistor's 100Ω value is a suggested starting point. Its final value must be determined based on the tradeoff between the amount of noise suppression that may be needed and minimizing the additional current drawn by the resistor (25mA for a 100Ω resistor and a 5V supply).

ESD PROTECTION

As stated in the Absolute Maximum Ratings, the LM4911QMM has a maximum ESD susceptibility rating of 2000V. For higher ESD voltages, the addition of a PCDN042 dual transil (from California Micro Devices), as shown in *Figure 6*, will provide additional protection.

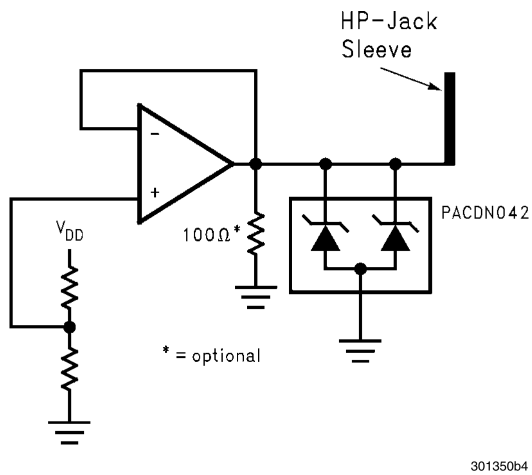

FIGURE 6. The PCDN042 provides additional ESD protection beyond the 2000V shown in the Absolute Maximum Ratings for the V_OC output

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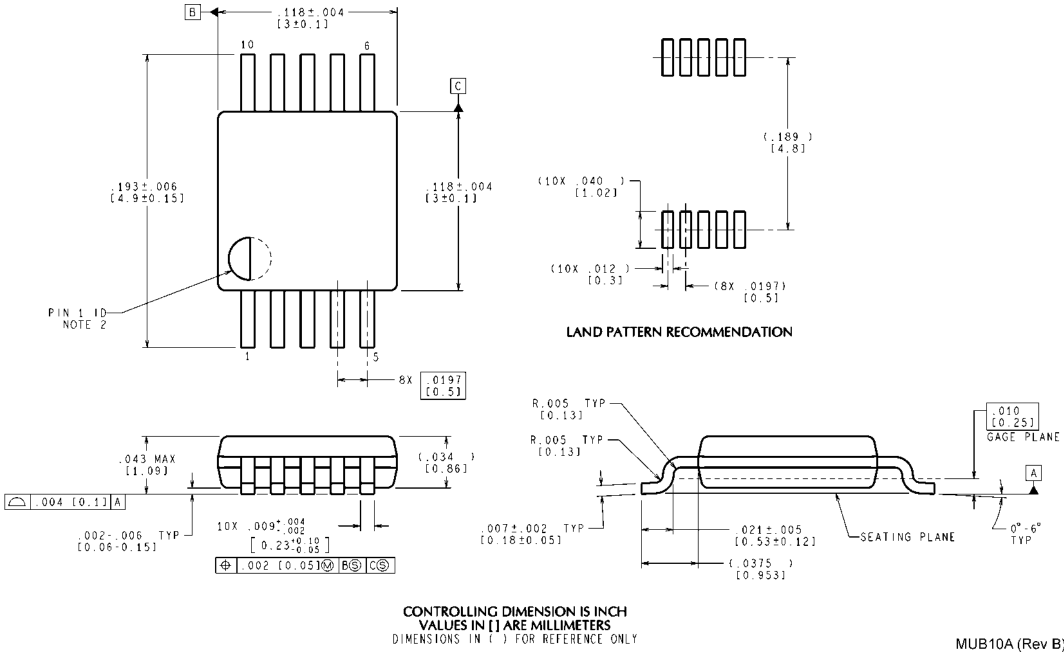
Physical Dimensions inches (millimeters) unless otherwise noted



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LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
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PowerWise® Solutions	www.national.com/powerwise	Applications & Markets	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
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