National Semiconductor

LH2101A/LH2201A/LH2301A
Dual High Performance Operational Amplifiers

General Description

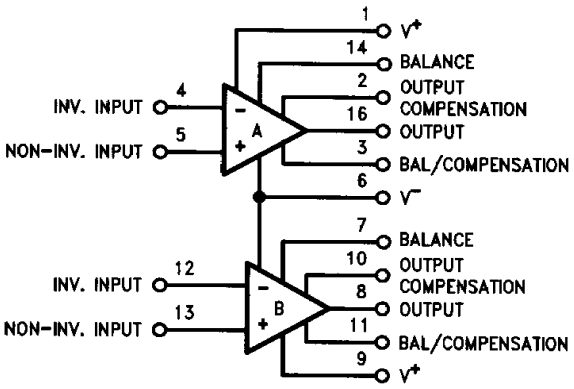
The LH2101A series of dual operational amplifiers are two LM101A type op amps in a single hermetic package. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, reduced insertion cost, and smaller size than two singles. For additional information, see the LM101A data sheet and National's Linear Application Handbook.

The LH2101A is specified for operation over the −55°C to +125°C military temperature range. The LH2201A is specified for operation over the −25°C to +85°C temperature range. The LH2301A is specified for operation over the 0°C to +70°C temperature range.

Features

- Low offset voltage
- Low offset current
- Guaranteed drift characteristics
- Offsets guaranteed over entire common mode and supply voltage ranges
- Slew rate of 10 V/μs as a summing amplifier

Connection Diagram



TL/K/10118–1

Order Number LH2101AD, LH2201AD or LH2301AD
See NS Package Number D16C

3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±22V
Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	
LH2101A	−55°C to +125°C
LH2201A	−25°C to +85°C
LH2301A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 Sec.)	300°C

Electrical Characteristics Each Side (Note 3)

Parameter	Conditions	Limits			Units
		LH2101A	LH2201A	LH2301A	
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 50\ k\Omega$	2.0	2.0	7.5	mV Max
Input Offset Current	$T_A = 25°C$	10	10	50	nA Max
Input Bias Current	$T_A = 25°C$	75	75	250	nA Max
Input Resistance	$T_A = 25°C$	1.5	1.5	0.5	MΩ Min
Supply Current	$T_A = 25°C$, $V_S \pm 20V$	3.0	3.3	3.0	mA Max
Large Signal Voltage Gain	$T_A = 25°C$, $V_S \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$	50	50	25	V/mV Min
Input Offset Voltage	$R_S \leq 50\ k\Omega$	3.0	3.0	10	mV Max
Average Temperature Coefficient of Input Offset Voltage		15	15	30	μV/°C Max
Input Offset Current		20	20	70	nA Max
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 125°C$ $-55°C \leq T_A \leq 25°C$	0.1 0.2	0.1 0.2	0.3 0.6	nA/°C Max
Input Bias Current		100	100	300	nA Max
Supply Curent	$T_A = +125°C$, $V_S = \pm 20V$	2.5	2.5		mA Max
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2\ k\Omega$	25	25	15	V/mV Min
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$ $R_L = 2\ k\Omega$	±12 ±10	±12 ±10	±12 ±10	V Min
Input Voltage Range	$V_S = \pm 20V$	±15	±15	±12	V Min
Common Mode Rejection Ratio	$R_S \leq 50\ k\Omega$	80	80	70	dB Min
Supply Voltage Rejection Ratio	$R_S < 50\ k\Omega$	80	80	70	dB Min

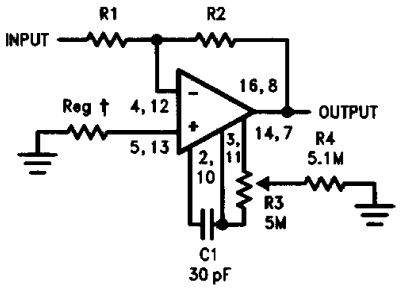
Note 1: The maximum junction temperature of the LH2101A is 150°C, while that of the LH2201A is 100°C. For operating temperatures of devices in the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq +125°C$, unless otherwise specified. With the LH2201A, however, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$. For the LH2301A these specifications apply for $0°C \leq T_A \leq +70°C$, and $\pm 5V \leq V_S \leq +15V$. Supply current and input voltage range are specified as $V_S = \pm 15V$ for the LH2301A. $C_1 = 30$ pF unless otherwise specified.

Auxiliary Circuits

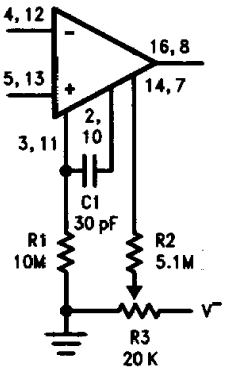
Inverting Amplifier with Balancing Circuit



TL/K/10118–2

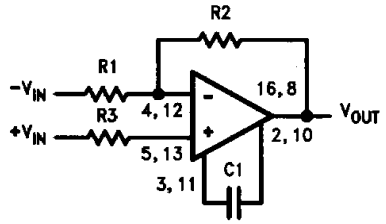
†May be zero or equal to parallel combination of R1 and R2 for minimum offset.

Alternate Balancing Circuit



TL/K/10118–3

Single Pole Compensation

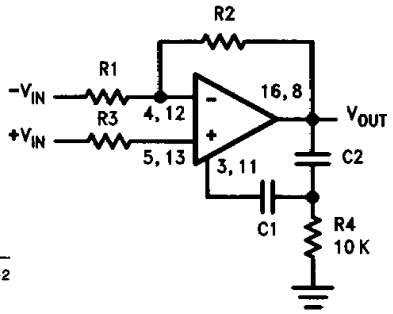


TL/K/10118–4

$C_1 \geq \frac{R_1 C_S}{R_1 + R_2}$

C_S = 30 pF

Two Pole Compensation



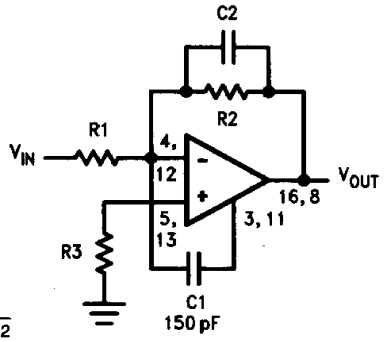
$C_1 \geq \frac{R_1 C_S}{R_1 + R_2}$

C_S = 30 pF

C2 = 10 C1

TL/K/10118–5

Feedforward Compensation



$C2 = \frac{1}{2\pi f_o R2}$

f_o = 3 MHz

TL/K/10118–6