LH231100B NMOS 1M (128K × 8) Mask Programmable ROM

FEATURES

- 131,072 × 8 bit organization
- Access time: 200 ns (MAX.)
- Power consumption:
  Operating: 550 mW (MAX.)
- Mask-programmable $OE_1/\overline{OE}_1/DC$ and $OE_2/\overline{OE}_2/DC$
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Package:
  32-pin, 600-mil DIP
  (32-pin compatible to 28-pin 1M mask ROM specific pinout)

DESCRIPTION

The LH231100B is a mask programmable ROM organized as 131,072 × 8 bits. It is fabricated using silicon-gate NMOS process technology.

PIN CONNECTIONS

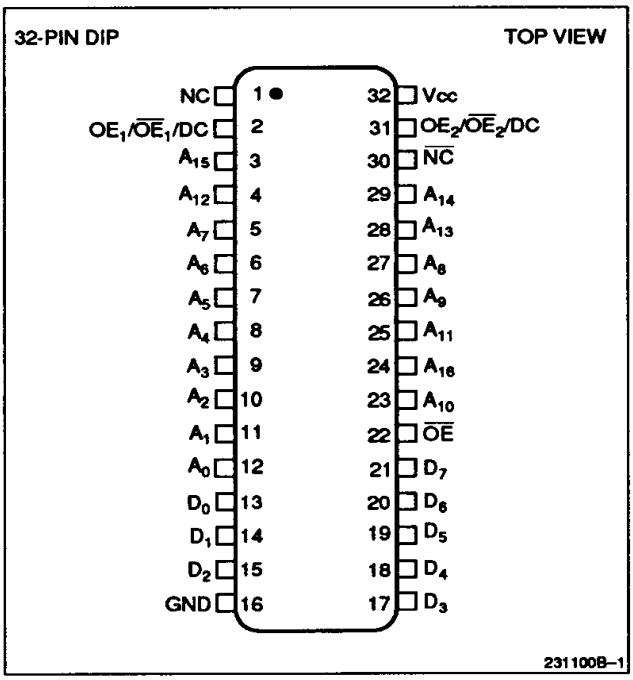

Figure 1. Pin Connections for DIP Package

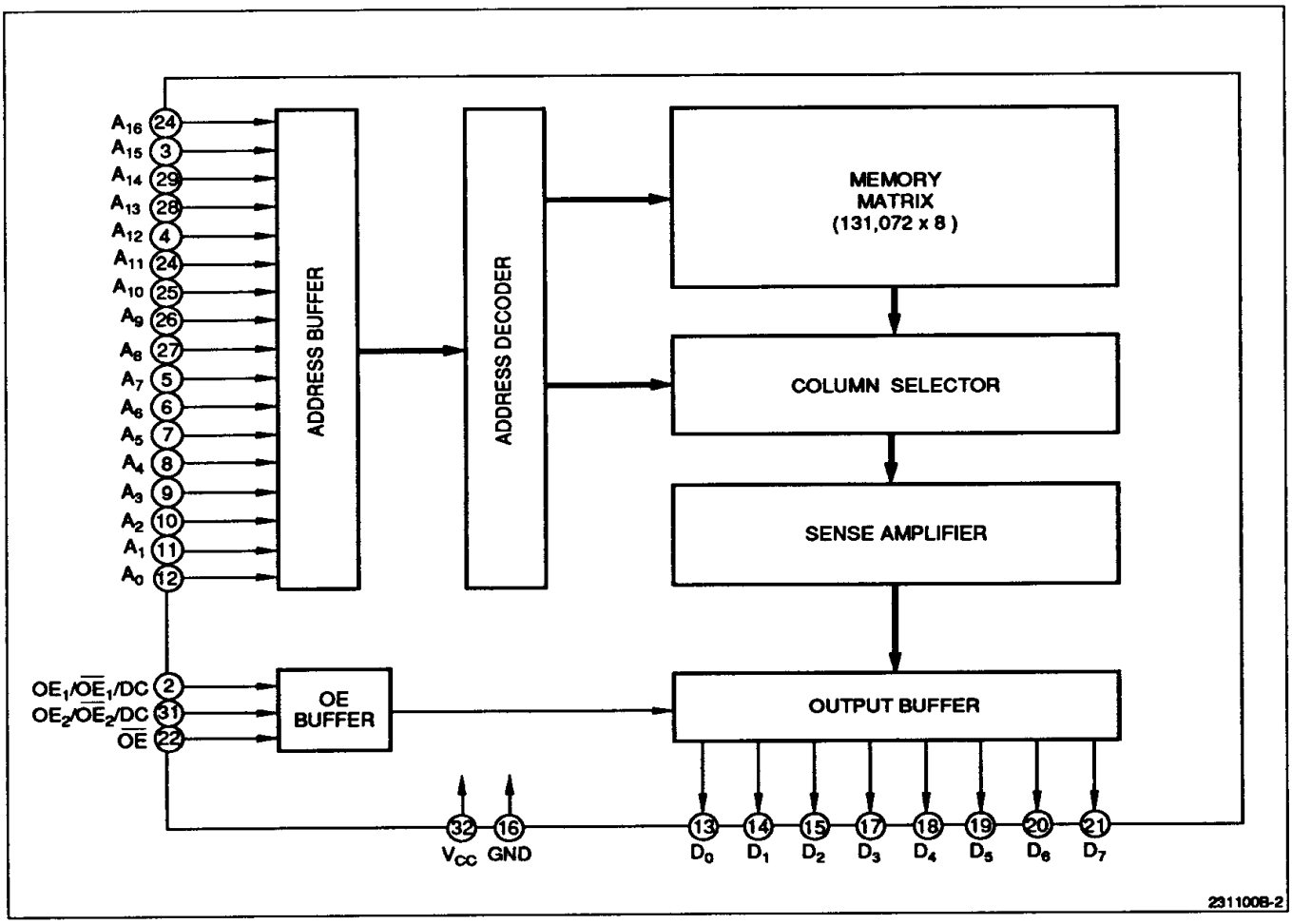

Figure 2. LH231100B Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{16}	Address input	
D_0 - D_7	Data output	
$OE_1/\overline{OE}_1/DC$ $OE_2/\overline{OE}_2/DC$	Output enable input or Don't Care connection	1

SIGNAL	PIN NAME	NOTE
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:
1. Active level of output enable is mask programmable. When DC is selected, it is fixed to an active level. (However, it is recommended to apply either "High" or "Low" to the DC pin).

TRUTH TABLE

$\overline{OE}$	$OE_1/\overline{OE}_1$	$OE_2/\overline{OE}_2$	MODE	D_0 - D_7	SUPPLY CURRENT	NOTE
H	X	X	Non selected	High-Z	Operating (I_{CC})	1
X	L/H	X				
X	X	L/H				
L	H/L	H/L	Selected	D_{OUT}		

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to +7.0	V	
Output voltage	V_{OUT}	-0.3 to +7.0	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC}	t_{RC} = 200 ns			100	mA	2

NOTES:
1. $\overline{OE}/\overline{OE_1}/\overline{OE_2}$ = V_{IH} or OE_1/OE_2 = V_{IL}
2. V_{IN} = V_{IH}/V_{IL}, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	200			ns	
Address access time	t_{AA}			200	ns	
Output enable access time	t_{OE}			80	ns	
Output hold time	t_{OH}	10			ns	
OE to output in High-Z	t_{OHZ}			80	ns	1

NOTE:
1. This is the time required for the output to become high impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			8	pF
Output capacitance	C_{OUT}			12	pF

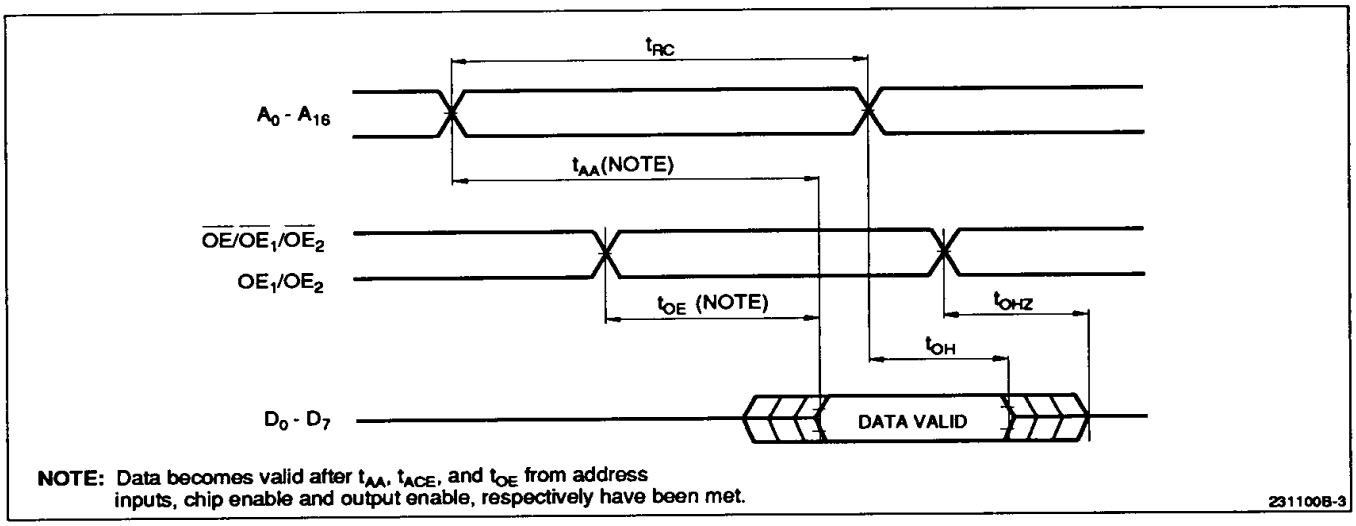

Figure 3. Timing Diagram

ORDERING INFORMATION