CA3282

Octal Low Side Power Driver with Serial Bus Control

June 1998

Features

- Output Current Drive Capability
  - All Outputs ON, Equal . . . . . 0.625A Each
  - Per Output Individually . . . . . 1A Each
  - Maximum Total of Outputs ON 5A
- High Voltage Power BiMOS Outputs
  - 8 Open Drain NDMOS Drivers
  - Individual Output Latch
  - Over-Current Limit Protection 1.05A
  - Over-Voltage Clamp Protection. 30V
- High Speed CMOS Logic Control
  - Low Quiescent I_{DD} Current 5mA
  - SPI Bus Controlled Interface
  - Individual Fault Unlatch and Feedback
  - Common Reset Line
- Operating Temperature Range . . . . . -40^{o}C to 125^{o}C

Applications

- Automotive and Industrial Systems
- Solenoids, Relays and Lamp Drivers
- Logic and µP Controlled Drivers
- Robotic Controls

Description

The CA3282 is a logic controlled, eight channel octal power driven. The serial peripheral interface (SPI) utilized by the CA3282 is a serial synchronous bus compatible with Intersil CDP68HC05, or equivalent, microcomputers. As shown in the Block Diagram for the CA3282 each of the open drain NDMOS output drivers has individual protection for over-voltage and over-current. Each output channel has separate output latch control with fault unlatch and diagnostic feedback. Under normal ON conditions, each output driver is in a low, saturation state. Comparators in the diagnostic circuitry monitor the output drivers to determine if an out of saturation condition exists. If a comparator senses a fault, the respective output driver is unlatched. In addition, over current protection is provided with current limiting in each output, independent of the diagnostic feedback loop.

The CA3282 is fabricated in a Power BiMOS IC process, and is intended for use in automotive and other applications having a wide range of temperature and electrical stress conditions. It is particularly suited for driving lamps, relays, and solenoids in applications where low operating power, high breakdown voltage, and high output current at high temperatures is required.

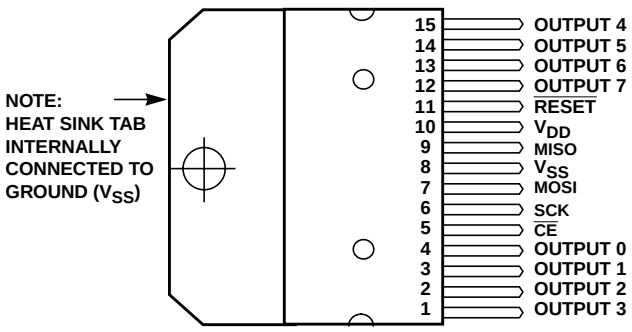
The CA3282 is supplied in 15 lead plastic SIP package with lead forms for either vertical or surface mount.

Ordering Information

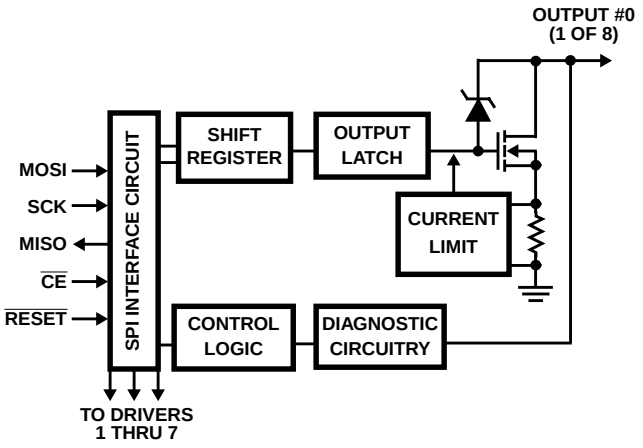
PART NUMBER	TEMP. RANGE(^{o}C)	PACKAGE AND LEAD FORM	PKG NO.
CA3282AS1	-40 to 125	15 Ld Plastic SIP Staggered Vertical	Z15.05A
CA3282AS2	-40 to 125	15 Ld Plastic SIP Surface Mount	Z15.05B

Pinout

CA3282 (SIP)
TOP VIEW



Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

File Number **2767.6**

Absolute Maximum Ratings

Output Voltage, V_O (Note 1) . . . . . V_{OC} (Clamp)
Output Load Current, I_{LOAD} (Per Output, Individual) 1A
Output Load Current, I_{LOAD} (All 8 Outputs ON, Equal I_{OUT}) 0.625A
Output Load Current, I_{LOAD} (Max. Total of Outputs ON) 5.0A
DC Logic Supply, V_{DD} 7V
Input Voltage, V_{IN} . . . . . -0.7 to +7V

Operating Conditions

Ambient Temperature Range . . . . . -40^oC to 125^oC
Junction Temperature Range . . . . . -40^oC to 150^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	$\theta_{JA}(^oC/W)$	$\theta_{JC}(^oC/W)$
Plastic SIP		
No Heat Sink	45	N/A
Infinite Heat Sink	N/A	3

Power Dissipation
Up to 125^oC w/o Heat Sink 0.56W
Above 125^oC w/o Heat Sink . . . . . .Derate Linearly at $22mW/^oC$
Up to 125^oC w/Infinite Heat Sink. 8.33W
Above 125^oC w/Infinite Heat Sink. . . . Derate Linearly at $333mW/^oC$
Maximum Storage Temperature Range . . . . . -55^oC to 150^oC
Maximum Lead Temperature (Soldering, 10s). . . . . 265^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The MOSFET Output Drain is internally clamped with a Drain-to-Gate zener diode that turns-on the MOSFET; holding the Drain at the Output Clamp Voltage, V_{OC}.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{DD} = 5V, T_A = -40^oC to 125^oC, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Supply Current, ON	I_{DD}	All Outputs ON, 0.5A Load Per Output	-	5	10	mA
Quiescent Supply Current, OFF	I_{DD}	All Outputs OFF	-	0.2	-	mA
Output Clamping Voltage	V_{OC}	I_{LOAD} = 0.5A, Output Programmed OFF	27	32	40	V
Output Clamping Energy	E_{OC}	I_{LOAD} = 0.5A, Output ON	20	-	-	mJ
Output Leakage Current	$I_{O\ LEAK}$	Output Programmed OFF V_O = 24V	-	150	1000	µA
		V_O = 14V	-	150	500	µA
		V_O = 5V	-	150	200	µA
Output ON Resistance	$r_{DS(ON)}$	I_{LOAD} = 0.5A (Note 3)	-	-	1	Ω
Output Current Limit	$I_{O\ LIMIT}$	Output Programmed ON, V_{OUT} > 3V	1.05	1.5	-	A
Turn-On Delay	t_{PHL}	I_O = 500mA, No Reactive Load	-	1	10	µs
Turn-Off Delay	t_{PLH}	I_O = 500mA, No Reactive Load	-	2	10	µs
Fault Reference Voltage	V_{OREF}	Output Programmed ON, Fault Detected If $V_O > V_{OREF}$	1.6	1.8	2.0	V
Fault Reset Delay (After $\overline{CE}$ Low to High Transition)	t_{UD}	See Figure 1	50	80	250	µs
Output OFF Voltage	V_{OFF}	Output Programmed OFF, Output Pin Floating	-	0	1	V
LOGIC INPUTS (MOSI, $\overline{CE}$, SCK and $\overline{RESET}$)						
Threshold Voltage at Falling Edge	V_{T-}	V_{DD} = 5V ±10%	$0.2V_{DD}$	$0.3V_{DD}$	-	V
Threshold Voltage at Rising Edge	V_{T+}	V_{DD} = 5V ±10%	-	$0.6V_{DD}$	$0.7V_{DD}$	V
Hysteresis Voltage	V_H	$V_{T+} - V_{T-}$	0.85	1.4	2.25	V
Input Current	I_I	V_{DD} = 5.5V, 0 < V_I < V_{DD}	-10	-	+10	µA
Input Capacitance	C_I	0 < V_I < V_{DD}	-	-	20	pF
LOGIC OUTPUT (MISO)						
Output LOW Voltage	V_{OL}	I_{OL} = 1.6mA	-	0.2	0.4	V
Output HIGH Voltage	V_{OH}	I_{OL} = 0.8mA	V_{DD} - 1.3V	V_{DD} - 0.2V	-	V

Electrical Specifications

V_{DD} = 5V, T_A = -40°C to 125°C, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Three State Leakage Current	I_{OL}	V_{DD} = 5.25V, 0 < V_O < V_{DD}, $\overline{CE}$ Pin Held High	-10	-	+10	µA
Output Capacitance	C_{OUT}	0 < V_O < V_{DD}, $\overline{CE}$ Pin Held High	-	-	20	pF

Serial Peripheral Interface Timing

(See Figure 1B)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Frequency	f_{OPER}		D.C.	Note 4	3.0	MHz
Enable Lead Time	(2) t_{LEAD}		-	<100	200	ns
Enable Lag Time	(3) t_{LAG}		-	<100	200	ns
Clock HIGH Time	(4) t_{wSCKH}		-	50	100	ns
Clock LOW Time	(5) t_{wSCKL}		-	50	100	ns
Data Setup Time	(6) t_{SU}		-	20	50	ns
Data Hold Time	(7) t_H		-	20	50	ns
Enable Time	(8) t_{EN}		-	50	100	ns
Disable Time	(9) t_{DIS}		-	150	300	ns
Data Valid Time	(10) t_V		-	75	150	ns
Output Data Hold Time	(11) t_{HO}		0	50	-	ns
Rise Time (MISO Output)	(12) t_{rSO}	V_{DD} = 20% to 70%, C_L = 200pF	-	35	100	ns
Rise Time SPI Inputs (SCK, MOSI, $\overline{CE}$)	(12) t_{rSI}	V_{DD} = 20% to 70%, C_L = 200pF	-	-	50	ns
Fall Time (MISO Output)	(13) t_{fSO}	V_{DD} = 70% to 20%, C_L = 200pF	-	45	100	ns
Fall Time SPI Inputs (SCK, MOSI, $\overline{CE}$)	(13) t_{fSI}	V_{DD} = 70% to 20%, C_L = 200pF	-	-	50	ns

NOTES:

3. Refer to Figure 4A for I_{OUT} current vs V_{SAT} voltage. Typical $r_{DS(ON)}$ values are given for -40°C, 25°C, 105°C and 125°C temperatures.
4. The Maximum Operating Frequency is typically greater than 10MHz but it is application limited primarily by external SPI input rise/fall times and MISO output loading.

Timing Diagrams

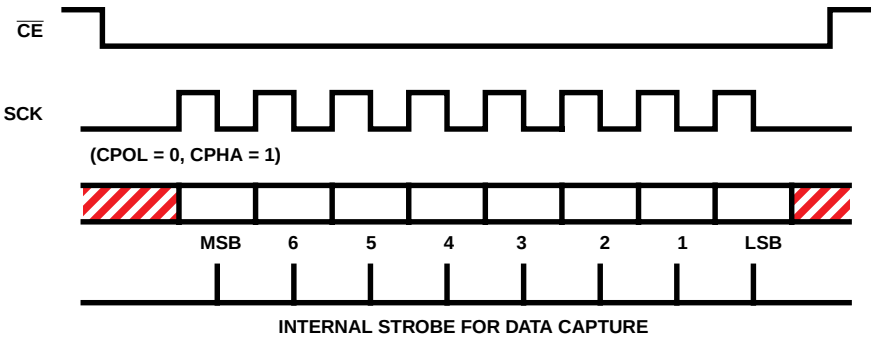


FIGURE 1A. DATA AND CLOCK TIMING DIAGRAM

Timing Diagrams (Continued)

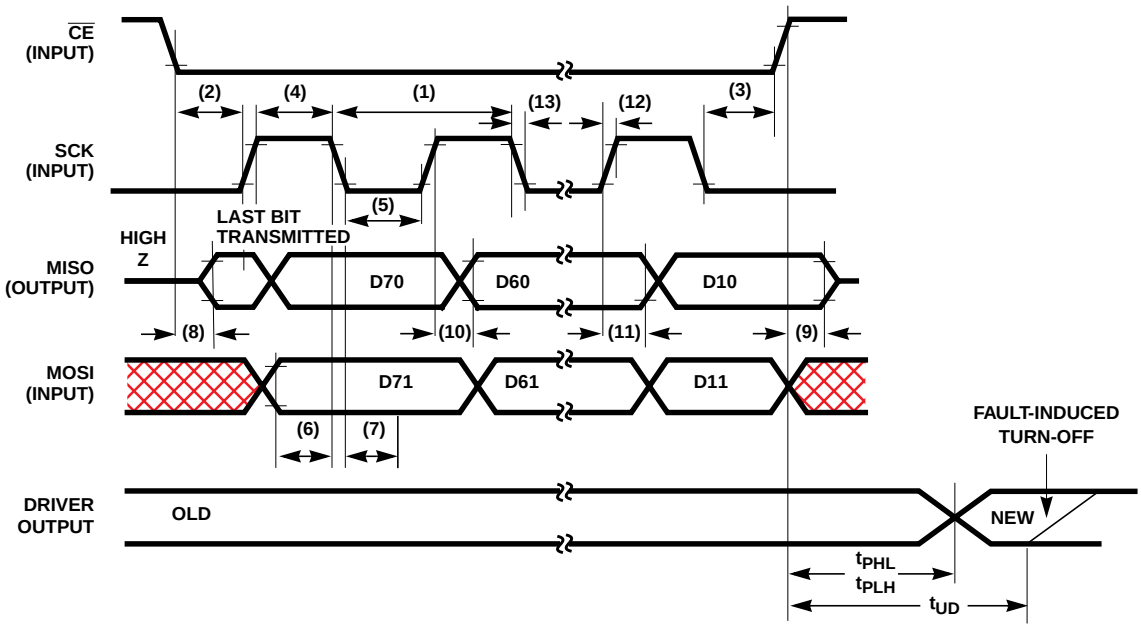


FIGURE 1B. SPI TIMING DIAGRAM

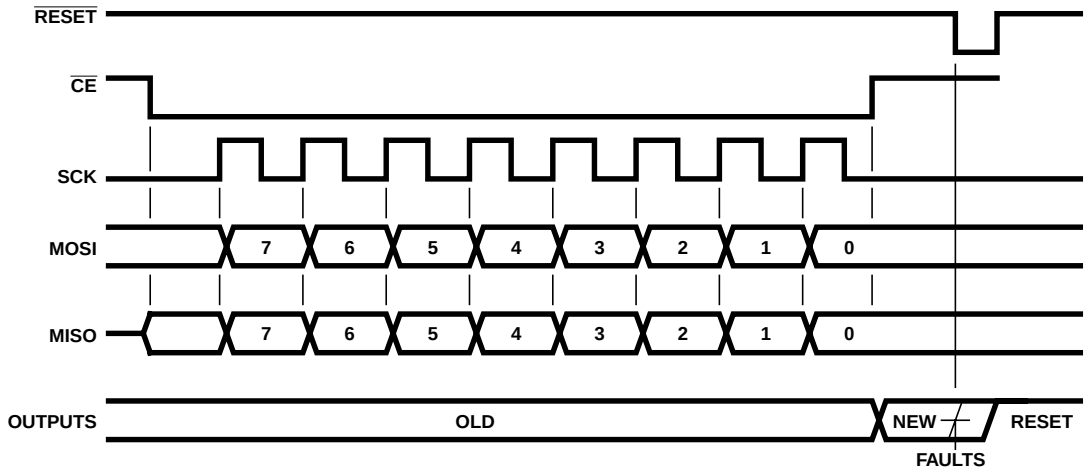


FIGURE 2. BYTE TIMING DIAGRAM WITH ASYNCHRONOUS RESET

Signal Descriptions

Power Output Drivers, Output 0 - Output 7 - The input and output bits corresponding to Output 0 thru Output 7 are transmitted and received most significant bit (MSB) first via the SPI bus. The outputs are provided with current limiting and voltage sense functions for fault indication and protection. The nominal load current for these outputs is 500mA, with current limiting set to a minimum of 1.05A. An on-chip clamp circuit capable of handling 500mA is provided at each output for clamping inductive loads.

$\overline{\text{RESET}}$ - Active low reset input. When this input line is low, the shift register and output latches are configured to turn off all output drivers. A power on clear function may be implemented by connecting this pin to V_{DD} with an external resistor, and to V_{SS} with an external capacitor. In any case, this pin must not be left floating.

$\overline{\text{CE}}$ - Active low chip enable. Data is transferred from the shift register to the outputs on the rising edge of this signal. The falling edge of $\overline{\text{CE}}$ loads the shift register with the output voltage sense bits coming from the output stages. The output driver for the MISO pin is enabled when this pin is low. $\overline{\text{CE}}$ must be a logic low prior to the first serial clock (SCK) and must remain low until after the last (eighth) serial clock cycle. A low level on $\overline{\text{CE}}$ also activates an internal disable circuit used for unlatching output states that are in a fault mode as

sensed by an out of saturation condition. A high on $\overline{CE}$ forces MISO to a high impedance state. Also, when $\overline{CE}$ is high, the octal driver ignores the SCK and MOSI signals.

SCK, MISO, MOSI - See Serial Peripheral Interface (SPI) section in this data sheet.

V_{DD} and V_{SS} (GND) - Positive and negative power supply lines.

Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) utilized by the CA3282 is a serial synchronous bus for control and data transfers. The Clock (SCK), which is generated by the microcomputer, is active only during data transfers. In systems using CDP68HC05 family microcomputers, the inactive clock polarity is determined by the CPOL bit in the microcomputer's control register. The CPOL bit is used in conjunction with the clock phase bit, CPHA to produce the desired clock data relationship between the microcomputer and octal driver. The CPHA bit in general selects the clock edge which captures data and allows it to change states. For the CA3282, the CPOL bit must be set to a logic zero and the CPHA bit to a logic one. Configured in this manner, MISO (output) data will appear with every rising edge SCK, and MOSI (input) data will be latched into the shift register with every falling edge of SCK. Also, the steady state value of the inactive serial clock, SCK, will be at a low level. Timing diagrams for the serial peripheral interface are shown in Figure 1.

SPI Signal Descriptions

MOSI (Master Out/Slave In) - Serial data input. Data bytes are shifted in at this pin, most significant bit (MSB) first. The data is passed directly to the shift register which in turn controls the latches and output drivers. A logic "0" on this pin will program the corresponding output to be ON, and a logic "1" will turn it OFF.

MISO (Master In/Slave Out) - Serial data output. Data bytes are shifted out at this pin, most significant bit (MSB) first. This pin is the serial output from the shift register and is three stated when $\overline{CE}$ is high. A high for a data bit on this pin indicates that the corresponding output is high. A low on this pin for a data bit indicates that the output is low. Comparing the serial output bits with the previous input bits, the microcomputer implements the diagnostic data supplied by the CA3282.

SCK - Serial clock input. This signal clocks the shift register SCK and new MOSI (input) data will be latched into the shift register on every falling edge of SCK. The SCK phase bit, CPHA, and polarity bit, CPOL, must be set to 1 and 0, respectively in the microcomputer's control register.

Functional Descriptions

The CA3282 is a low operating power, high voltage, high current, octal power driver featuring eight channels of open drain NDMOS output drivers. The drivers have low saturation voltage and output short circuit protection, suited for driving resistive or inductive loads such as lamps, relays and solenoids. Data is transmitted to the device serially using the Serial Peripheral Interface (SPI) protocol. Each channel is independently controlled by an output latch and a common $\overline{RESET}$ line that disables all eight outputs. Byte timing with asynchronous reset is shown in Figure 4. The circuit receives 8-bit serial data by means of the serial input (MOSI), and stores this data in an internal register to control the output drivers. The serial output (MISO) provides 8-bit diagnostic data representing the voltage level at the driver output. This allows the microcomputer to diagnose the condition at the output drivers. The device is selected when the chip enable ($\overline{CE}$) line is low. When ($\overline{CE}$) is high, the device is deselected and the serial output (MISO) is placed in a three-state mode. The device shifts serial data on the rising edge of the serial clock (SCK), and latches data on the falling edge. On the rising edge of chip enable ($\overline{CE}$), new input data from the shift register is latched in the output drivers. The falling edge of chip enable ($\overline{CE}$) transfers the output drivers fault information back to the shift register. The output drivers have low ON voltage at rated current, and are monitored by a comparator for an out of saturation condition, in which case the output driver with the fault becomes unlatched and diagnostic data is sent to the microcomputer via the MISO line. A typical microcomputer interface circuit is shown in Figure 2. Also, the CA3282 may be cascaded with another CA3282 octal driver.

Shift Register

The shift register has both serial and parallel inputs and outputs. Serial output and input data are simultaneously transferred to and from the SPI bus. The parallel outputs are latched into the output latch in the CA3282 at the end of a data transfer. The parallel inputs jam diagnostic data into the shift register at the beginning of a data transfer cycle.

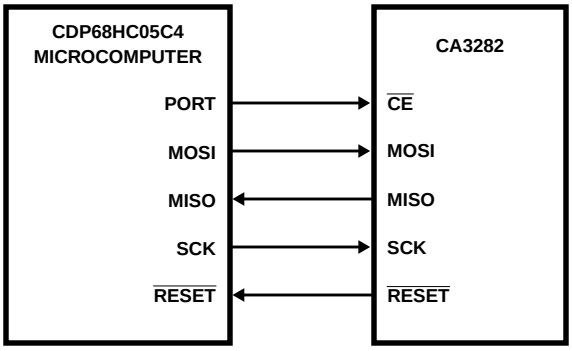


FIGURE 3. TYPICAL MICROCOMPUTER INTERFACE WITH THE CA3282

Output Latch

The output latch holds input data from the shift register which is used to activate the outputs. The latch circuit may be cleared by a fault condition (to protect the overloaded outputs), or by the $\overline{RESET}$ signal.

Output Drivers

The output drivers provide and active low output of 500mA nominal with current limiting set to 1.05A to allow for high inrush currents. In addition, each output is provided with a voltage clamp circuit to limit inductive transients. Each output driver is also monitored by a comparator for an out of saturation condition. If the output voltage of an ON output pin exceeds the saturation voltage limit, a fault condition is assumed and the latch driving this output is reset, turning the output off. The output comparators, which also provide diagnostic feedback data to the shift register, contain an internal pull-down current which will cause the cell to indicate a low output voltage if the output is programmed OFF and the output pin is open circuited.

$\overline{CE}$ High to Low Transition

When $\overline{CE}$ is low the three state MISO pin is enabled. On the falling edge of $\overline{CE}$, diagnostic data from the output voltage comparators will be latched into the shift register. If an output is high, a logic one will be loaded into that bit in the shift register. If the output is low, a logic zero will be loaded. During the time that $\overline{CE}$ is low, data bytes controlling the output drivers are shifted in at the MOSI pin most significant bit (MSB) first. A logic zero on this pin will program the corresponding output to be ON, and a logic one will turn it OFF.

$\overline{CE}$ Low to High Transition

When the last data bit has been shifted into the CA3282, the $\overline{CE}$ pin should be pulled high. At the rising edge of $\overline{CE}$, shift register data is latched into the output latch and the outputs are activated with the new data. An internal 150µs delay timer will start at this rising edge to compensate for high inrush currents in lamps and inductive loads. During this period, the outputs will be protected only by the analog current limiting circuits since resetting of the output latches by fault conditions will be inhibited during this time. This allows the device to handle inrush currents immediately after turn on. When the 150µs delay has elapsed, the output voltages are sensed by the comparators and any out of saturation outputs are latched off. The serial clock input pin (SCK) should be low during $\overline{CE}$ transitions to avoid false clocking of the shift register. The SCK input is gated by $\overline{CE}$ so that the SCK input is ignored when $\overline{CE}$ is high.

Detecting Fault Conditions

Fault conditions may be checked as follows. Clock in a new control byte and wait approximately 150µs to allow the outputs to settle. Clock in the same control byte and note the diagnostic data output at the MISO pin. The diagnostic bits should be identical to the data clocked in. Any differences will indicate a fault in the corresponding outputs. For example, if an output was programmed ON by clocking in a zero, and the corresponding diagnostic bit for that output is a one, indicating the driver output is still high, then a short circuit or overload condition may have caused the output to unlatch. Alternatively, if the output was programmed OFF by clocking in one, and the diagnostic bit for that output shows a zero, then the probable cause is an open circuit resulting in a floating output.

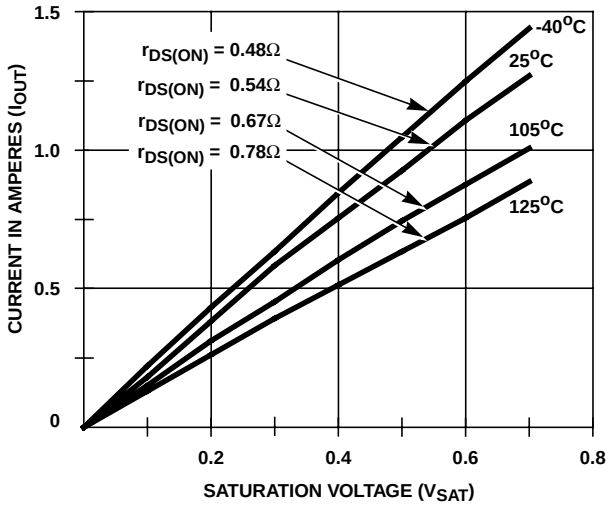


FIGURE 3A. CA3282 TYPICAL OUTPUT DRIVER $r_{DS(ON)}$ CHARACTERISTICS OF CURRENT OUT vs SATURATION VOLTAGE, V_{SAT} FOR A -40°C TO 125°C JUNCTION TEMPERATURE

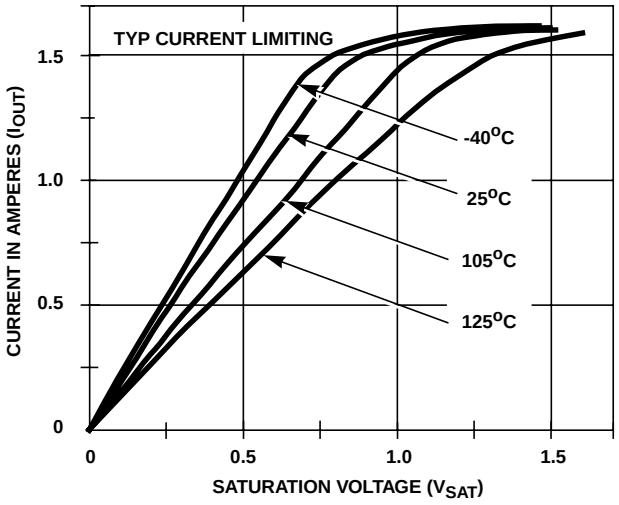


FIGURE 3B. CA3282 TYPICAL OUTPUT DRIVER $r_{DS(ON)}$ CHARACTERISTICS OF CURRENT OUT vs SATURATION VOLTAGE, V_{SAT} FOR A -40°C TO 125°C JUNCTION TEMPERATURE

Dissipation In Multiple Outputs

The CA3282 Octal Power Driver has multiple MOS Output Drivers and requires special consideration with regard to maximum current and dissipation ratings. While each output has a maximum current specification consistent with the device structure, all such devices on the chip can not be simultaneously rated to the same high level of peak current. The total combined current and the dissipation on the chip must be adjusted for maximum allowable ratings, given simultaneous multiple output conditions.

For the CA3282, the maximum positive output current rating is 1A when one output is ON. When ALL outputs are ON, the rating is reduced to 0.625A because the total maximum current is limited to 5A. For any given application, all output drivers on a chip may or may not have a different level of loading. The discussion here is intended to provide relatively simple methods to determine the maximum dissipation and current ratings as a general solution and, as a special solution, when all switched ON outputs have the same current loading.

General Solution

A general equation for dissipation should specify that the total power dissipation in a package is the sum of all significant elements of dissipation on the chip. However, in Power BiMOS Circuits very little dissipation is needed to control the logic and predriver circuits on the chip. The over-all chip dissipation is primarily the sum of the I^2R dissipation losses in each channel where the current, I is the output current and the resistance, R is the NMOS channel resistance, $r_{DS(ON)}$ of each output driver. As such, the total dissipation, P_D for n output drivers is:

$$P_D = \sum_{k=1}^{n} P_k \quad \text{(EQ. 1)}$$

This expression sums the dissipation, P_K of each output driver without regard to uniformity of dissipation in each MOS channel. The dissipation loss in an NMOS channel is:

$$P_k = I^2 \times r_{DS(ON)} \quad \text{(EQ. 2)}$$

where the current, I is determined by the output load when the channel is turned ON. The channel resistance, $r_{DS(ON)}$ is a function of the circuit design, level of gate voltage and the chip temperature. Refer to the Electrical Specifications values for worse case channel resistance.

The temperature rise in the package due to the dissipation is the product of the on-chip dissipation, P_D and the package Junction-to-Case thermal resistance, θ_{JC}. To determine the junction temperature, T_J, given the case (heat sink tab) temperature, T_C, the linear heat flow solution is:

$$T_J = T_C + P_D \times \theta_{JC} \quad \text{(EQ. 3)}$$

or

$$T_C = T_J - P_D \times \theta_{JC} \quad \text{(EQ. 3A)}$$

Since this solution relates only to the package, further consideration must be given to a practical heat sink. The equation of linear heat flow assumes that the Junction-to-Ambient thermal resistance, θ_{JA}, is the sum of the thermal resistance from Junction-to-Case and the thermal resistance from Case (heat sink)-to-Ambient, θ_{CA}. The Junction-to-Ambient thermal resistance, θ_{JA} is the sum of all thermal paths from the chip junction to the ambient temperature (T_A) environment and can be expressed as:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad \text{(EQ. 4)}$$

Equation 3 and Equation 3A may be expressed as:

$$T_J = T_A + P_D \times \theta_{JA} \quad \text{(EQ. 5)}$$

or

$$T_A = T_J - P_D \times \theta_{JA} \quad \text{(EQ. 5A)}$$

Not all Integrated Circuit packages have a directly definable case temperature because the heat is spread thru the lead frame to a PC Board which is the effective heat sink.

Calculation Example 1

For the CA3282, $\theta_{JC} = 3^oC/W$ and the worst case junction temperature, as an application design solution, should not exceed 150^oC. For any given application, Equation 1 determines the dissipation, P_D.

Assume the package is mounted to a heat sink having a thermal resistance of $6^oC/W$ and, for a given application, the dissipation, P_D = 3W. Assume the operating ambient temperature, $T_A = 100^oC$. The calculated Junction-to-Ambient thermal resistance is:

$\theta_{JA} = \theta_{JC} + \theta_{CA} = 9^oC/W$

The solution for junction temperature by Equation 5 is :

$T_J = 100^oC + 3W \times 9^oC/W = 127^oC$

Calculation Example 2

Using the CA3282 maximum Junction-to-Ambient Thermal Resistance, θ_{JA} value of $45^oC/W$ (no external heat sink) and the worst case Junction Temperature, T_C of 150^oC we have an application design solution for the maximum ambient temperature or dissipation. For example; Using Equation 1 and assuming a device dissipation, P_D of 1W, the maximum allowable Ambient Temperature, T_A from Equation 5A is calculated as follows:

$T_A = 150^oC - 1.0W \times 45^oC/W = 105^oC$

Equal Current Loading Solution

Where a given application has equal current loading in the output drivers, equal $r_{DS(ON)}$ and temperature conditions may be assumed. As such, a convenient method to show rating boundaries is to substitute the dissipation Equation 2 into the junction temperature Equation 3. For m outputs that are ON with equal currents, where $I = I_1 = I_2 ..... = I_m$, we have the following solution for dissipation:

$$P_D = m \times P_k = m \times I^2 \times r_{DS(ON)} \quad \text{(EQ. 6)}$$

$$I = \sqrt{\frac{T_J - T_C}{m \times \theta_{JC} \times r_{DS(ON)}}} \quad \text{(EQ. 7)}$$

The number of output drivers ON and conducting (m) may be from 1 to n. (i.e., For all 8 output drivers conducting, m = n = 8.) Maximum temperature, dissipation and current ratings must be observed. The drain current vs case temperature may be plotted for any value of m from 1 to 8, provided drain currents remain equal.

The curve of Figure 5 illustrates the boundary limits for temperature and dissipation. Figure 6 shows the maximum current for all 8 outputs ON with equal current plotted versus Case Temperature, T_C. Boundary conditions relate to the Absolute Maximum Ratings as defined in the data sheet.

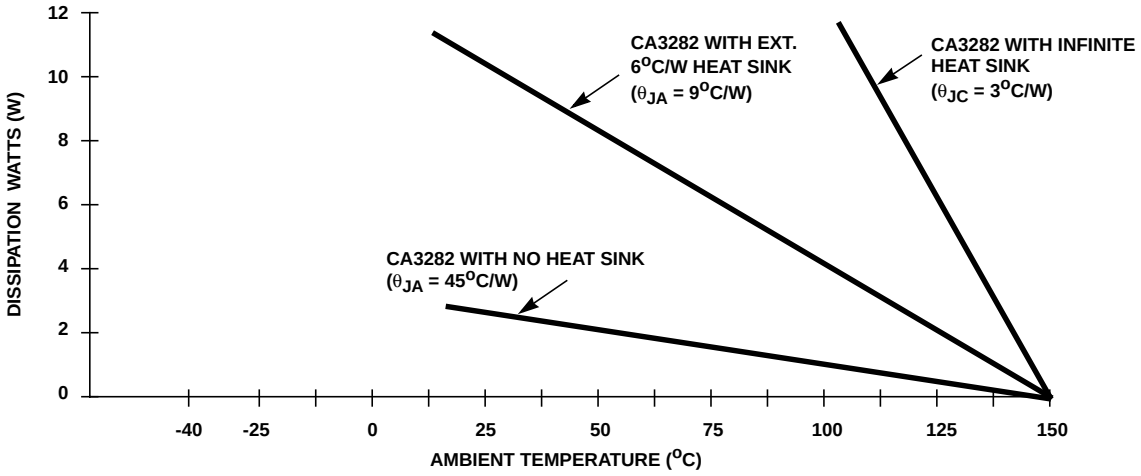


FIGURE 5. DISSIPATION DERATING CURVE

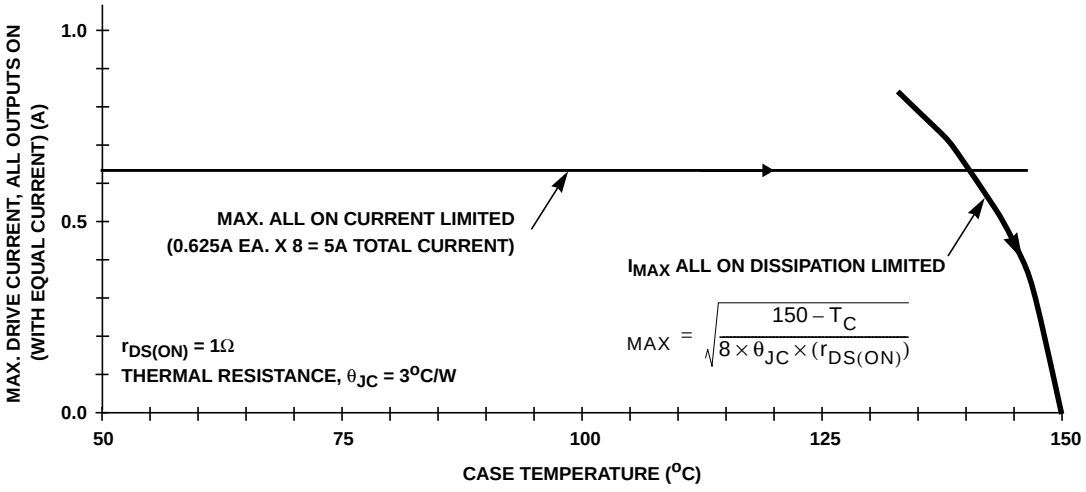
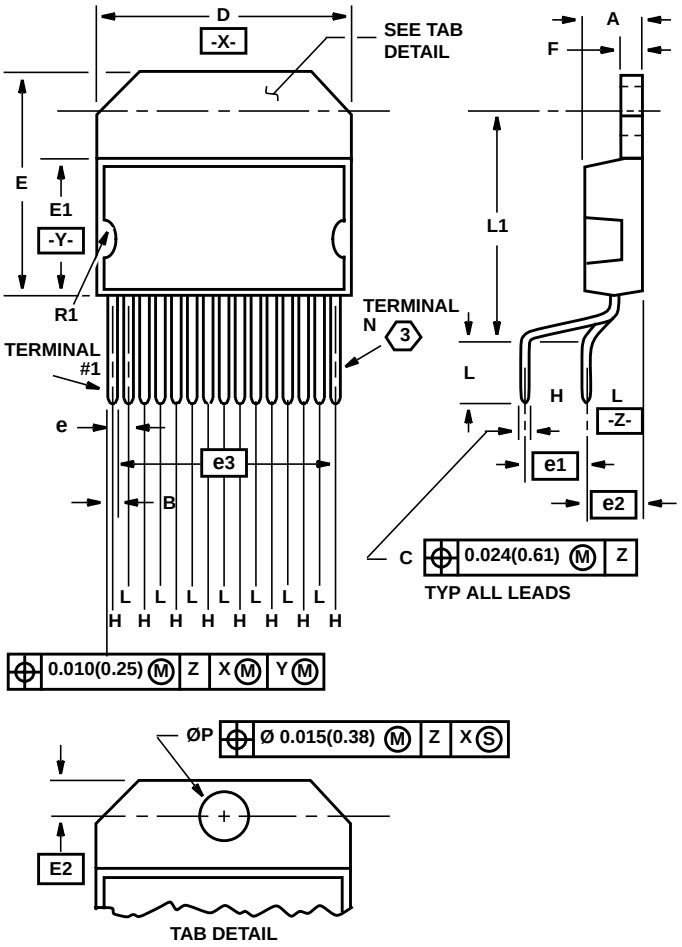


FIGURE 6. CURRENT vs CASE (TAB) TEMPERATURE, ALL OUTPUTS ON WITH EQUAL CURRENT

Single-In-Line Plastic Packages (SIP)



Z15.05A (JEDEC MO-048 AB ISSUE A)
15 LEAD PLASTIC SINGLE-IN-LINE PACKAGE STAGGERED VERTICAL LEAD FORM

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.172	0.182	4.37	4.62
B	0.024	0.031	0.61	0.79
C	0.014	0.024	0.36	0.61
D	0.778	0.798	19.76	20.27
E	0.684	0.694	17.37	17.63
E1	0.416	0.426	10.57	10.82
E2	0.110 BSC		2.79 BSC	
e	0.050 BSC		1.27 BSC	
e1	0.200 BSC		5.08 BSC	
e2	0.169 BSC		4.29 BSC	
e3	0.700 BSC		17.78 BSC	
F	0.057	0.063	1.45	1.60
L	0.150	0.176	3.81	4.47
L_1	0.690	0.710	17.53	18.03
N	15		15	
ØP	0.148	0.152	3.76	3.86
R1	0.065	0.080	1.65	2.03

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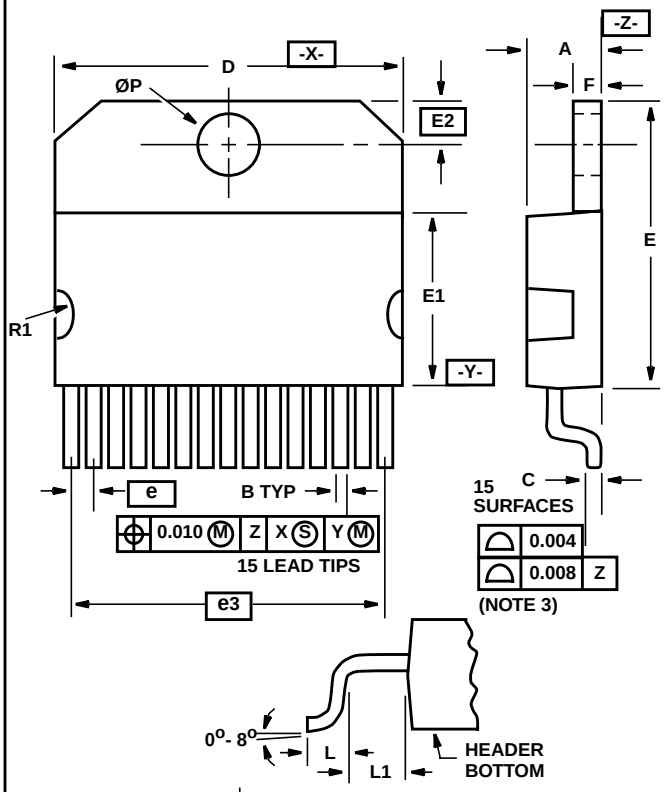
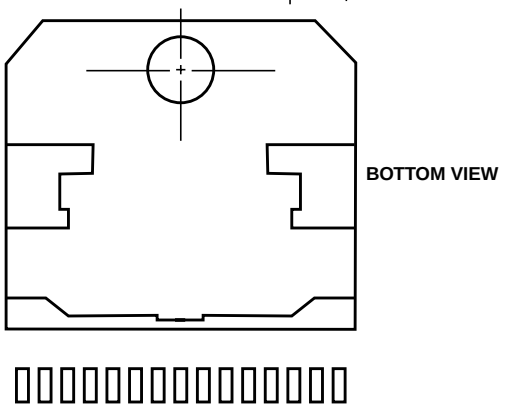
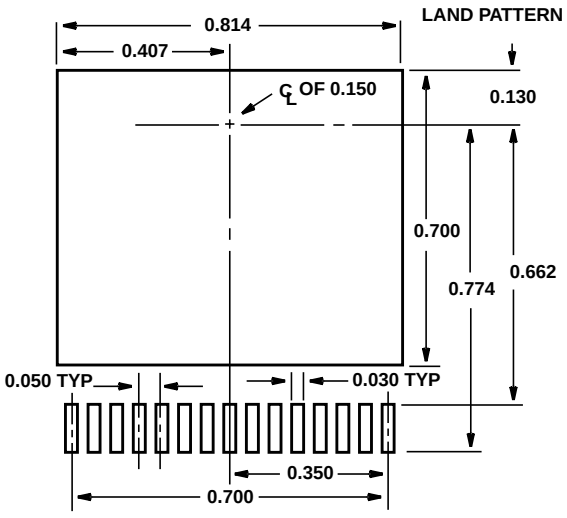
NOTES:

1. Refer to series symbol list, JEDEC Publication No. 95.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1982.
3. N is the number of terminals.
4. Controlling dimension: INCH.

Single-In-Line Plastic Packages (SIP)







Z15.05B

15 LEAD PLASTIC SINGLE-IN-LINE PACKAGE SURFACE MOUNT "GULLWING" LEAD FORM

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.172	0.182	4.37	4.62
B	0.024	0.031	0.61	0.79
C	0.018	0.024	0.46	0.61
D	0.778	0.798	19.76	20.27
E	0.684	0.694	17.37	17.63
E1	0.416	0.426	10.57	10.82
E2	0.110 BSC		2.79 BSC	
e	0.050 BSC		1.27 BSC	
e3	0.700 BSC		17.78 BSC	
F	0.057	0.063	1.45	1.60
L	0.065	0.080	1.66	2.03
L1	0.098	0.108	2.49	2.74
N	15		15	
ØP	0.148	0.152	3.76	3.86
R1	0.065	0.080	1.65	2.03

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NOTES:

1. Dimensioning and Tolerancing per ANSI Y14.5M - 1982.
2. N is the number of terminals.
3. All lead surfaces are within 0.004 inch of each other. No lead can be more than 0.004 inch above or below the header plane, (-Z- Datum).
4. Controlling dimension: INCH.