National Semiconductor

LMC6064EP

OBSOLETE
August 30, 2011

Precision CMOS Quad Micropower Operational Amplifier

General Description

The LMC6064EP is a precision quad low offset voltage, micropower operational amplifier, capable of precision single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low power consumption make the LMC6064EP ideally suited for battery powered applications.

Other applications using the LMC6064EP include precision full-wave rectifiers, integrators, references, sample-and-hold circuits, and true instrumentation amplifiers.

This device is built with National's advanced double-Poly Silicon-Gate CMOS process.

For designs that require higher speed, see the LMC6084 precision quad operational amplifier.

For single or dual operational amplifier with similar features, see the LMC6061 or LMC6062 respectively.

ENHANCED PLASTIC

- Extended Temperature Performance of −40°C to +85°C
- Baseline Control - Single Fab & Assembly Site
- Process Change Notification (PCN)
- Qualification & Reliability Data
- Solder (PbSn) Lead Finish is standard
- Enhanced Diminishing Manufacturing Sources (DMS) Support

PATENT PENDING

Features

(Typical Unless Otherwise Noted)

- Low offset voltage: 100 µV
- Ultra low supply current: 16 µA/Amplifier
- Operates from 4.5V to 15V single supply
- Ultra low input bias current: 10 fA
- Output swing within 10 mV of supply rail, 100k load
- Input common-mode range includes V−
- High voltage gain: 140 dB
- Improved latchup immunity

Applications

- Instrumentation amplifier
- Photodiode and infrared detector preamplifier
- Transducer amplifiers
- D/A converter
- Selected Military Applications
- Selected Avionics Applications

Ordering Information

Part Number	VID Part Number	NS Package Number (*Note 3*)
LMC6064AIMEP	V62/04748-01	M14A
(*Note 1*, *Note 2*)	TBD	TBD

Note 1: For the following (Enhanced Plastic) version, check for availability: LMC6064AIMEP, LMC6064IMEP, LM6064AIMXEP, LM6064IMXEP, LMC6064AINEP, LMC6064INEP. Parts listed with an "X" are provided in Tape & Reel and parts without an "X" are in Rails.

Note 2: FOR ADDITIONAL ORDERING AND PRODUCT INFORMATION, PLEASE VISIT THE ENHANCED PLASTIC WEB SITE AT: www.national.com/mil

Note 3: Refer to package details under Physical Dimensions

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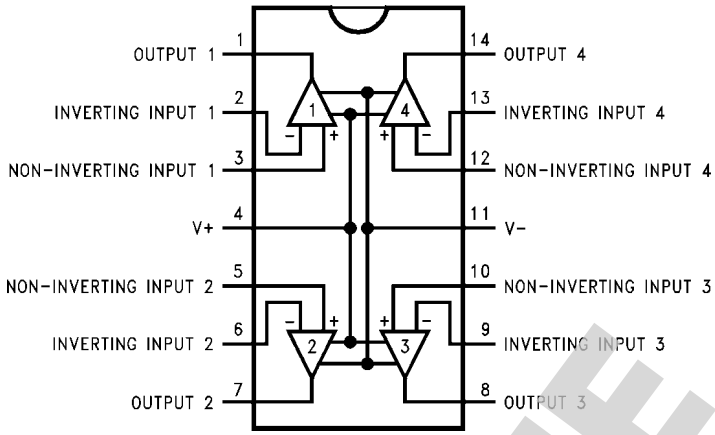
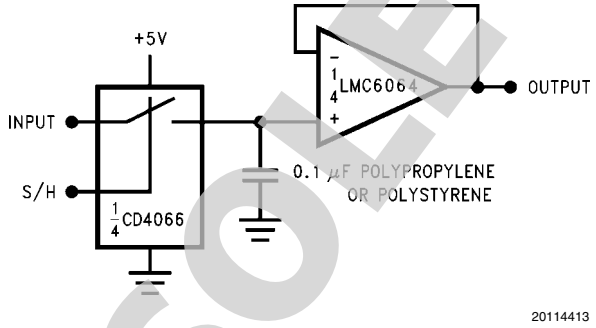
Connection Diagram

14-Pin DIP/SO



Top View

Low-Leakage Sample and Hold



Absolute Maximum Ratings (*Note 4*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	(V^+) +0.3V, (V^-) −0.3V
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(*Note 14*)
Output Short Circuit to V^-	(*Note 5*)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature	150°C
ESD Tolerance (*Note 7*)	2 kV
Current at Input Pin	±10 mA
Current at Output Pin	±30 mA
Current at Power Supply Pin	40 mA
Power Dissipation	(*Note 6*)

Operating Ratings (*Note 4*)

Temperature Range	
LMC6064AIEP, LMC6064IEP	$-40°C \le T_J \le +85°C$
Supply Voltage	$4.5V \le V^+ \le 15.5V$
Thermal Resistance (θ_{JA}) (*Note 15*)	
14-Pin Molded DIP	81°C/W
14-Pin SO	126°C/W
Power Dissipation	(*Note 13*)

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified. (*Note 16*)

Symbol	Parameter	Conditions		Typ (*Note 8*)	LMC6064AIEP Limit (*Note 9*)	LMC6064IEP Limit (*Note 9*)	Units
V_{OS}	Input Offset Voltage			100	350 **900**	800 **1300**	µV Max
TCV_{OS}	Input Offset Voltage Average Drift			1.0			µV/°C
I_B	Input Bias Current			0.010	 **4**	 **4**	pA Max
I_{OS}	Input Offset Current			0.005	 **2**	 **2**	pA Max
R_{IN}	Input Resistance			>10			Tera Ω
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$		85	75 **72**	66 **63**	dB Min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$		85	75 **72**	66 **63**	dB Min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$		100	84 **81**	74 **71**	dB Min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V for CMRR ≥ 60 dB		−0.4	−0.1 **0**	−0.1 **0**	V Max
				$V^+ - 1.9$	$V^+ - 2.3$ **$V^+ - 2.5$**	$V^+ - 2.3$ **$V^+ - 2.5$**	V Min
A_V	Large Signal Voltage Gain	$R_L = 100 kΩ$ (*Note 10*)	Sourcing	4000	400 **300**	300 **200**	V/mV Min
			Sinking	3000	180 **100**	90 **60**	V/mV Min
		$R_L = 25 kΩ$ (*Note 10*)	Sourcing	3000	400 **150**	200 **80**	V/mV Min
			Sinking	2000	100 **50**	70 **35**	V/mV Min

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Symbol	Parameter	Conditions	Typ (*Note 8*)	LMC6064AIEP Limit (*Note 9*)	LMC6064IEP Limit (*Note 9*)	Units
V_O	Output Swing	V^+ = 5V R_L = 100 kΩ to 2.5V	4.995	4.990 **4.980**	4.950 **4.925**	V Min
			0.005	0.010 **0.020**	0.050 **0.075**	V Max
		V^+ = 5V R_L = 25 kΩ to 2.5V	4.990	4.975 **4.965**	4.950 **4.850**	V Min
			0.010	0.020 **0.035**	0.050 **0.150**	V Max
		V^+ = 15V R_L = 100 kΩ to 7.5V	14.990	14.975 **14.965**	14.950 **14.925**	V Min
			0.010	0.025 **0.035**	0.050 **0.075**	V Max
		V^+ = 15V R_L = 25 kΩ to 7.5V	14.965	14.900 **14.850**	14.850 **14.800**	V Min
			0.025	0.050 **0.150**	0.100 **0.200**	V Max
I_O	Output Current V^+ = 5V	Sourcing, V_O = 0V	22	16 **10**	13 **8**	mA Min
		Sinking, V_O = 5V	21	16 **8**	16 **8**	mA Min
I_O	Output Current V^+ = 15V	Sourcing, V_O = 0V	25	15 **10**	15 **10**	mA Min
		Sinking, V_O = 13V (*Note 14*)	26	20 **8**	20 **8**	mA Min
I_S	Supply Current	All Four Amplifiers V^+ = +5V, V_O = 1.5V	64	76 **92**	92 **112**	µA Max
		All Four Amplifiers V^+ = +15V, V_O = 7.5V	80	94 **110**	114 **132**	µA Max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified. (*Note 16*)

Symbol	Parameter	Conditions	Typ (*Note 8*)	LMC6064AIEP Limit (*Note 9*)	LMC6064IEP Limit (*Note 9*)	Units
SR	Slew Rate	(*Note 11*)	35	20 **10**	15 **7**	V/ms Min
GBW	Gain-Bandwidth Product		100			kHz
θ_m	Phase Margin		50			Deg
	Amp-to-Amp Isolation	(*Note 12*)	155			dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	83			$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002			$pA/\sqrt{Hz}$
T.H.D.	Total Harmonic Distortion	F = 1 kHz, A_V = −5 R_L = 100 kΩ, V_O = 2 V_{PP} ±5V Supply	0.01			%

Note 4: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 5: Applies to both single-supply and split-supply operation. Continous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 6: The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A)/\theta_{JA}$.

Note 7: Human body model, 1.5 kΩ in series with 100 pF.

Note 8: Typical values represent the most likely parametric norm.

Note 9: All limits are guaranteed by testing or statistical analysis.

Note 10: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \leq V_O \leq 11.5V$. For Sinking tests, $2.5V \leq V_O \leq 7.5V$.

Note 11: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 12: Input referred $V^+ = 15V$ and $R_L = 100$ kΩ connected to 7.5V. Each amp excited in turn with 100 Hz to produce $V_O = 12\ V_{PP}$.

Note 13: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 14: Do not connect output to V^+, when V^+ is greater than 13V or reliability witll be adversely affected.

Note 15: All numbers apply for packages soldered directly into a PC board.

Note 16: "Testing and other quality control techniques are used to the extent deemed necessary to ensure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific PARAMETRIC testing, product performance is assured by characterization and/or design."

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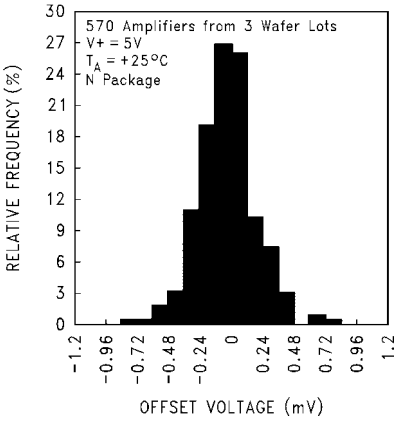
Typical Performance Characteristics

Distribution of LMC6064AIMEP Input Offset Voltage (T_A = +25°C)



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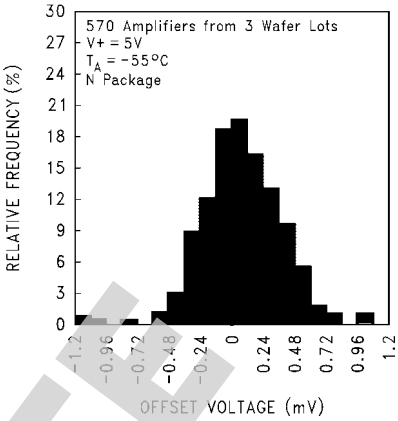
Distribution of LMC6064AIMEP Input Offset Voltage (T_A = −55°C)



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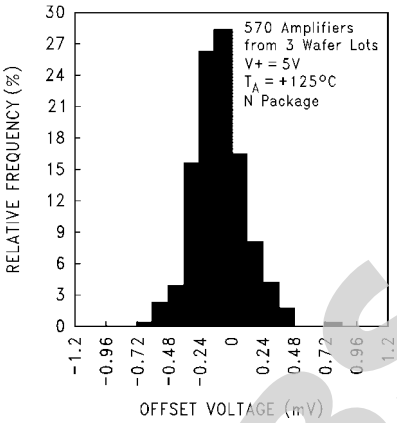
Distribution of LMC6064AIMEP Input Offset Voltage (T_A = +125°C)



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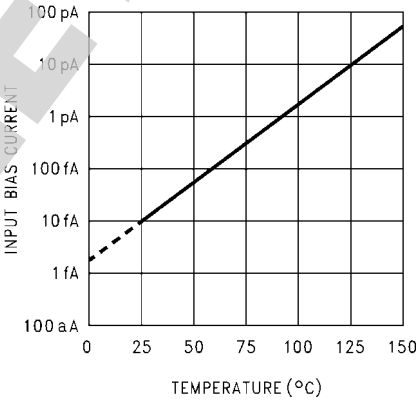
Input Bias Current vs Temperature



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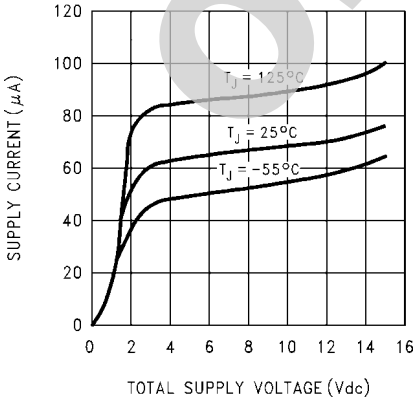
Supply Current vs Supply Voltage



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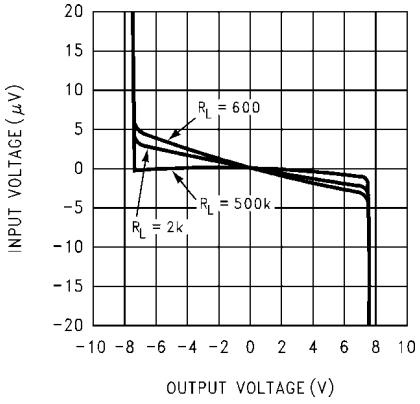
Input Voltage vs Output Voltage



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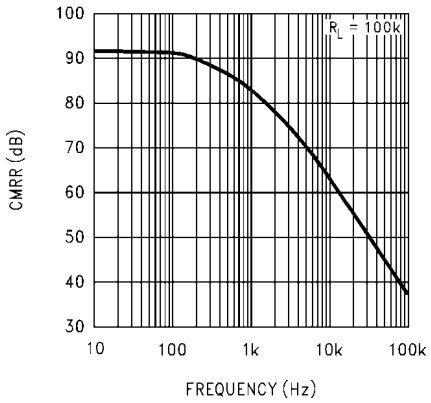
Common Mode Rejection Ratio vs Frequency



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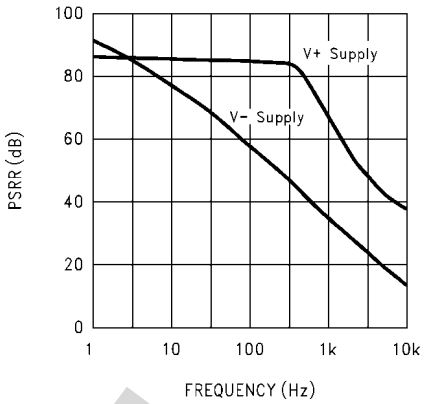
Power Supply Rejection Ratio vs Frequency



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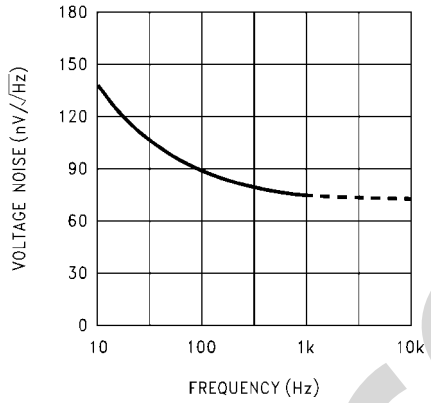
Input Voltage Noise vs Frequency



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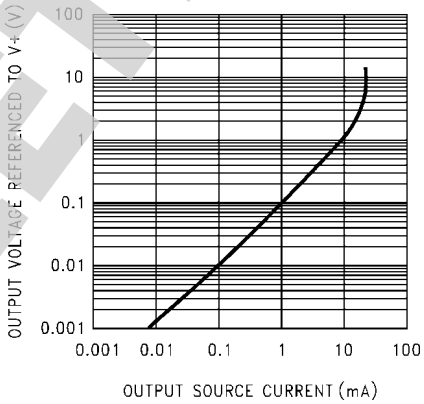
Output Characteristics Sourcing Current



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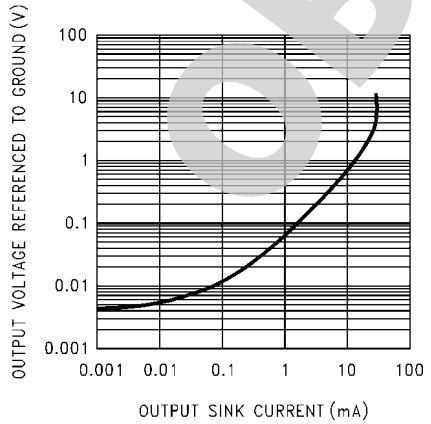
Output Characteristics Sinking Current



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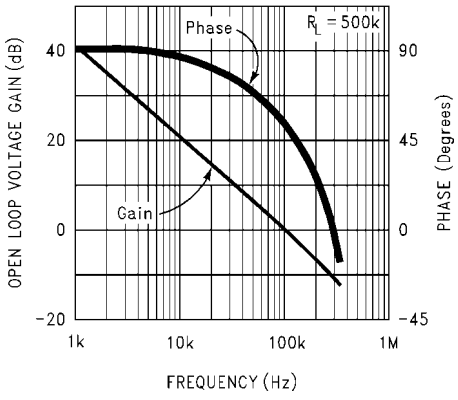
Gain and Phase Response vs Temperature (−55°C to +125°C)



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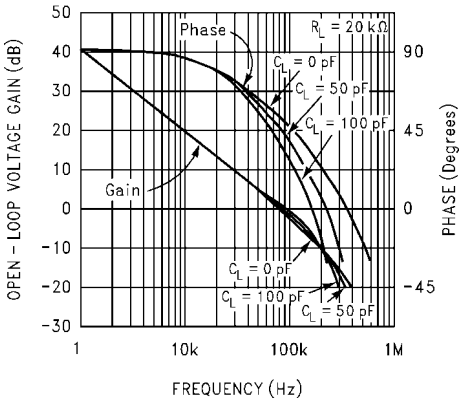
Gain and Phase Response vs Capacitive Load with R_L = 20 kΩ



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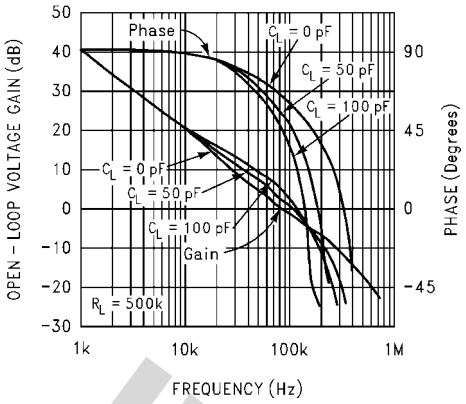
Gain and Phase Response vs Capacitive Load with R_L = 500 kΩ



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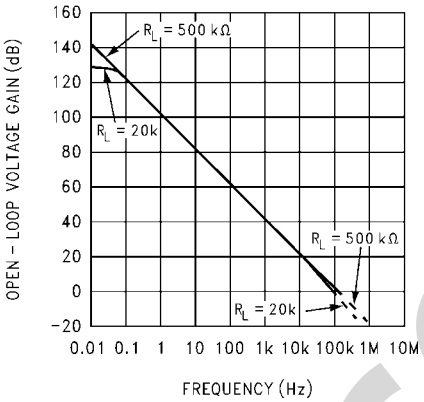
Open Loop Frequency Response



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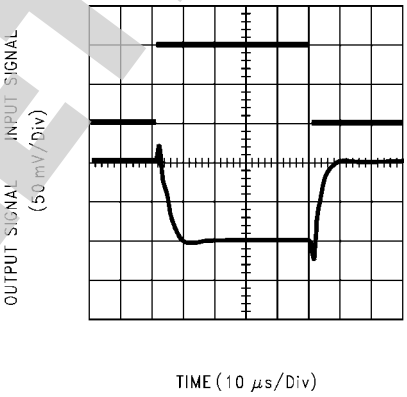
Inverting Small Signal Pulse Response



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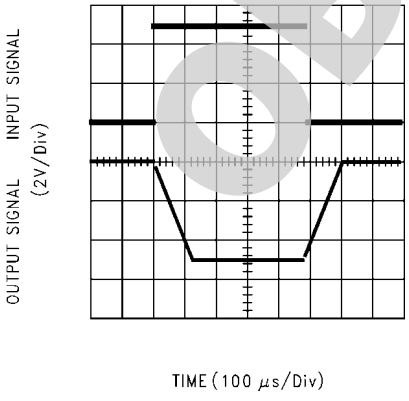
Inverting Large Signal Pulse Response



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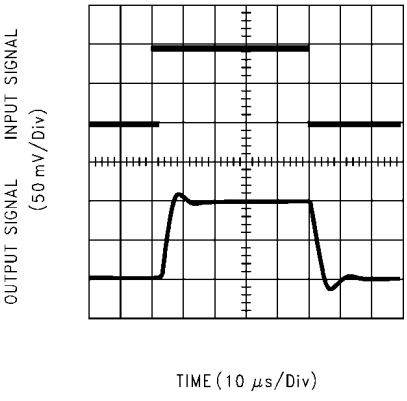
Non-Inverting Small Signal Pulse Response



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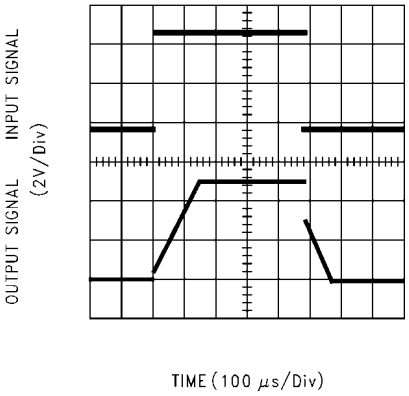
Non-Inverting Large Signal Pulse Response



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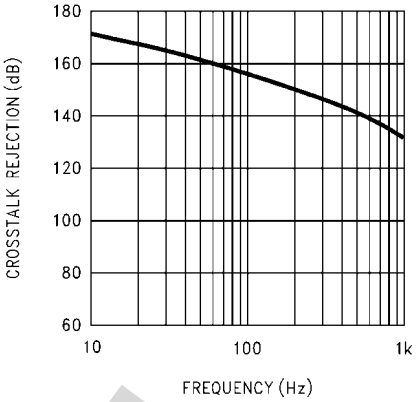
Crosstalk Rejection vs Frequency



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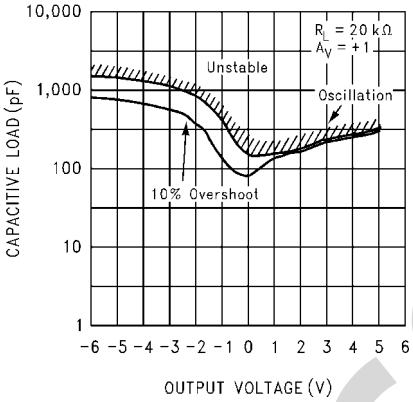
Stability vs Capacitive Load, R_L = 20 kΩ



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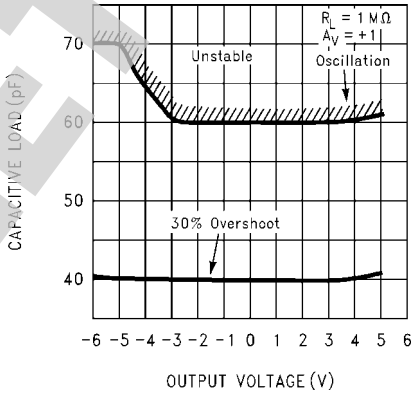
Stability vs Capacitive Load R_L = 1 MΩ



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Applications Hints

AMPLIFIER TOPOLOGY

The LMC6064EP incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6064EP both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6064EP.

Although the LMC6064EP is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6064EP is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See ***Printed-Circuit-Board Layout for High Impedance Work***).

The effect of input capacitance can be compensated for by adding a capacitor. Place a capacitor, C_f, around the feedback resistor (as in *Figure 1*) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 C_{IN} \leq R_2 C_f$$

Since it is often difficult to know the exact value of C_{IN}, C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and the LMC662 for a more detailed discussion on compensating for input capacitance.

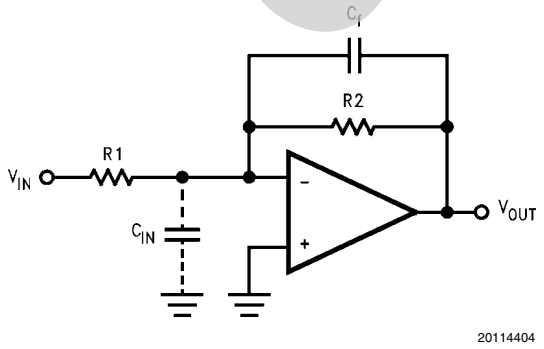


FIGURE 1. Canceling the Effect of Input Capacitance

CAPACITIVE LOAD TOLERANCE

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominate pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see typical curves).

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in *Figure 2*.

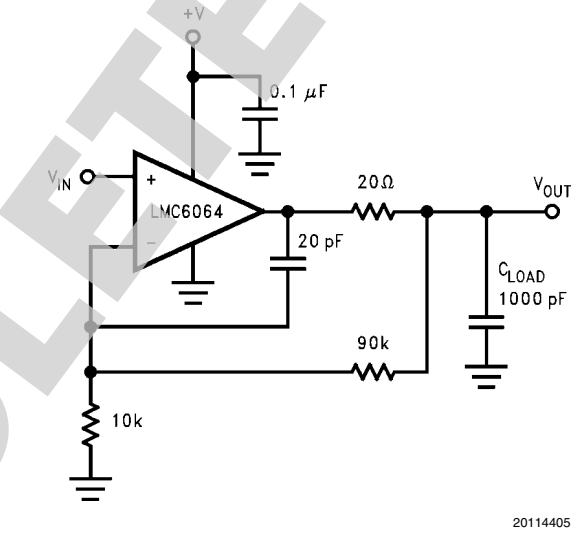


FIGURE 2. LMC6064EP Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of *Figure 2*, R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (*Figure 3*). Typically a pull up resistor conducting 10 µA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

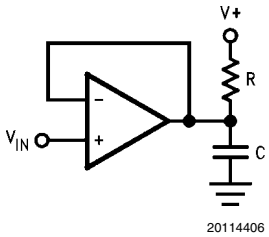


FIGURE 3. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6064EP, typically less than 10 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6064EP's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals etc. connected to the op-amp's inputs, as in *Figure 4*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6064EP's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See *Figure 5* for typical connections of guard rings for standard op-amp configurations.

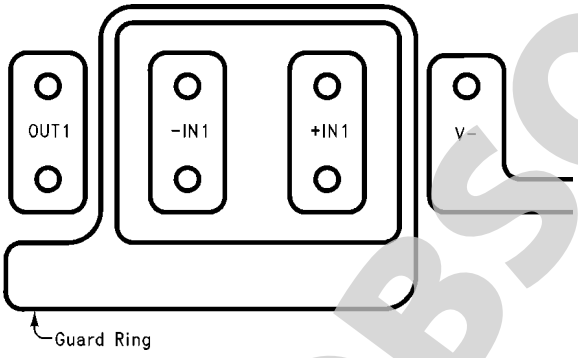


FIGURE 4. Example of Guard Ring in P.C. Board Layout

Latchup

CMOS devices tend to be susceptible to latchup due to their internal parasitic SCR effects. The (I/O) input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMC6064EP and LMC6082 are designed to withstand 100 mA surge current on the I/O pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the I/O pins. In addition, like an SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins will also inhibit latchup susceptibility.

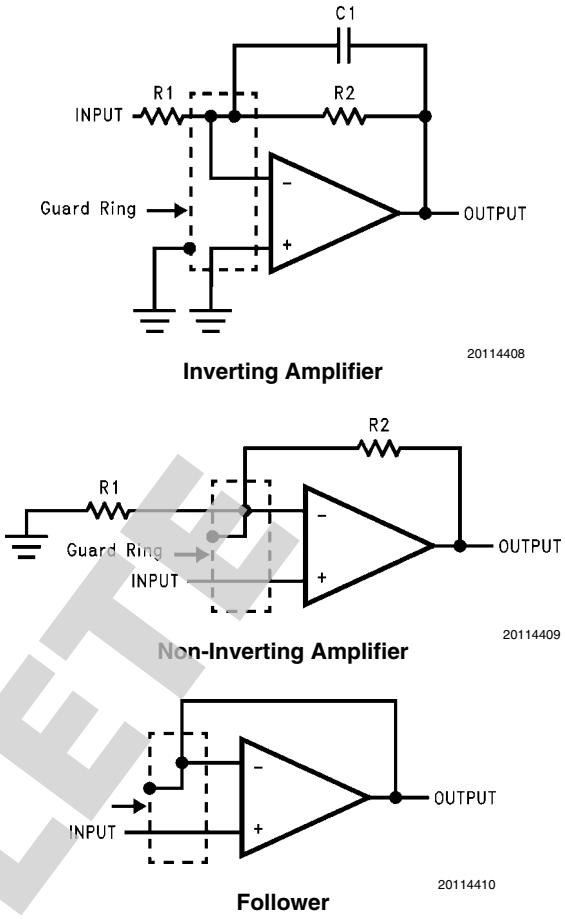
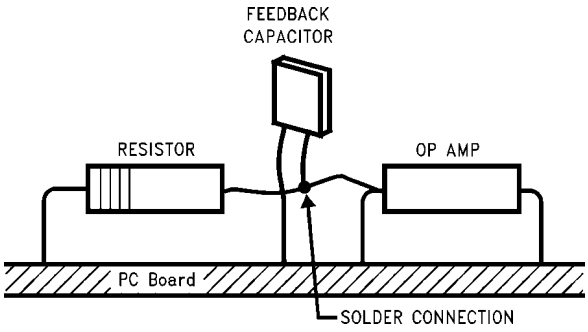


FIGURE 5. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 6*.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

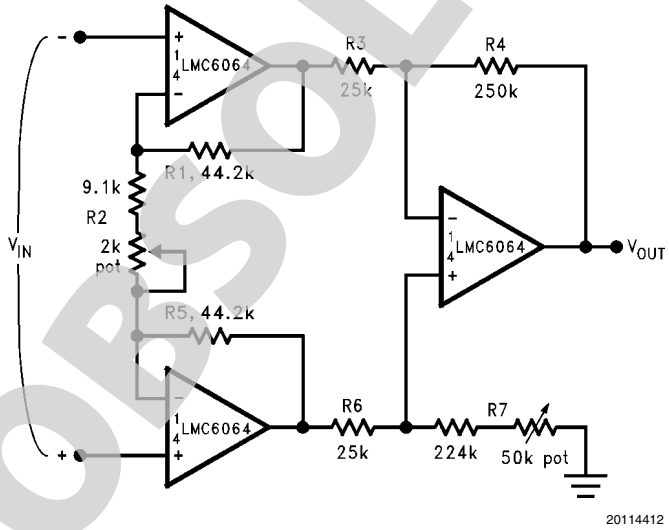
FIGURE 6. Air Wiring

Typical Single-Supply Applications

(V^+ = 5.0 V_{DC})

The extremely high input impedance, and low power consumption, of the LMC6064EP make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

Figure 7 shows an instrumentation amplifier that features high differential and common mode input resistance (>$10^{14}\Omega$), 0.01% gain accuracy at A_V = 100, excellent CMRR with 1 kΩ imbalance in bridge source resistance. Input current is less than 100 fA and offset drift is less than 2.5 µV/°C. R_2 provides a simple means of adjusting gain over a wide range without degrading CMRR. R_7 is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, low drift resistors should be used.



If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

$A_V \approx 100$ for circuit shown (R_2 = 9.822k).

FIGURE 7. Instrumentation Amplifier

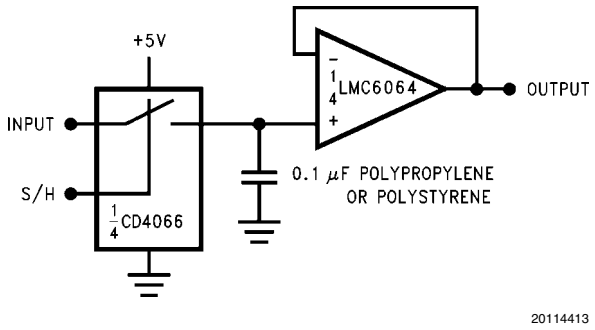


FIGURE 8. Low-Leakage Sample and Hold

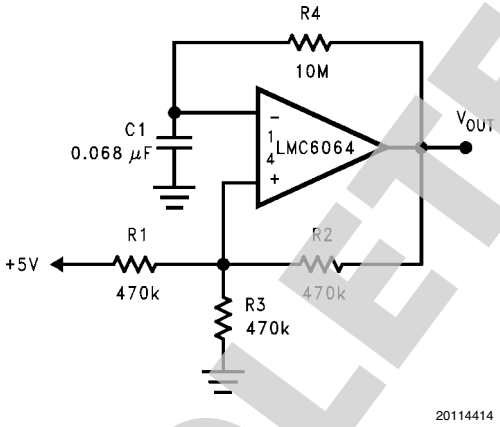


FIGURE 9. 1 Hz Square Wave Oscillator

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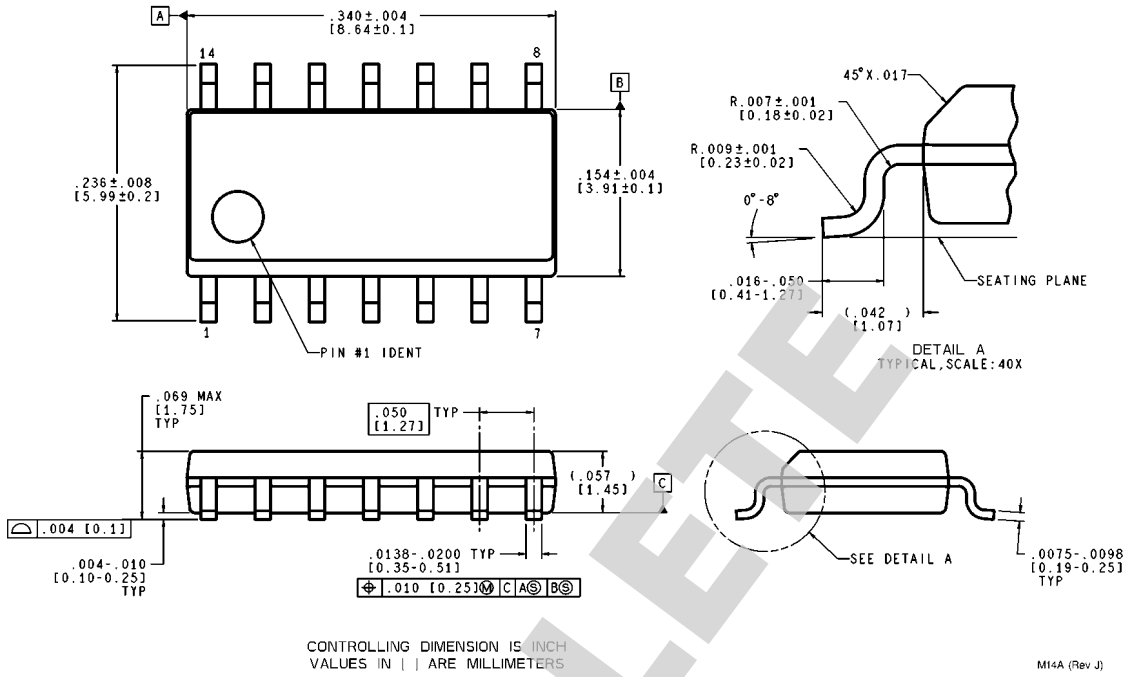
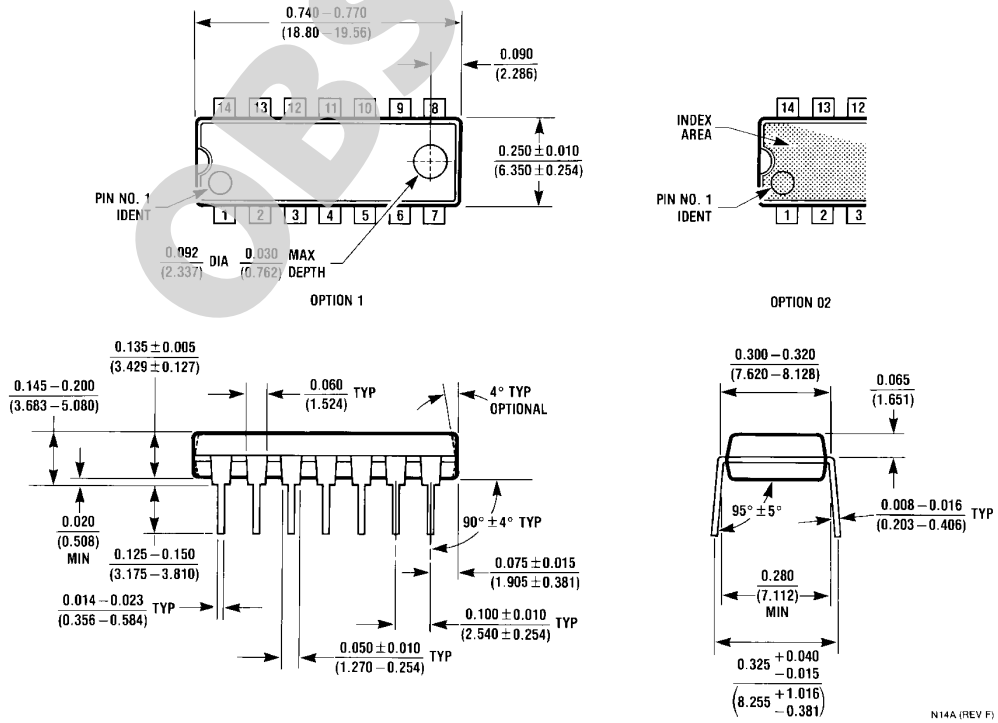
Physical Dimensions inches (millimeters) unless otherwise noted



14-Pin Small Outline Package
NS Package Number M14A



14-Pin Molded Dual-In-Line Package
NS Package Number N14A

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