# M62427FP

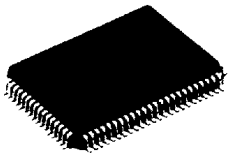
**SOUND QUALITY/SOUND FIELD CONTROL DIGITAL SOUND CONTROLLER FOR MINI-COMPONENT STEREO**

## DESCRIPTION

The M62427FP is an optimum digital sound controller IC for home audio.
This IC contains a 5-element graphic equalizer, master volume, sound and karaoke functions (voice cancel). It can control all of these functions with serial data.
In addition to the tone control function, this IC provides adapter pins for digital surround, microphone mixing and key control and is optimum to the sound quality and sound field control of audio equipment with karaoke function.

## FEATURES

- 80-pin QFP package
- Capable of performing the following functions with serial data
  - 5-band tone control (0, ±3, ±6, ±10dB)
  - Bass boost (HPF type) [ON/OFF] (PASS)
  - Surround (using external delay) [ON/OFF]
  - Vocal cancel (stereo) [ON/OFF]
  - Multilingual voice record switching [LCHonly/RCHonly]
  - Electronic volume 32 steps (0dB to -∞)
  - Port output 3 lines
- Supporting digital delay
- Adapter input/output supporting karaoke key control

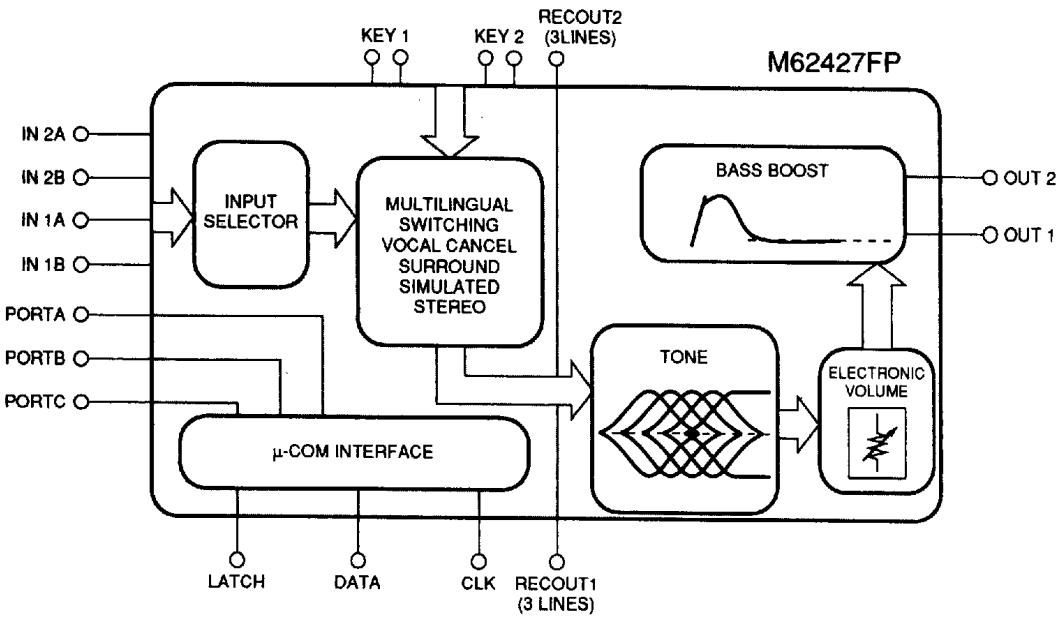


Outline 80P6N-A
0.8mm pitch QFP
(20.0mmX14.0mmX2.8mm)

## RECOMMENDED OPERATING CONDITIONS

Supply voltage range..... Vcc=±4.5 to ±7.5V

## SYSTEM CONFIGURATION



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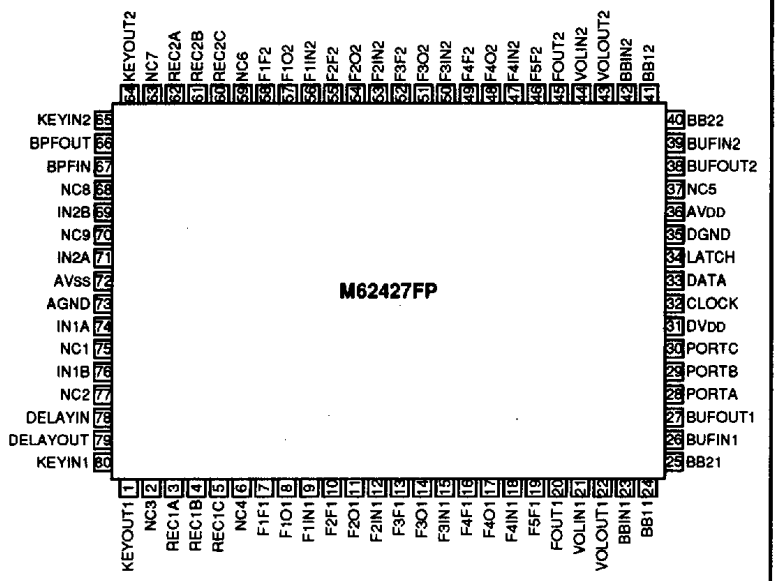
## PIN CONFIGURATION (TOP VIEW)




Outline 80P6N-A

NC:NO CONNECTION

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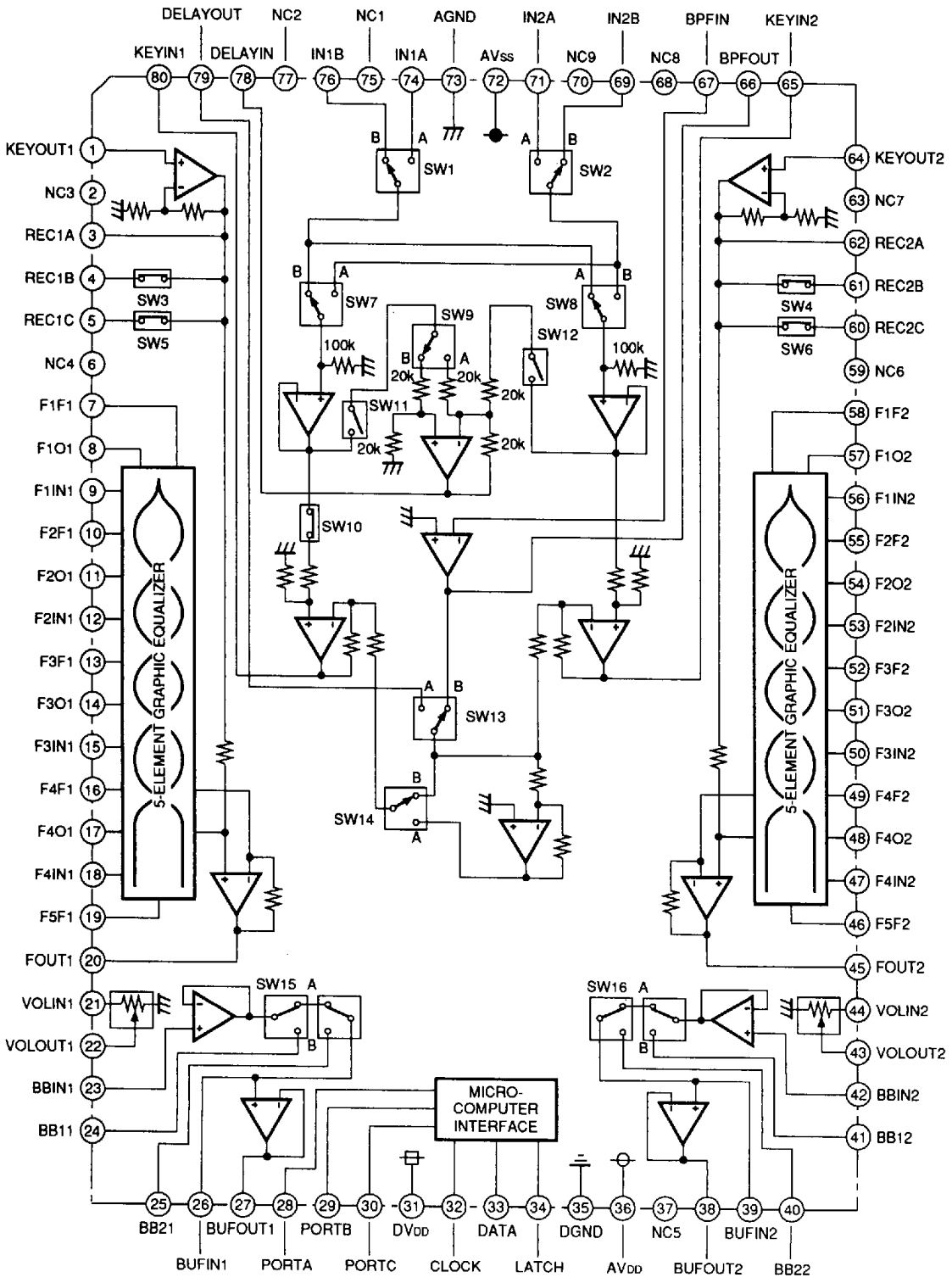
## IC INTERNAL BLOCK DIAGRAM



## SOUND QUALITY/SOUND FIELD CONTROL DIGITAL SOUND CONTROLLER FOR MINI-COMPONENT STEREO

### PIN DESCRIPTION

| Pin No. | Symbol | Function | |
|---|---|---|---|
| ⑫ | AVss | Load power pin of internal analog circuit | |
| ⑬ | AGND | Ground pin of internal analog circuit | |
| ⑭ ⑪ | IN1A, IN2A | Input pin of channel A | |
| ⑯ ⑨ | IN1B, IN2B | Input pin of channel B | |
| ⑱ | DELAYIN | (R-L) output pin for surround. Connect to the input of the delay circuit. Total load resistance is 20kΩ | |
| ⑲ | DELAYOUT | (R-L) input pin for surround. Connect to the output of the delay circuit. | |
| ⑳ ⑮ | KEYIN1, KEYIN2 | Key control adapter output pin. Connect to the input of the key control circuit. Total load resistance is 20kΩ | |
| ① ⑭ | KEYOUT1, KEYOUT2 | Key control adapter input pin. Connect to the output of the key control circuit. | |
| ⑱ | BPFOUT | Band pass filter amplifier output pin for vocal cancel | |
| ⑰ | BPFIN | Band pass filter amplifier input pin for vocal cancel | |
| ③ ⑫ | REC1A, REC2A | REC output pin A | Total load resistance is 20kΩ min. |
| ④ ⑪ | REC1B, REC2B | REC output pin B (with mute SW) | |
| ⑤ ⑩ | REC1C, REC2C | REC output pin C (with mute SW) | |
| ⑦ ⑧ | F1F1, F1F2 | (Band filter) connection pin of resonance impedance of the 1st element | |
| ⑧ ⑦ | F1O1, F1O2 | Output pin of resonance buffer amplifier of the 1st element | |
| ⑨ ⑥ | F1IN1, F1IN2 | Input pin of resonance buffer amplifier of the 1st element | |
| ⑩ ⑤ | F2F1, F2F2 | (Band filter) connection pin of resonance impedance of the 2nd element | |
| ⑪ ④ | F2O1, F2O2 | Output pin of resonance buffer amplifier of the 2nd element | |
| ⑫ ③ | F2IN1, F2IN2 | Input pin of resonance buffer amplifier of the 2nd element | |
| ⑬ ② | F3F1, F3F2 | (Band filter) connection pin of resonance impedance of the 3rd element | |
| ⑭ ① | F3O1, F3O2 | Output pin of resonance buffer amplifier of the 3rd element | |
| ⑮ ㊿ | F3IN1, F3IN2 | Input pin of resonance buffer amplifier of the 3rd element | |
| ⑯ ㊾ | F4F1, F4F2 | (Band filter) connection pin of resonance impedance of the 4th element | |
| ⑰ ㊽ | F4O1, F4O2 | Output pin of resonance buffer amplifier of the 4th element | |
| ⑱ ㊼ | F4IN1, F4IN2 | Input pin of resonance buffer amplifier of the 4th element | |
| ⑲ ㊻ | F5F1, F5F2 | Band filter connection pin of the 5th element | |
| ⑳ ㊺ | FOUT1, FOUT2 | Tone output pin. Connect to the next stage with capacitor connection | |
| ㉑ ㊹ | VOLIM1, VOLIN2 | R rudder volume input pin | |
| ㉒ ㊸ | VOLOUT1, VOLOUT2 | R rudder volume output pin | |
| ㉓ ㊷ | BBIN1, BBIN2 | Bass boost input pin | |
| ㉔ ㊶ | BB11, BB12 | Input pin for high pass filter connection of bass boost | |
| ㉕ ㊵ | BB21, BB22 | Output pin for high pass filter connection of bass boost | |
| ㉖ ㊴ | BUFIN1, BUFIN2 | Input pin of bass boost buffer amplifier | |
| ㉗ ㊳ | BUFOUT1, BUFOUT2 | Output pin of bass boost buffer amplifier | |
| ㉘ | PORTA | Output of port A | |
| ㉙ | PORTB | Output of port B | |
| ㉚ | PORTC | Output of port C | |
| ㉛ | DVDD | Power supply of internal logic circuit | |
| ㉜ | CLOCK | Clock input pin for serial data transfer | |
| ㉝ | DATA | Input pin of control data. Reads data at the rising edge of clock | |
| ㉞ | LATCH | Input pin of latch signal. Changes the circuit status at the rising edge of the latch signal | |
| ㉟ | DGND | Ground pin of the internal logic circuit | |
| ㊱ | AVDD | Positive power pin of the internal analog circuit | |
| ⑮ ⑩ | NC1, NC9 | Non-connection pin | |
| ⑰ ⑧ | NC2, NC8 | | |
| ② ⑬ | NC3, NC7 | | |
| ⑥ ⑨ | NC4, NC6 | | |
| ㊲ | NC5 | | |

SOUND QUALITY/SOUND FIELD CONTROL DIGITAL SOUND CONTROLLER FOR MINI-COMPONENT STEREO

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|---|---|---|---|---|
| $AV_{DD}$, AVss | Analog supply voltage | | ±7.8 | V |
| $DV_{DD}$ | Digital supply voltage | | 6.0 | V |
| Pd | Power dissipation | TA≤25°C | 1250 | mW |
| Kθ | Thermal derating | Ta>25°C Board installation (Note 1) | 12.5 | mW/°C |
| Topr | Operating temperature | | -20 to +55 | °C |
| Tstg | Storage temperature | | -55 to +125 | °C |

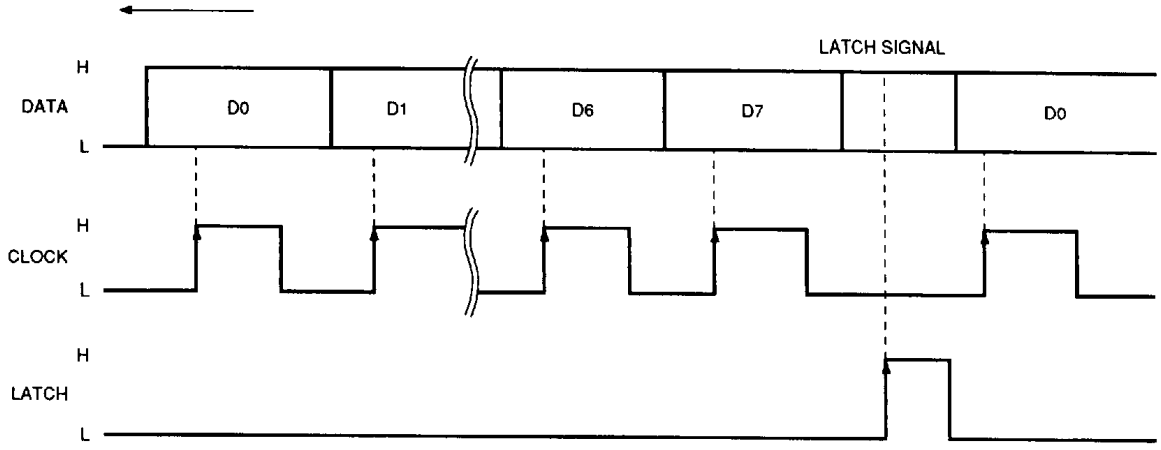
Note 1:Board
Size of printed circuit board (140mm x 140mm)
Thickness of printed circuit board (1.6mm)
Material of printed circuit board (Glass epoxy)
Single side Cu pattern Thickness of Cu (18μm)
Cu pattern dimensions (0.25mm (width) x 50mm (length)/lead)

## RECOMMENDED OPERATING CONDITIONS (Ta=25°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $AV_{DD}$ | Analog positive supply voltage | (Note 2) | 4.5 | 7.0 | 7.5 | V |
| AVss | Analog negative supply voltage | (Note 2) | -4.5 | -7.0 | -7.5 | V |
| $DV_{DD}$ | Digital supply voltage | $DV_{DD}$≤$AV_{DD}$ | 4.5 | 5.0 | 5.5 | V |
| VIH | Logic "H" level input voltage | | $DV_{DD}$-0.7 | – | $V_{DD}$ | V |
| VIL | Logic "L" level input voltage | | 0 | – | DGND+0.7 | V |

Note 2:After applying $AV_{DD}$, apply supply voltages in the order of AVss and $DV_{DD}$ for the IC.

## RELATIONSHIP BETWEEN DATA AND CLOCK




Data signal is read at the rising edge of clock.
Signal is latched at the rising edge of the latch signal.

## ELECTRICAL CHARACTERISTICS

(Ta=25°C, AVDD=7.0V, AVss =-7.0V, DVDD=5.0V, f=1kHz, unless otherwise noted. In addition, tone control bass boost is 0dB.)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| AIDD | Power supply | Analog positive power circuit current | With AVDD=7.0V and AVss=-7.0V, pin ㊱ pin current, when no signal is provided | 19 | 40 | 55 | mA |
| AIss | | Analog negative power circuit current | With AVDD=7.0V and AVss =-7.0V, pin ㉜ pin current, when no signal is provided | -55 | -40 | -19 | mA |
| DIDD | | Digital power circuit current | With DVDD=5V, pin ㉛ pin current, when no signal is provided | – | 0.3 | 1.2 | mA |
| RIN | Input/output | Input resistance | Pins ㉞, ㉖, ㉑ and ㉙, Ta=25°C | 100 | 200 | 300 | kΩ |
| VIM | | Maximum input voltage | (Input to pins ㉞ and ㉖), (input to pins ㉑ and ㉙) Output from pins ㉗ and ㉘, RL=10kΩ, THD=1% | 3.0 | 4.0 | – | Vrms |
| Vodc | | Output pin voltage | Pin ㉗, pin ㉘, when no signal is provided | -0.1 | 0 | 0.1 | V |
| Vrecdc | | | Pin ③, pin ⑫, when no signal is provided | -0.1 | 0 | 0.1 | V |
| Gv | | Pass gain | VIN=1Vrms, FLAT, (pins ㉞ and ㉖), gain between (pins ㉑ and ㉙) and (pins ㉗ and ㉘) | -20 | 0 | 2.0 | dB |
| Vono | | Output noise voltage | JIS-A filter, when no signal is provided, Rg=10kΩ, with FLAT (path), Pins ㉗ and ㉘ | – | 10.0 | 24 | μVrms |
| Vrecno | | | Pins ③ and ⑫ | – | 10.0 | 20 | μVrms |
| THD | | Distortion | Pin ㉗, pin ㉘, BW=400 to 30kHz VI=-20dBv, RL=10kΩ | – | 0.01 | 0.05 | % |
| THDrecA | | | Pin ③, pin ⑫, BW=400 to 30kHz VI=-20dBv, RL=30kΩ | – | 0.01 | 0.05 | % |
| THDrec B, C | | | (Pins ④ and ⑪), (pins ⑤ and ⑩), BW=400 to 30 kHz | – | 0.01 | 0.05 | % |
| CT | | Cross talk between channels | Vo=0.5Vrms, RL=10kΩ, JIS-A between pins ㉗ and ㉘, Rg=10kΩ | – | -55 | -45 | dB |
| CTrec | | | Vo=0.5Vrms, RL=30kΩ, JIS-A between pins ③ and ⑫, Rg=10kΩ | – | -55 | -45 | dB |
| Gboost1 | Tone control | Tone control voltage gain | 3dB, f=1kHz, Vo=1Vrms, Gain between input pins ①, ⑭ and output pins ⑳, ㊺ | 1.5 | 3 | 4.5 | dB |
| Gboost2 | | | 6dB | 4.5 | 6 | 7.5 | dB |
| Gboost3 | | | 9dB | 7.0 | 9 | 11.0 | dB |
| Gcut1 | | | -3dB | -4.5 | -3 | -1.5 | dB |
| Gcut2 | | | -6dB | -7.5 | -6 | -4.5 | dB |
| Gcut3 | | | -9dB | -11.0 | -9 | -7.0 | dB |
| BALton | | Balance between channels | f=1kHz, Vo=1Vrms, Input to pins ①, ⑭ Output from pins ⑳, ㊺, each boost With +10 and -10dB | -1.5 | 0 | +1.5 | dB |
| VPA | Port output | Port output | RL=10kΩ | 6.0 | 7.0 | – | V |
| VPB | | | | | | | |
| VPC | | | | | | | |

## DATA INPUT FORMAT

Four types of input formats can be selected by changing the D6/D7 slot setting status.

(Initialize all data of the four formats when power is turned on.)

← Input direction

Input format selection slot

(1)

| D01 | D11 | D21 | D31 | D41 | D51 | D6 | D7 |
|---|---|---|---|---|---|---|---|
| Rec out B SW3, 4 1:Mute 0:Through | Rec out C SW5, 6 1:Mute 0:Through | Voice switching mode SW7 1:Side A 0:Side B | SW8 1:Side A 0:Side B | SW9 1:Side A 0:Side B | SW10 1:ON 0:OFF | 0 | 0 |

(2)

| D02 | D12 | D22 | D32 | D42 | D52 | D6 | D7 |
|---|---|---|---|---|---|---|---|
| SW11, 12 1:ON 0:OFF | SW13 1:Side A 0:Side B | SW14 1:Side A 0:Side B | Port A 1:H 0:L | Port output Port B 1:H 0:L | Port C 1:H 0:L | 0 | 1 |

(3)

| D03 | D13 | D23 | D33 | D43 | D53 | D6 | D7 |
|---|---|---|---|---|---|---|---|
| * Refer to the slot setting list (5) for tone control<br>Bass boost SW15, 16 Side A/Side B | | | * Refer to the slot setting code list (6) for tone boost/cut | | | 1 | 0 |

(4)

| D04 | D14 | D24 | D34 | D44 | D54 | D6 | D7 |
|---|---|---|---|---|---|---|---|
| * Refer to the slot setting code list (7) for master volume | | | | | Input selector SW1, 2 1:Side A 0:Side B | 1 | 1 |

### (5) Setting code (tone control)

| | | D03 | D13 | D23 |
|---|---|---|---|---|
| Tone 1 (F1) | | 0 | 0 | 1 |
| Tone 2 (F2) | | 0 | 1 | 0 |
| Tone 3 (F3) | | 0 | 1 | 1 |
| Tone 4 (F4) | | 1 | 0 | 0 |
| Tone 5 (F5) | | 1 | 0 | 1 |
| Bass boost | OFF | 1 | 1 | 0 |
| | ON | 1 | 1 | 1 |

### (6) Setting code (tone boost/cut)

| | | D33 | D43 | D53 |
|---|---|---|---|---|
| Boost | +0dB | 0 | 0 | 0 |
| | +3dB | 0 | 0 | 1 |
| | +6dB | 0 | 1 | 0 |
| | +10dB | 0 | 1 | 1 |
| Cut | -0dB | 1 | 0 | 0 |
| | -3dB | 1 | 0 | 1 |
| | -6dB | 1 | 1 | 0 |
| | -10dB | 1 | 1 | 1 |

### (7) Setting codes (master volume)

| Amount of ATT | D04 | D14 | D24 | D34 | D44 |
|---|---|---|---|---|---|
| - 0.0dB | 0 | 0 | 0 | 0 | 0 |
| - 2.0dB | 1 | 0 | 0 | 0 | 0 |
| - 4.0dB | 0 | 1 | 0 | 0 | 0 |
| - 6.0dB | 1 | 1 | 0 | 0 | 0 |
| - 8.0dB | 0 | 0 | 1 | 0 | 0 |
| -10.0dB | 1 | 0 | 1 | 0 | 0 |
| -12.0dB | 0 | 1 | 1 | 0 | 0 |
| -14.0dB | 1 | 1 | 1 | 0 | 0 |
| -16.0dB | 0 | 0 | 0 | 1 | 0 |
| -18.0dB | 1 | 0 | 0 | 1 | 0 |
| -20.0dB | 0 | 1 | 0 | 1 | 0 |
| -22.0dB | 1 | 1 | 0 | 1 | 0 |
| -24.0dB | 0 | 0 | 1 | 1 | 0 |
| -26.0dB | 1 | 0 | 1 | 1 | 0 |
| -28.0dB | 0 | 1 | 1 | 1 | 0 |
| -30.0dB | 1 | 1 | 1 | 1 | 0 |
| -32.0dB | 0 | 0 | 0 | 0 | 1 |
| -34.0dB | 1 | 0 | 0 | 0 | 1 |
| -36.0dB | 0 | 1 | 0 | 0 | 1 |
| -38.0dB | 1 | 1 | 0 | 0 | 1 |
| -40.0dB | 0 | 0 | 1 | 0 | 1 |
| -42.0dB | 1 | 0 | 1 | 0 | 1 |
| -44.0dB | 0 | 1 | 1 | 0 | 1 |
| -48.0dB | 1 | 1 | 1 | 0 | 1 |
| -52.0dB | 0 | 0 | 0 | 1 | 1 |
| -56.0dB | 1 | 0 | 0 | 1 | 1 |
| -60.0dB | 0 | 1 | 0 | 1 | 1 |
| -64.0dB | 1 | 1 | 0 | 1 | 1 |
| -68.0dB | 0 | 0 | 1 | 1 | 1 |
| -72.0dB | 1 | 0 | 1 | 1 | 1 |
| -76.0dB | 0 | 1 | 1 | 1 | 1 |
| -∞ | 1 | 1 | 1 | 1 | 1 |

### (8) Port output setting codes

| Data | | Port output |
|---|---|---|
| D32 | 0 | Port A is set to L |
| | 1 | Port A is set to H |
| D42 | 0 | Port B is set to L |
| | 1 | Port B is set to H |
| D52 | 0 | Port C is set to L |
| | 1 | Port C is set to H |

### (9) Other setting codes

| Voice cancel | |
|---|---|
| D41=1 | SW9:Side A |
| D51=1 | SW10:ON |
| D02=1 | SW11, 12:ON |
| D12=0 | SW13:Side B |
| D22=0 | SW14:Side B |

| Sound | |
|---|---|
| D41=0 | SW9:Side B |
| D51=1 | SW10:ON |
| D02=1 | SW11, 12:ON |
| D12=1 | SW13:Side A |
| D22=1 | SW14:Side A |

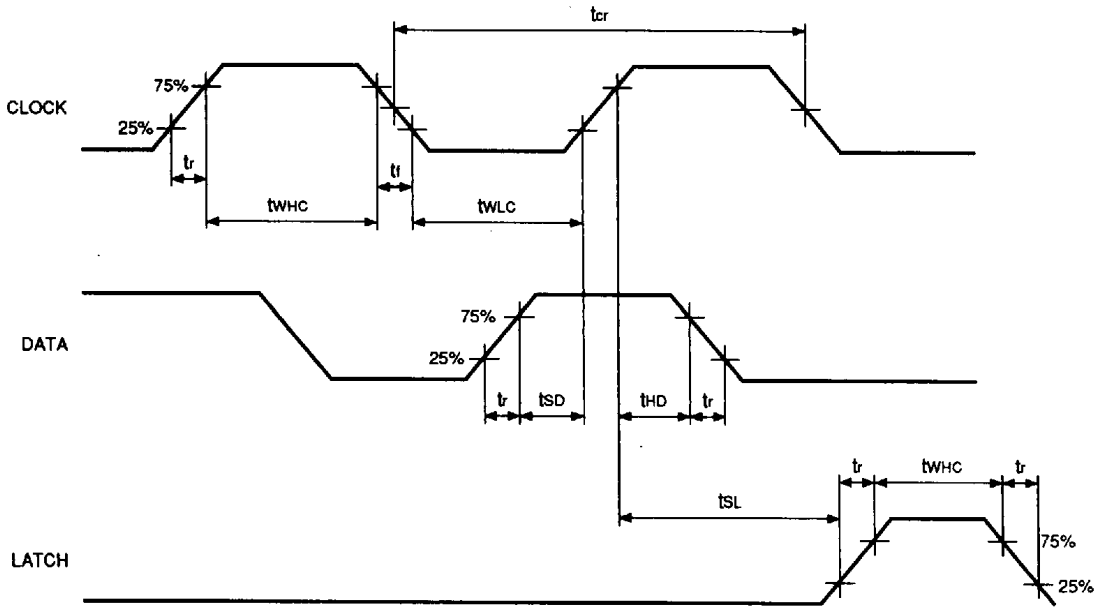
| Simulated stereo | |
|---|---|
| D41=1 | SW9:Side A |
| D51=0 | SW10:OFF |
| D02=1 | SW11, 12:ON |
| D12=0 | SW13:Side B |
| D22=0 | SW14:Side B |

| Multilingual record supported | | | |
|---|---|---|---|
| Rch (1ch) | | Lch (2ch) | |
| D21=0 | SW7:Side B | D21=1 | SW7:Side A |
| D31=1 | SW8:Side A | D31=0 | SW8:Side B |

## TIMING DEFINITION OF DIGITAL BLOCK

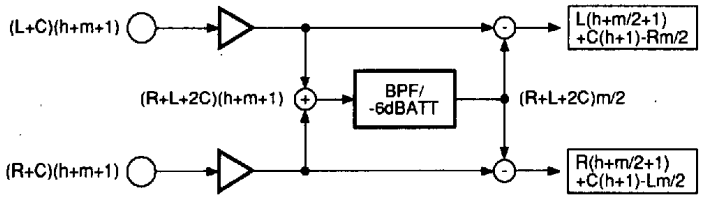
| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| $t_{cr}$ | Clock cycle time | 4 | – | – | µs |
| $t_{WHC}$ | Clock pulse width ("H" level) | 1.6 | – | – | µs |
| $t_{WLC}$ | Clock pulse width ("L" level) | 1.6 | – | – | µs |
| $t_r$ | Rising time of clock, data and latch | – | – | 0.4 | µs |
| $t_f$ | Falling time of clock, data and latch | – | – | 0.4 | µs |
| $t_{SD}$ | Data setup time | 0.8 | – | – | µs |
| $t_{HD}$ | Data hold time | 0.8 | – | – | µs |
| $t_{SL}$ | Latch setup time | 1 | – | – | µs |
| $t_{WHL}$ | Latch pulse width | 1.6 | – | – | µs |

## CLOCK AND DATA TIMINGS

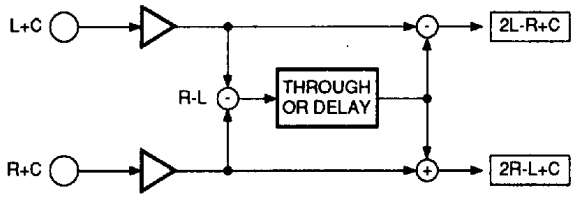


## FUNCTION DESCRIPTION

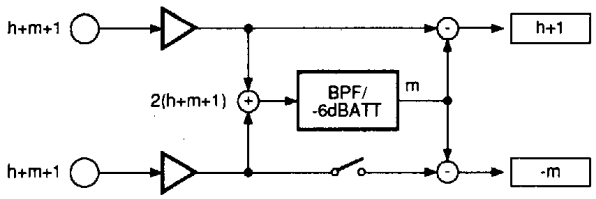
### (1) Equivalent circuit with vocal cancel



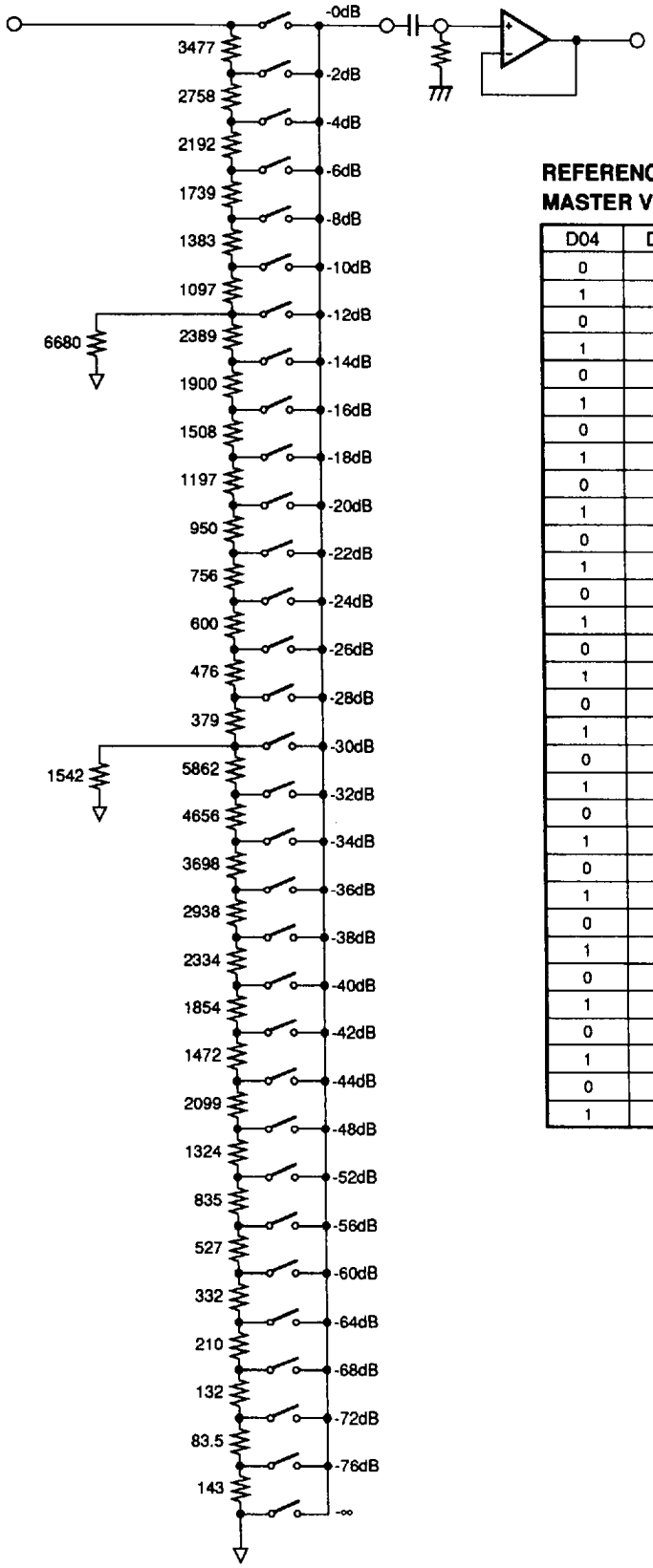

### (2) Equivalent circuit with surround




### (3) Equivalent circuit with simulated stereo



**(4) Master volume equivalent circuit**




**REFERENCE VALUES FOR MASTER VOLUME ATTENUATION**

| D04 | D14 | D24 | D34 | D44 | Amount of ATT |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | - 0.0dB |
| 1 | 0 | 0 | 0 | 0 | - 2.0dB |
| 0 | 1 | 0 | 0 | 0 | - 4.0dB |
| 1 | 1 | 0 | 0 | 0 | - 6.0dB |
| 0 | 0 | 1 | 0 | 0 | - 8.0dB |
| 1 | 0 | 1 | 0 | 0 | -10.0dB |
| 0 | 1 | 1 | 0 | 0 | -12.0dB |
| 1 | 1 | 1 | 0 | 0 | -14.0dB |
| 0 | 0 | 0 | 1 | 0 | -16.0dB |
| 1 | 0 | 0 | 1 | 0 | -18.0dB |
| 0 | 1 | 0 | 1 | 0 | -20.0dB |
| 1 | 1 | 0 | 1 | 0 | -22.0dB |
| 0 | 0 | 1 | 1 | 0 | -24.0dB |
| 1 | 0 | 1 | 1 | 0 | -26.0dB |
| 0 | 1 | 1 | 1 | 0 | -28.0dB |
| 1 | 1 | 1 | 1 | 0 | -30.0dB |
| 0 | 0 | 0 | 0 | 1 | -32.0dB |
| 1 | 0 | 0 | 0 | 1 | -34.0dB |
| 0 | 1 | 0 | 0 | 1 | -36.0dB |
| 1 | 1 | 0 | 0 | 1 | -38.0dB |
| 0 | 0 | 1 | 0 | 1 | -40.0dB |
| 1 | 0 | 1 | 0 | 1 | -42.0dB |
| 0 | 1 | 1 | 0 | 1 | -44.0dB |
| 1 | 1 | 1 | 0 | 1 | -48.0dB |
| 0 | 0 | 0 | 1 | 1 | -52.0dB |
| 1 | 0 | 0 | 1 | 1 | -56.0dB |
| 0 | 1 | 0 | 1 | 1 | -60.0dB |
| 1 | 1 | 0 | 1 | 1 | -64.0dB |
| 0 | 0 | 1 | 1 | 1 | -68.0dB |
| 1 | 0 | 1 | 1 | 1 | -72.0dB |
| 0 | 1 | 1 | 1 | 1 | -76.0dB |
| 1 | 1 | 1 | 1 | 1 | -∞ |

### (5) Equivalent circuit of tone control resonance circuit block

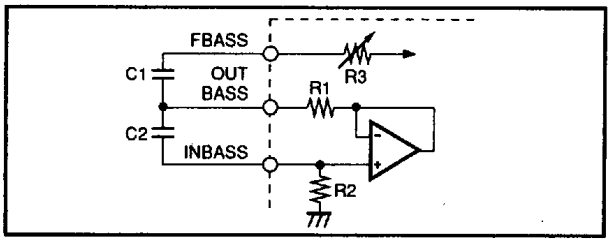



**Fig.1 Internal resonance equivalent circuit**

Center frequency

$fo=1/2\pi \sqrt{C1 \cdot C2 \cdot R1 \cdot R2}$ (Hz)

$Q=\sqrt{(C2 \cdot R2)/(C1 \cdot R1)}$

(Example) Bass band (f=150Hz)

R1=1.5kΩ, R2=56kΩ

C1=1.5μ, C2=0.01μ

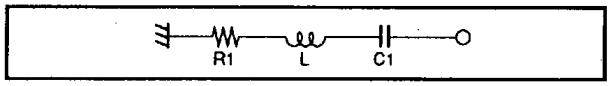
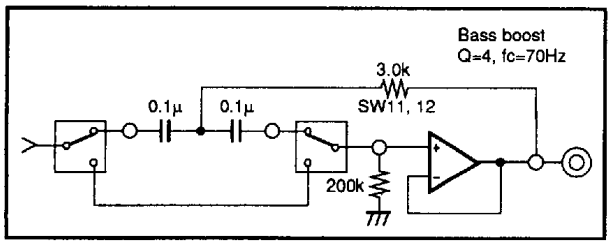


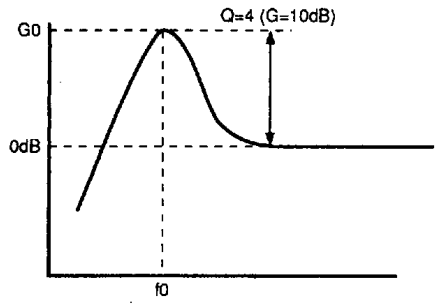

**Fig.2 Equivalent circuit using I**

Figure 1 means Figure 2 in equivalence. The part constant is converted by the following formula.

$L=C2 \cdot R1 \cdot R2$

### (6) Equivalent circuit of bass boost circuit block



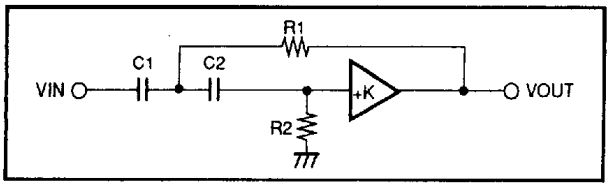




**Fig.3 Positive feedback type secondary high pass filter circuit of bass boost block**

Amplitude characteristics of secondary high pass filter(forreference)

| Q | G0 |
|---|---|
| 1 | 0 to 1dB |
| 2 | 6 dB |
| 4 | 10 dB |
| 5 | 13 dB |
| 10 | 20 dB |

The transmission function is given by the following formula.

$$\frac{V_{OUT}}{V_{IN}} = \frac{Ks^2}{S^2+S\left[\frac{1}{R2C1}+\frac{1}{R2C2}+(1-K)\frac{1}{R1C1}\right]+\frac{1}{R1R2C1C2}}$$

$$\omega 0^2 = \frac{1}{R1R2C1C2}$$

$$Q = \frac{1}{\sqrt{\frac{R1C1}{R2C2}}+\sqrt{\frac{R1C2}{R2C1}}+(1-K)\sqrt{\frac{R2C2}{R1C1}}}$$

The bass boost block consists of the positive feedback type secondary high pass circuit shown in Figure 3.

A design calculation example of the bass boost block is shown below.

If C1=C2=Cf and K=+1 are assumed, the following are found with the above formula.

Rf=1/(ω0Cf).....(1)

R1=Rf/2Q.....(2)

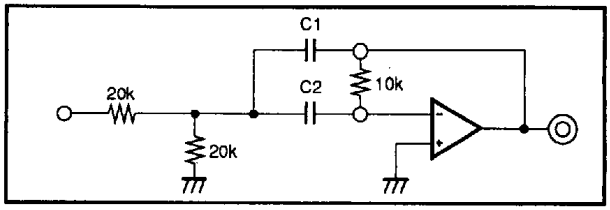
R2=2QRf.....(3)

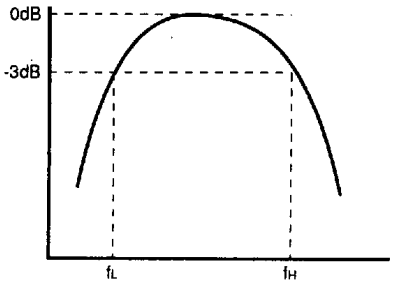
If the cut-off frequency is 70Hz, and Q is 4, ω0=2π X 70Hz, and Q=4 are assumed.

With C1=C2=Cf=0.1μF, R1 and R2 are approximately 3.0kΩ and 200kΩ, respectively, because of (1), (2) and (3).

Rf=22.7kΩ
R1=2.84kΩ
R2=182kΩ

### (7) Equivalent circuit of band pass filter block



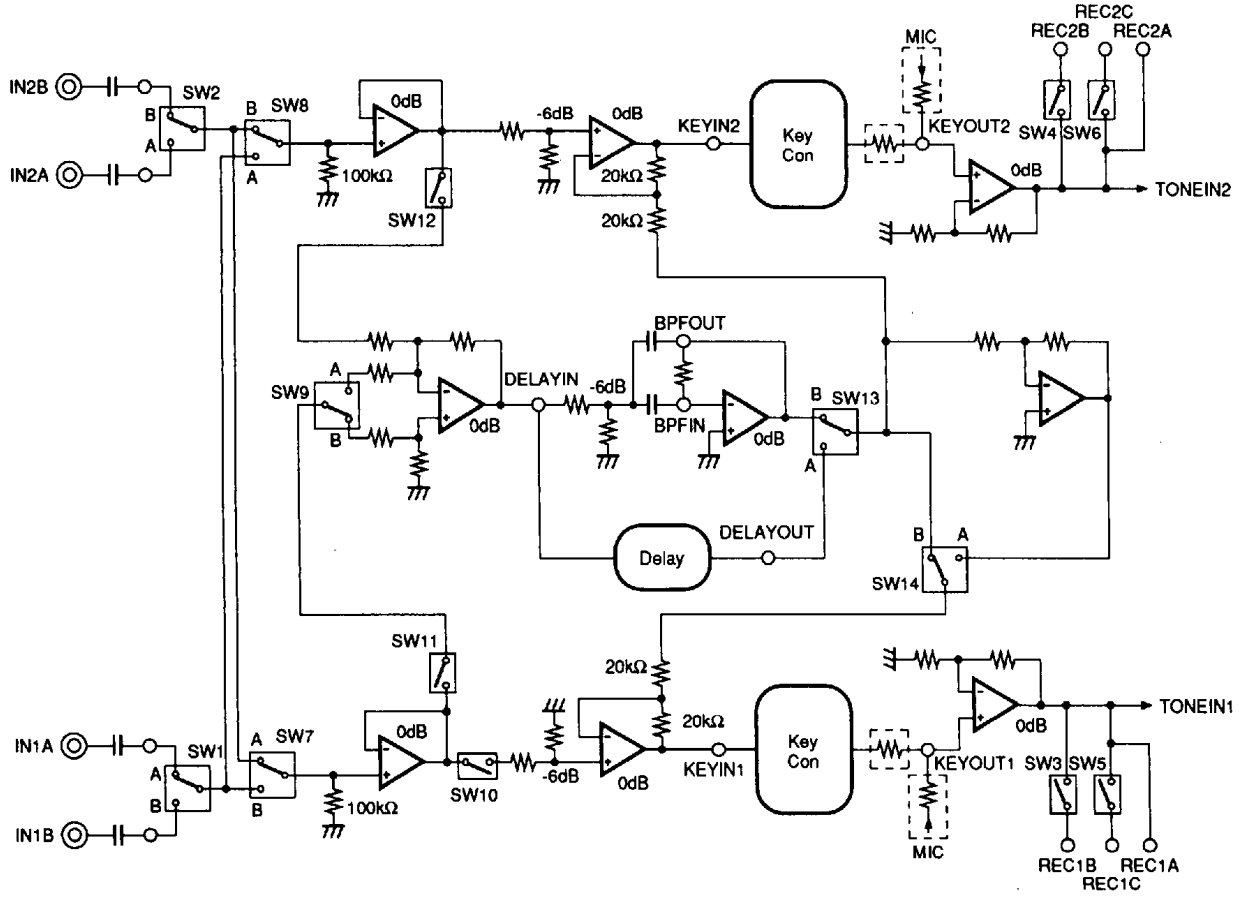




(Band pass filter design formula)

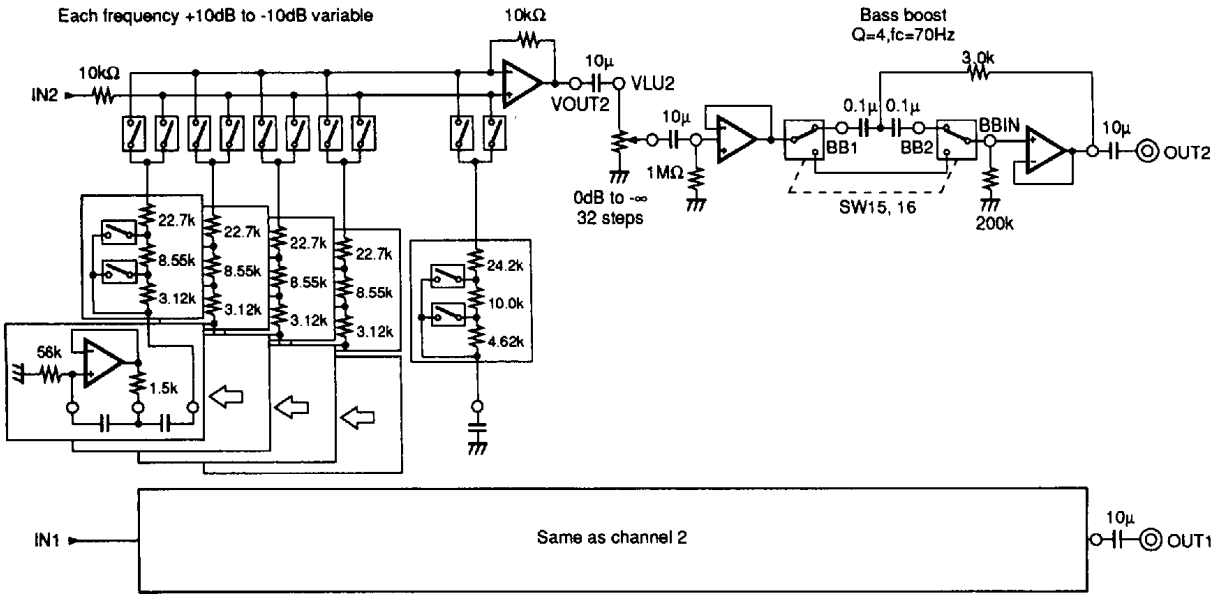
$f_H$ (Cut-off frequency at side H)$=\frac{1}{2\pi C1 \cdot 10k}$

$f_L$ (Cut-off frequency at side L)$=\frac{1}{2\pi C2 \cdot 10k}$

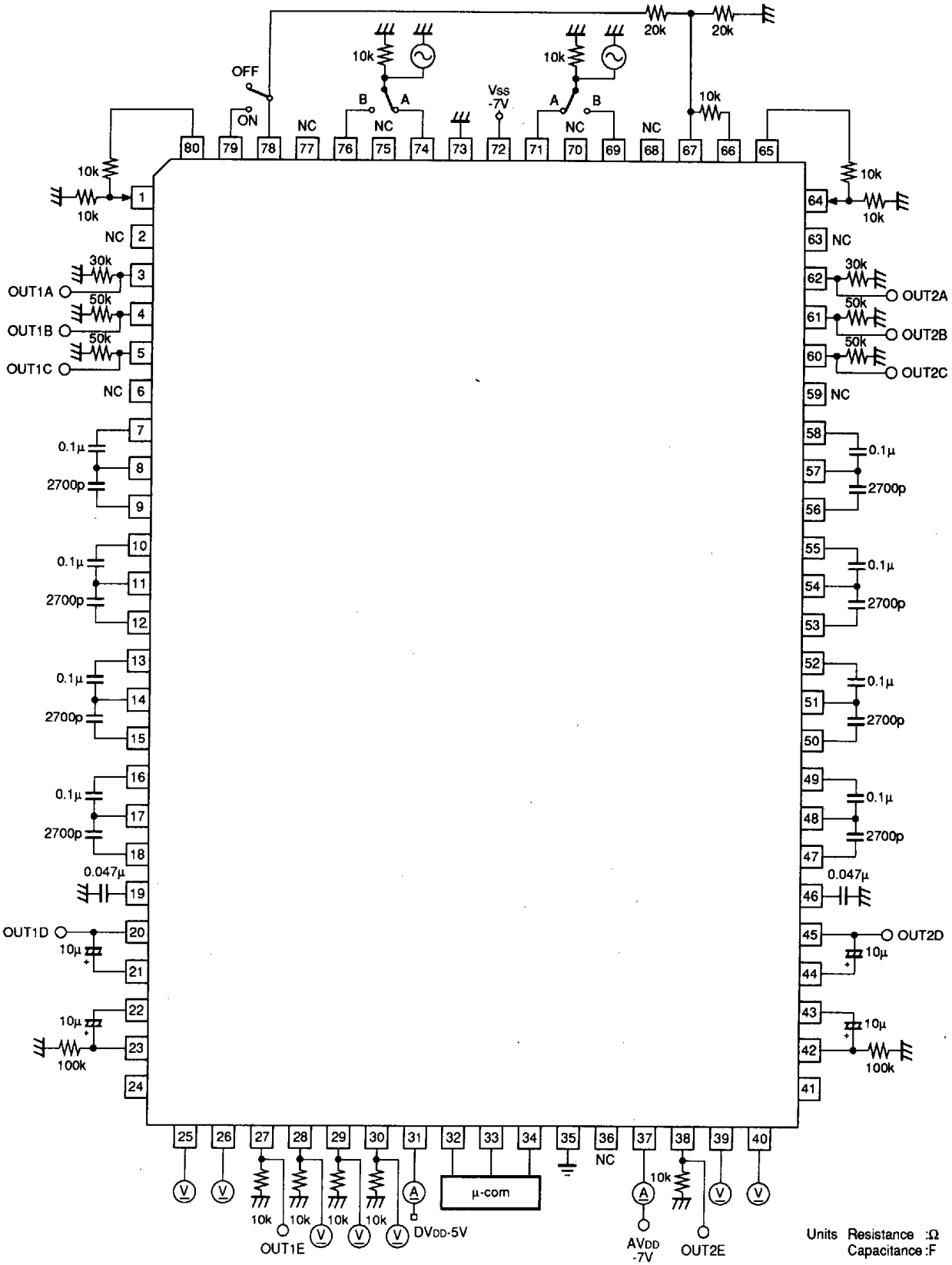
## SIGNAL TRANSMISSION BLOCK DIAGRAM (1)




## SIGNAL TRANSMISSION BLOCK DIAGRAM (2)

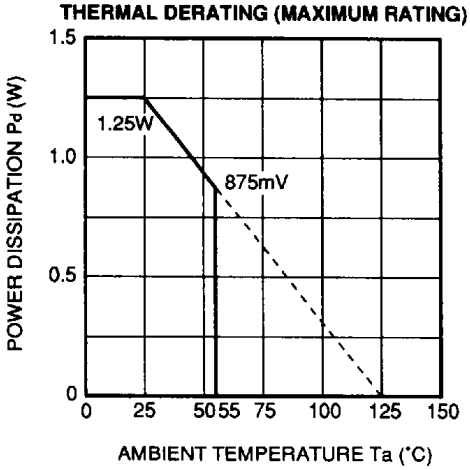


## TEST CIRCUIT

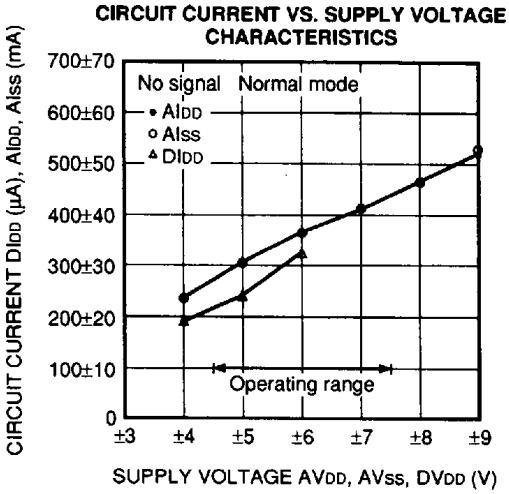


## TYPICAL CHARACTERISTICS

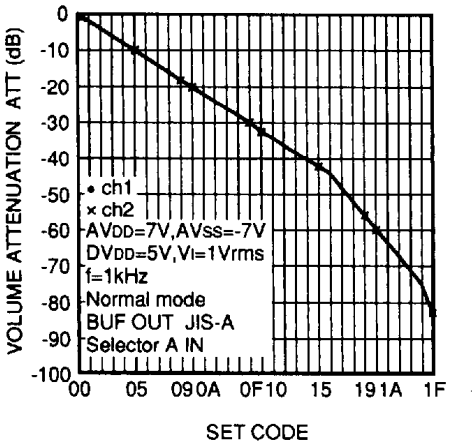
THERMAL DERATING (MAXIMUM RATING)



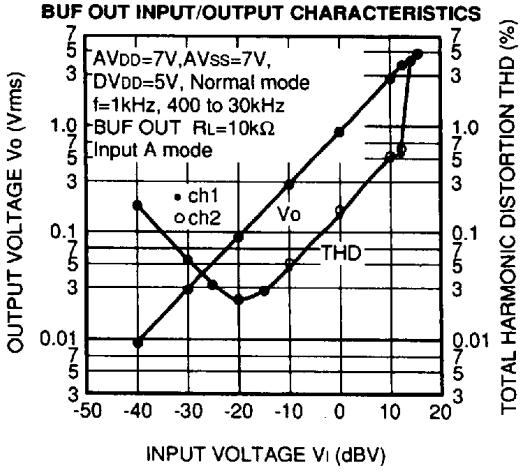

CIRCUIT CURRENT VS. SUPPLY VOLTAGE CHARACTERISTICS



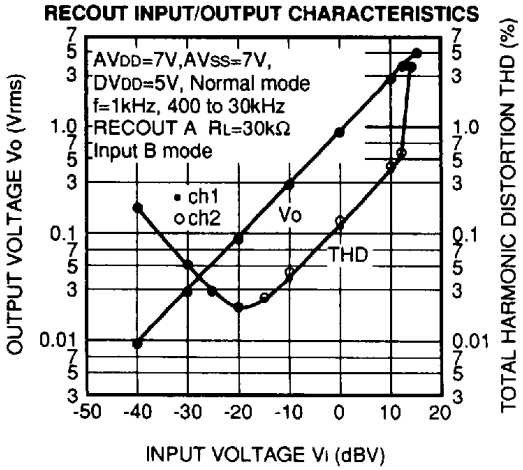

VOLUME CONTROL CHARACTERISTICS



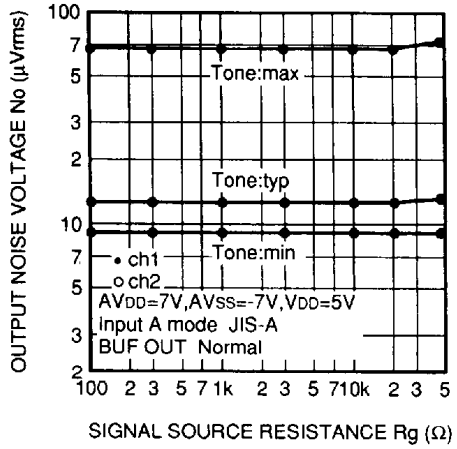

BUF OUT INPUT/OUTPUT CHARACTERISTICS



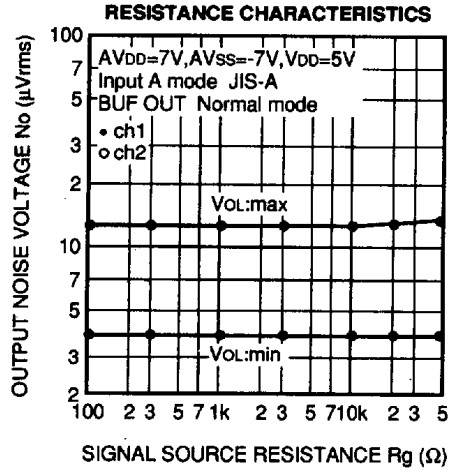

RECOUT INPUT/OUTPUT CHARACTERISTICS



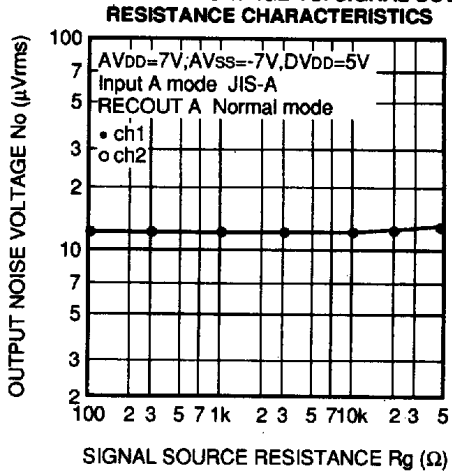

OUTPUT NOISE VOLTAGE VS. SIGNAL SOURCE RESISTANCE CHARACTERISTICS



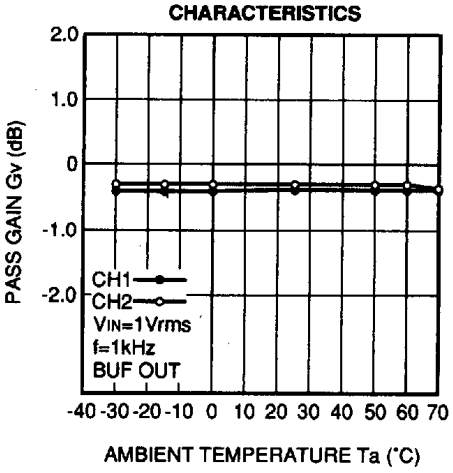
**OUTPUT NOISE VOLTAGE VS. SIGNAL SOURCE RESISTANCE CHARACTERISTICS**



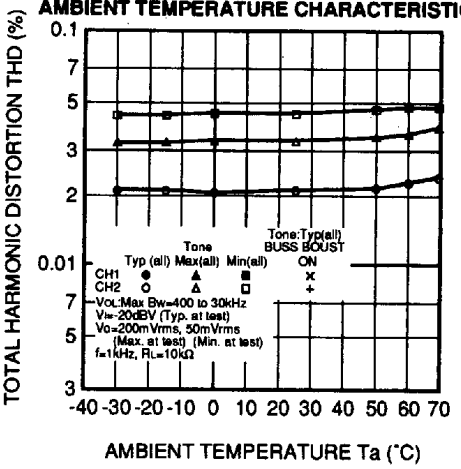

**OUTPUT NOISE VOLTAGE VS. SIGNAL SOURCE RESISTANCE CHARACTERISTICS**



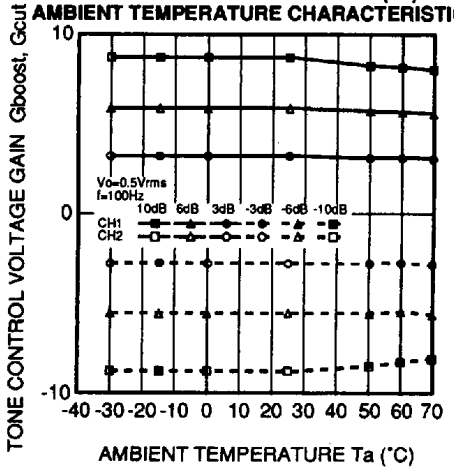

**PASS GAIN VS. AMBIENT TEMPERATURE CHARACTERISTICS**



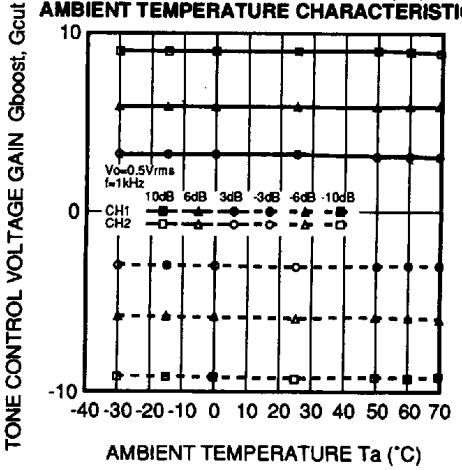

**TOTAL HARMONIC DISTORTION (BUF OUT) VS. AMBIENT TEMPERATURE CHARACTERISTICS**



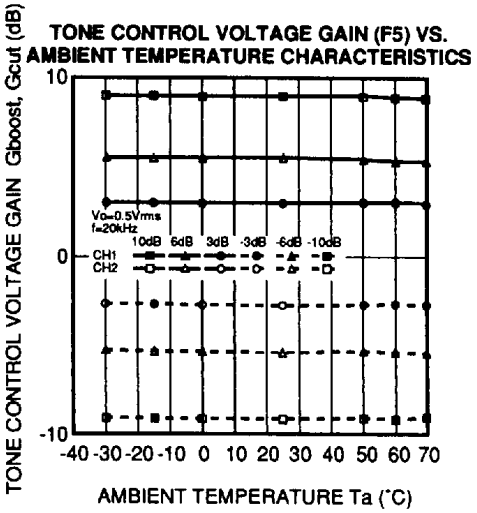

**TONE CONTROL VOLTAGE GAIN (F1) VS. AMBIENT TEMPERATURE CHARACTERISTICS**




**TONE CONTROL VOLTAGE GAIN (F3) VS. AMBIENT TEMPERATURE CHARACTERISTICS**

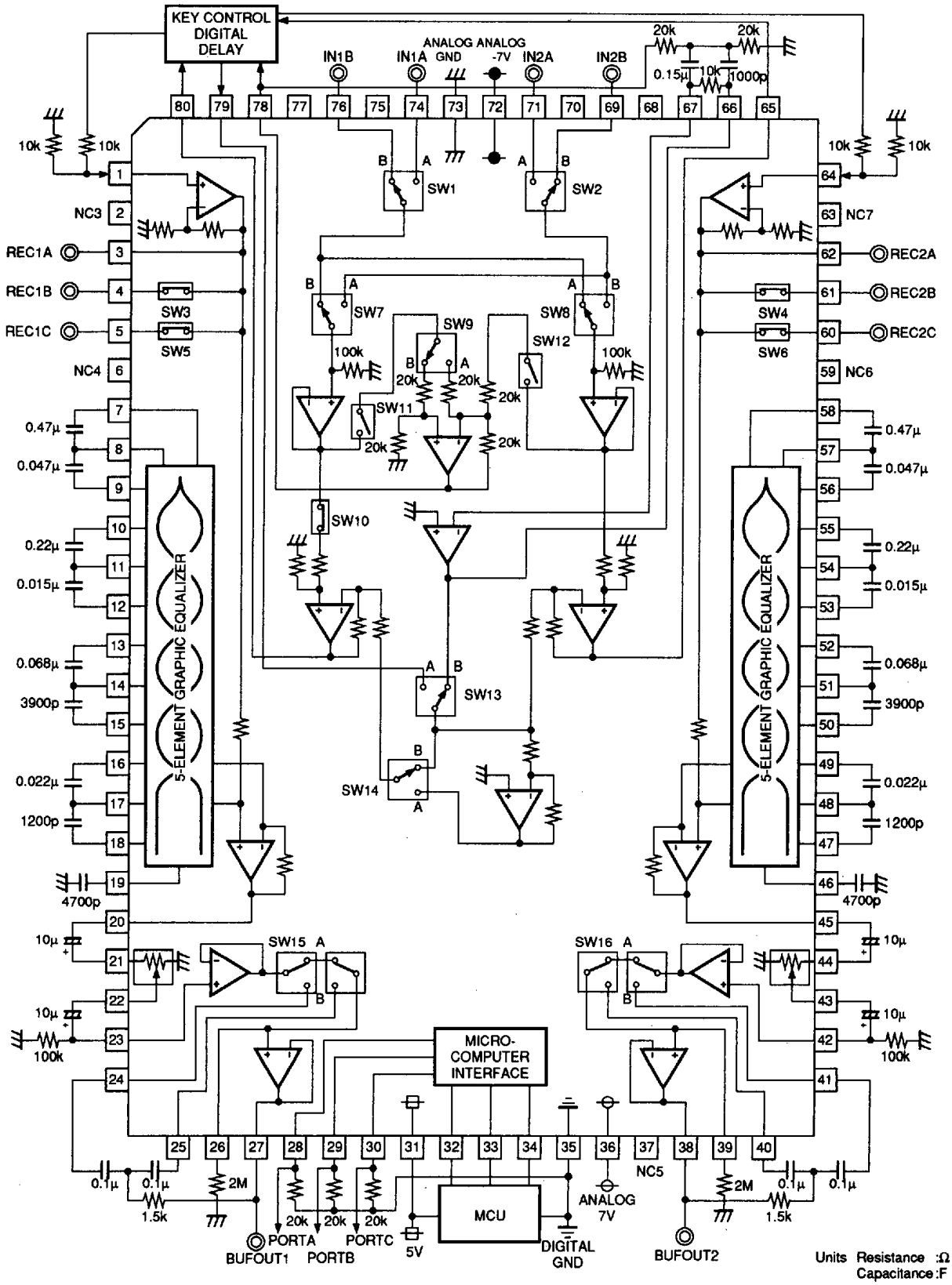


TONE CONTROL VOLTAGE GAIN (F5) VS. AMBIENT TEMPERATURE CHARACTERISTICS

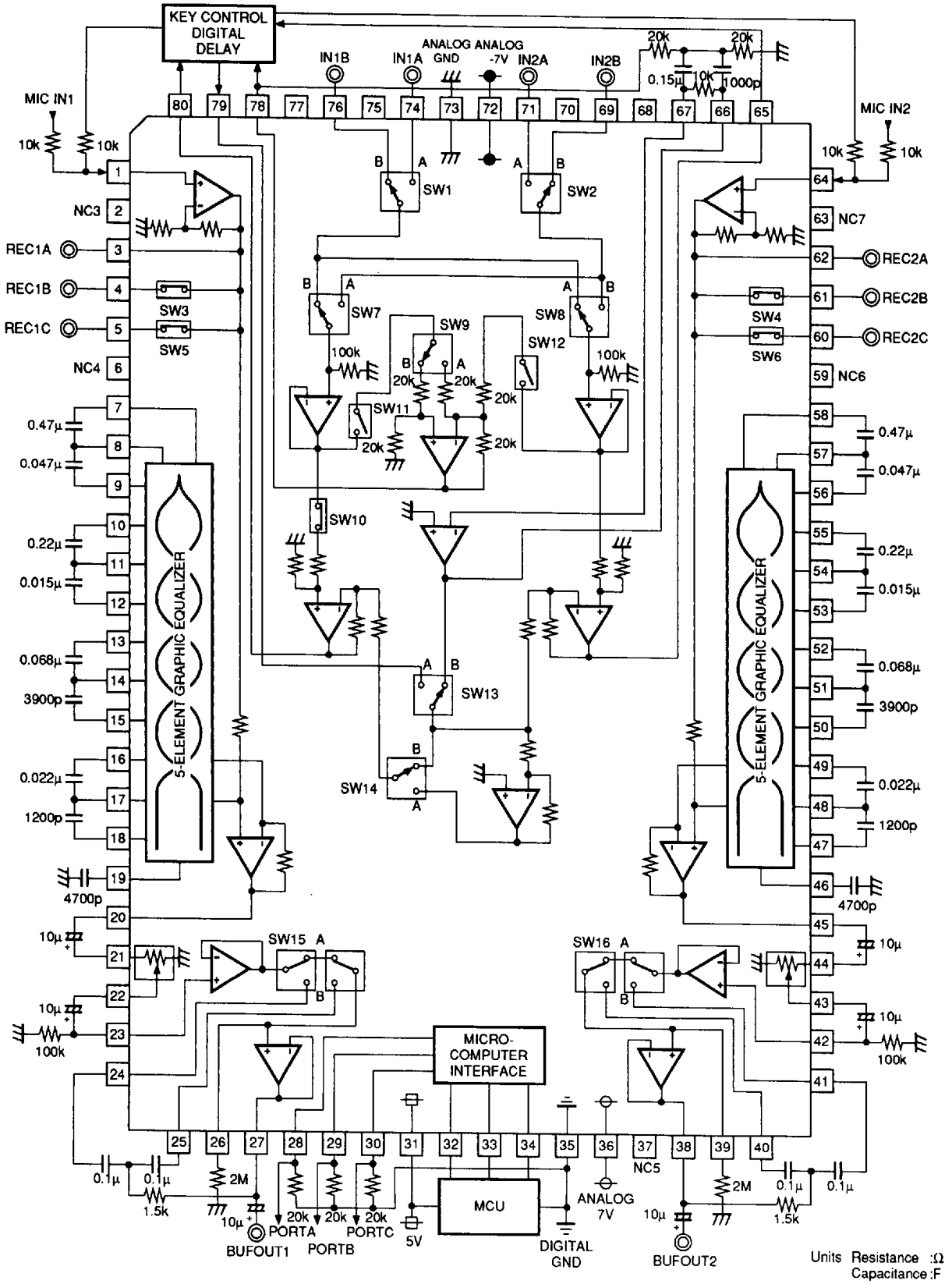


SOUND QUALITY/SOUND FIELD CONTROL DIGITAL SOUND CONTROLLER FOR MINI-COMPONENT STEREO

## APPLICATION EXAMPLE 1



## APPLICATION EXAMPLE 2



**APPLICATION EXAMPLE 3** (Single power supply)