

Preliminary - August 7, 2000

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## DESCRIPTION

The SC1158 is a low-cost, full featured, synchronous voltage-mode controller designed for use in single ended power supply applications where efficiency is of primary concern. Synchronous operation allows for the elimination of heat sinks in many applications. The SC1158 is ideal for implementing DC/DC converters needed to power advanced microprocessors such as Pentium® II and K6-2. Internal level-shift, high-side drive circuitry, and preset shoot-thru control, allows for use of inexpensive N-channel power switches.

SC1158 features include an integrated 4-bit  $V_{ID}$  DAC, temperature compensated voltage reference, triangle wave oscillator, current limit comparator, frequency shift over-current protection, and an internally compensated error amplifier.

The SC1158 operates at a fixed 140KHz, providing an optimum compromise between efficiency, external component size, and cost.

## FEATURES

- Low cost / full featured
- Synchronous operation
- 4 Bit  $V_{ID}$  DAC programmable output (1% tolerance)
- Meets Intel VRM8.2 (Pentium® II) high range
- 1.5% Reference

## APPLICATIONS

- Pentium® II, K6-2 Core Supplies
- Multiple Microprocessor Supplies
- Voltage Regulator Modules (VRM)
- Programmable Power Supplies
- High Efficiency DC/DC Conversion

## ORDERING INFORMATION

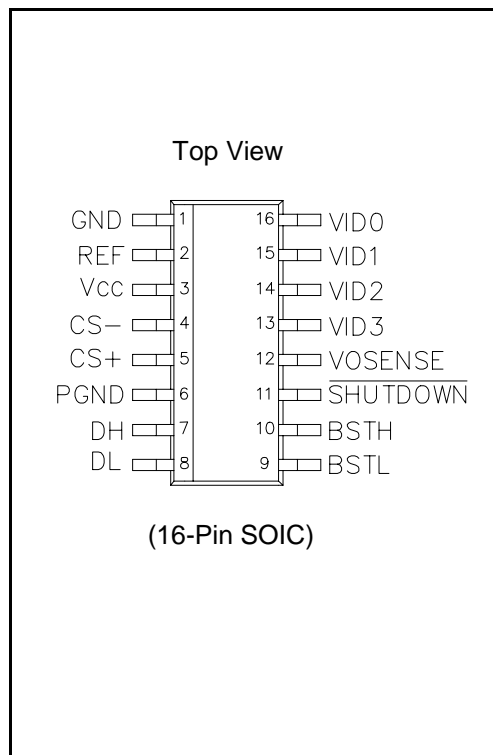
DEVICE <sup>(1)</sup>	PACKAGE <sup>(2)</sup>	TEMP. RANGE (T <sub>J</sub> )
SC1158CS.TR	SO-16NB	0 - 125°C

Note:

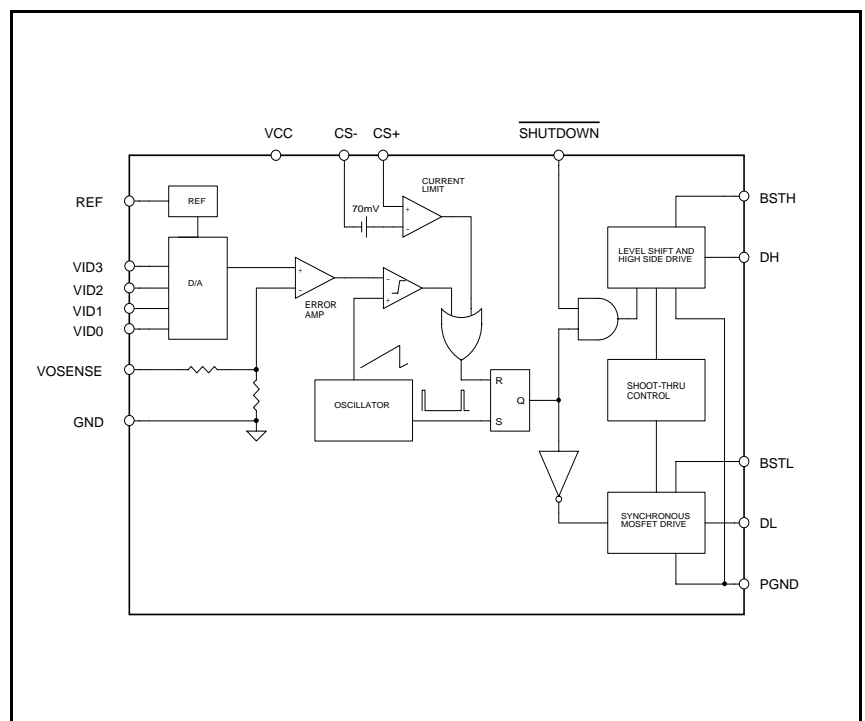
(1) Only available in tape and reel packaging. A reel contains 2500 devices.

(2) "NB" indicates 150 MIL body.

## PIN CONFIGURATION



## BLOCK DIAGRAM



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**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Maximum	Units
V <sub>CC</sub> to GND	V <sub>IN</sub>	-0.3 to 7	V
PGND to GND		± 1	V
BST to GND		-0.3 to 15	V
Thermal Resistance Junction to Case	θ <sub>JC</sub>	30	°C/W
Thermal Resistance Junction to Ambient	θ <sub>JA</sub>	130	°C/W
Operating Temperature Range	T <sub>A</sub>	0 to 70	°C
Storage Temperature Range	T <sub>STG</sub>	-65 to +150	°C
Lead Temperature (Soldering) 10 sec	T <sub>LEAD</sub>	300	°C
ESD Rating (Human Body Model)	ESD	1.5	kV

**ELECTRICAL CHARACTERISTICS**

 Unless specified: V<sub>CC</sub> = 4.75V to 5.25V; GND = PGND = 0V; FB = V<sub>O</sub>; 0mV < (CS(+) - CS(-)) < 60mV; T<sub>J</sub> = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage		See Table 1.			
Supply Voltage	V <sub>CC</sub>	4.5		7	V
Supply Current	V <sub>CC</sub> = 5.0		8	15	mA
Load Regulation	I <sub>O</sub> = 0.3A to 15A <sup>(1)</sup>		1		%
Line Regulation	All VID codes <sup>(1)</sup>		±0.15		%
Gain (A <sub>OL</sub> )	V <sub>OSENSE</sub> to V <sub>O</sub>		35		dB
Current Limit Voltage		60	70	80	mV
Oscillator Frequency		125	140	155	kHz
Buffered Reference Voltage	I <sub>REF</sub> ≤ 1mA		1.25		V
Oscillator Max Duty Cycle		90	95		%
DH Sink/Source Current	BST <sub>H</sub> - DH = 4.5V, DH - PGND <sub>H</sub> = 3V	1			A
DL Sink/Source Current	BST <sub>L</sub> - DL = 4.5V, DL - PGND <sub>L</sub> = 3V	1			A
Dead Time		50	100		ns
VID Pin Source current	VID <sub>x</sub> ≤ 2.4V	30	100		uA

**NOTE:**

- (1) Specification refers to application circuit (Figure 1.).
- (2) This device is ESD sensitive. Use of standard ESD handling precautions is required.

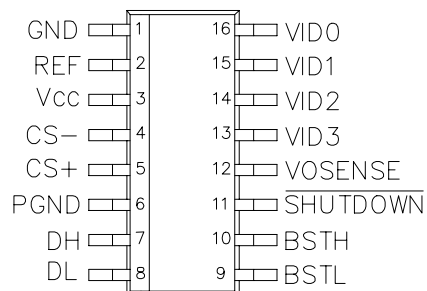
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**PIN DESCRIPTION**

Pin #	Pin Name	Pin Function
1	GND	Small Signal Analog and Digital Ground
2	REF	Buffered Reference output
3	V <sub>CC</sub>	Chip Supply Voltage
4	CS(-)	Current Sense Input (negative)
5	CS(+)	Current Sense Input (positive)
6	PGND	Power Ground for High and Low Side Drivers
7	DH	High Side Driver Output
8	DL	Low Side Driver Output
9	BSTL	V <sub>CC</sub> for Low Side Driver (Boost)
10	BSTH	V <sub>CC</sub> for High Side Driver (Boost)
11	SHUTDOWN	Logic Low shuts down the converter; High or open for normal operation.
12	VOSENSE	Top end of internal feedback chain
13	VID3 <sup>(1)</sup>	Programming Input (MSB)
14	VID2 <sup>(1)</sup>	Programming Input
15	VID1 <sup>(1)</sup>	Programming Input
16	VID0 <sup>(1)</sup>	Programming Input (LSB)

**NOTE:**

(1) All logic level inputs and outputs are open collector TTL compatible.

**PIN CONFIGURATION**


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**OUTPUT VOLTAGE TABLE**

 Unless specified:  $V_{CC} = 4.75V$  to  $5.25V$ ;  $GND = PGND = 0V$ ;  $FB = V_O$ ;  $0mV < (CS(+)) - CS(-) < 60mV$ ;  
 $T_J = 0^{\circ}C$  to  $85^{\circ}C$ 

PARAMETER	CONDITIONS	VID 3210	MIN	TYP	MAX	UNITS
Output Voltage <sup>(1)</sup>	$I_O = 2A$ in Application Circuit (Figure 1)	1111	1.980	2.000	2.020	V
		1110	2.079	2.100	2.121	
		1101	2.178	2.200	2.222	
		1100	2.277	2.300	2.323	
		1011	2.376	2.400	2.424	
		1010	2.475	2.500	2.525	
		1001	2.574	2.600	2.626	
		1000	2.673	2.700	2.727	
		0111	2.772	2.800	2.828	
		0110	2.871	2.900	2.929	
		0101	2.970	3.000	3.030	
		0100	3.069	3.100	3.131	
		0011	3.168	3.200	3.232	
		0010	3.267	3.300	3.333	
		0001	3.366	3.400	3.434	
		0000	3.465	3.500	3.535	

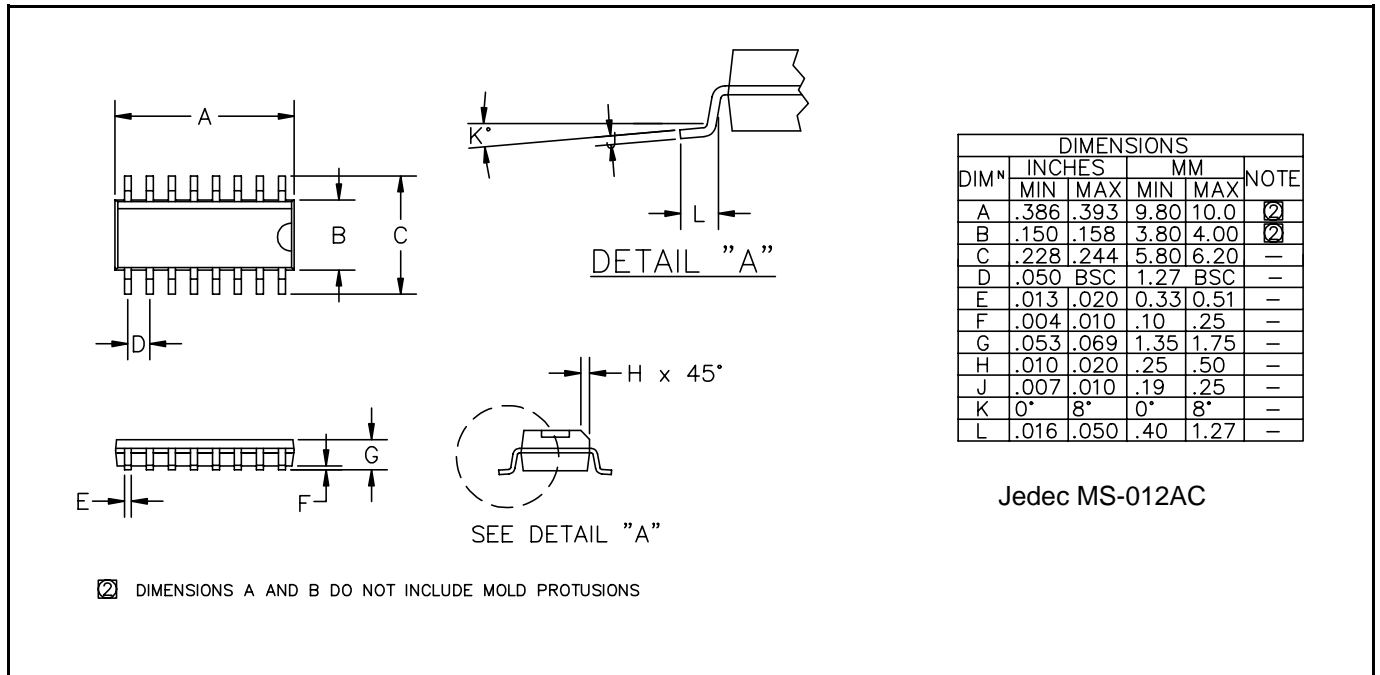
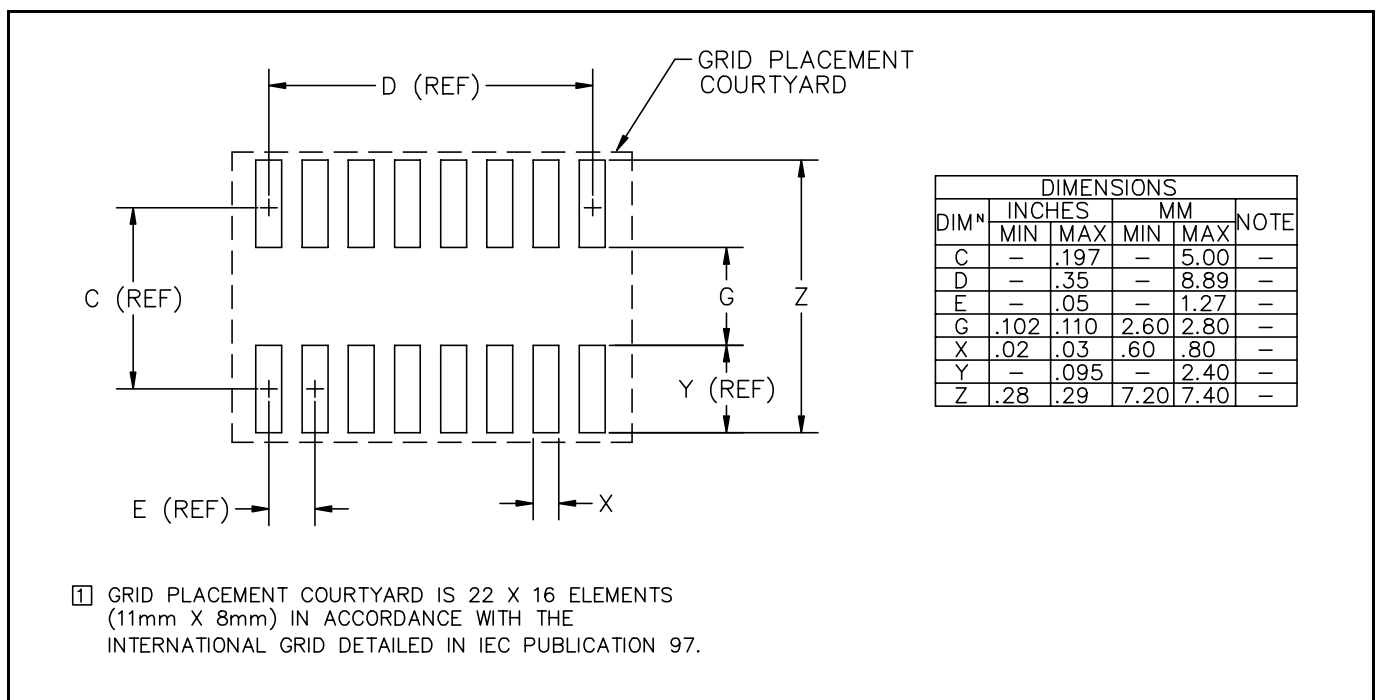
**THEORY OF OPERATION**

The voltage at the VOSENSE pin is applied, through the internal precision resistor feedback chain, to the inverting input of the error amplifier. The non-inverting input of the error amplifier is supplied with a DC voltage derived by the DAC from the internal trimmed bandgap voltage reference. The output of the error amplifier is compared to the triangular output of the internal oscillator to generate a fixed frequency, variable duty cycle pulse train. The internal oscillator uses an on-chip capacitor and precision trimmed current sources to set the frequency to 140 kHz.

The generated pulse train is gated with the output of the current limit latch and the inhibit signal to produce a drive signal for the upper FET. It is also inverted to produce a drive signal for the lower FET. These FET drive signals are modified by the "shoot-through control" circuitry so that the top FET turn-on is delayed until the bottom FET has turned off, and visa-versa.

The current limit latch is set (ending the upper FET drive pulse early) if the current limit comparator indicates an overcurrent condition. The latch is reset at the start of each oscillator period.

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**OUTLINE DRAWING SO-16**

**LAND PATTERN SO-16**


ECN00-1243