

Z89135/Z89136

LOW-COST DTAD CONTROLLER

FEATURES

Device	ROM (KB)	RAM* (Bytes)	I/O Lines	Speed (MHz)
Z89135	24	256	47	20
Z89136	24	256	47	20

- 24 KB of Z8 Program ROM (Z89135)
- Watch-Dog Timer and Power-On Reset
- Low Power STOP Mode
- On-Chip Oscillator which Accepts a Crystal or External Clock Drive
- Two 8-Bit Z8 Counter Timers with 6-Bit Prescaler
- Global Power-Down Mode
- Low Power Consumption - 200 mW (typical)
- Two Comparators with Programmable Interrupt Priority
- Six Vectored, Priority Z8 Interrupts
- RAM and ROM Protect

- Clock Speed of 20.48 MHz
- 16-Bit Digital Signal Processor (DSP)
- 6K Word DSP Program ROM
- 512 Words On-Chip DSP RAM
- 8-Bit A/D Converter with up to 128 kHz Sample Rate
- 10-Bit PWM D/A Converter (4 kHz to 64 kHz)
- Three Vectored, Prioritized DSP Interrupts
- Two DSP Timers to Support Different A/D and D/A Sampling Rates
- Z8 and DSP Operation in Parallel
- IBM® PC-Based Development Tools
- Developer's Toolbox for T.A.M. Applications

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GENERAL DESCRIPTION

The Z89135/136 is a fully integrated, dual processor controller designed for low-cost digital telephone answering machines. The I/O control processor is a Z8® MCU with 24 KB of program memory, two 8-bit counter/timers, and up to 47 I/O pins. The DSP is a 16-bit processor with a 24-bit ALU and accumulator, 512 x 16 bits of RAM, single cycle instructions, and 6K word program ROM plus constants memory. The chip also contains a half-flash 8-bit A/D converter with up to 128 kHz sample rate and 10-bit PWM D/A converter. The sampling rates for the converters are programmable. The precision of the 8-bit A/D may be extended by resampling the data at a lower rate in software.

The Z8 and DSP processors are coupled by mailbox registers and an interrupt system, which allows DSP or Z8 programs to be directed by events in each other's domain.

The Z89136 is the ROMless version of the Z89135. The DSP is not ROMless. The DSP's program memory is always the internal ROM.

GENERAL DESCRIPTION (Continued)

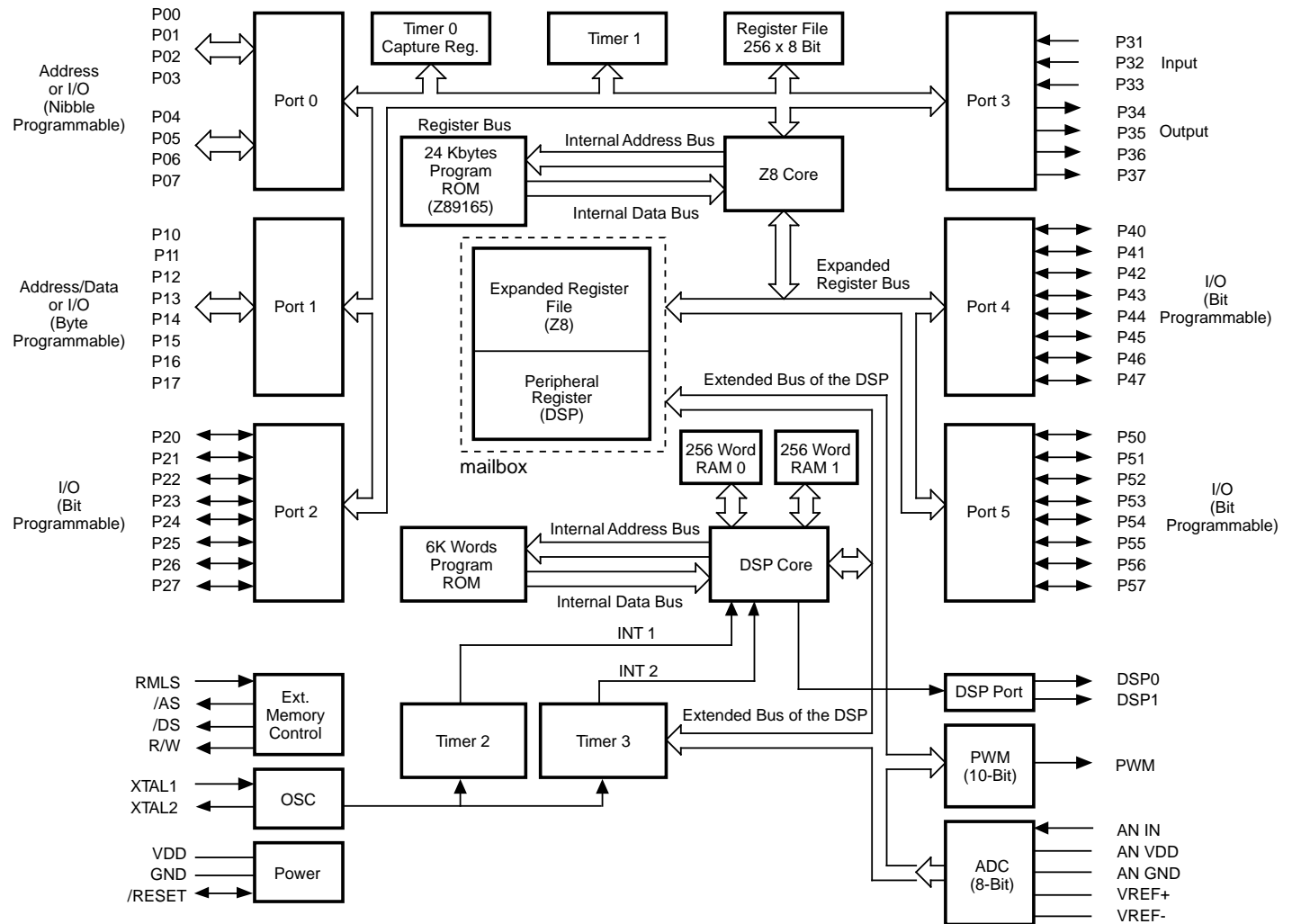


Figure 1. Functional Block Diagram

Z8 Core Processor

The Z8 is Zilog's 8-bit MCU core with an Expanded Register File to allow access to register-mapped peripheral and I/O circuits. The Z8[®] MCU offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features.

For applications demanding powerful I/O capabilities, the Z89135/136 offers 47 pins dedicated to input and output. These lines are grouped into six ports. Each port is configurable under software control to provide timing, status signals and parallel I/O with or without handshake.

There are four basic memory resources for the Z8 that are available to support a wide range of configurations: Program Memory, Register File, Data Memory, and Expanded Register File. The Z8 core processor is characterized by an efficient register file that allows any of 256 on-board data and control registers to be the source and/or the destination of almost any instruction. Traditional microprocessor accumulator bottlenecks are eliminated.

The Register File is composed of 236 bytes of general-purpose registers, four I/O port registers and 15 control and status registers. The Expanded Register File consists of mailbox registers, WDT mode register, DSP Control register, Stop-Mode Recovery register, Port Configuration register, and the control and data registers for Port 4 and Port 5.

To unburden the software from supporting the real-time problems, such as counting/timing and data communication, the Z8 offers two on-chip counter/timers with a large number of user selectable modes.

Watch-Dog Timer and Stop-Mode Recovery features are software driven by setting specific bits in control registers.

STOP and HALT instructions support reduced power operation. The low power STOP Mode allows parameter information to be stored in the register file if power fails. An external capacitor or battery retains power to the device.

DSP Coprocessor

The DSP coprocessor is a second generation, 16-bit two's complement CMOS Digital Signal Processor (DSP). Most instructions, including multiply and accumulate, are accomplished in a single clock cycle. The processor contains two on-chip data RAM blocks of 256 words, a 6K word program ROM, 24-bit ALU, 16 x 16 multiplier, 24-bit Accumulator, shifter, six-level stack, three vectored interrupts, and two inputs for conditional program jumps. Each RAM block contains a set of four pointers which may be incremented or decremented automatically to affect hardware looping without software overhead. The data RAMs can be simultaneously addressed and loaded to the multiplier for a true single cycle scalar multiply.

Four external DSP registers are mapped into the expanded register file of the Z8. Communication between the Z8 and the DSP occurs through those common registers which form the mailbox registers.

The analog signal is generated by a 10-bit resolution Pulse Width Modulator. The PWM output is a digital signal with CMOS output levels. The output signal has a resolution of 1 in 1024 with a sampling rate of 16 kHz (XTAL = 20.48 MHz). The sampling rate can be changed under software control and can be set at 4, 10, 16, and 64 kHz. The dynamic range of the PWM is from 0 to 4V.

An 8-bit resolution half-flash A/D converter is provided. The conversion is conducted with a sampling frequency of 8, 16, 32, 64, or 128 kHz. (XTAL = 20.48 MHz) in order to provide oversampling. The input signal is 4V peak to peak. Scaling is normally $\pm 1.25V$ for the 2.5V peak to peak offset.

Two additional timers (Timer2 and Timer3) have been added to support different sampling rates for the A/D and D/A converters. These timers are free running counters that divide the crystal frequency to the appropriate sampling of frequency.

Notes: All signals with a preceding front slash, "/", are active Low. For example, B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V _{CC}	V _{DD}
Ground	GND	V _{SS}

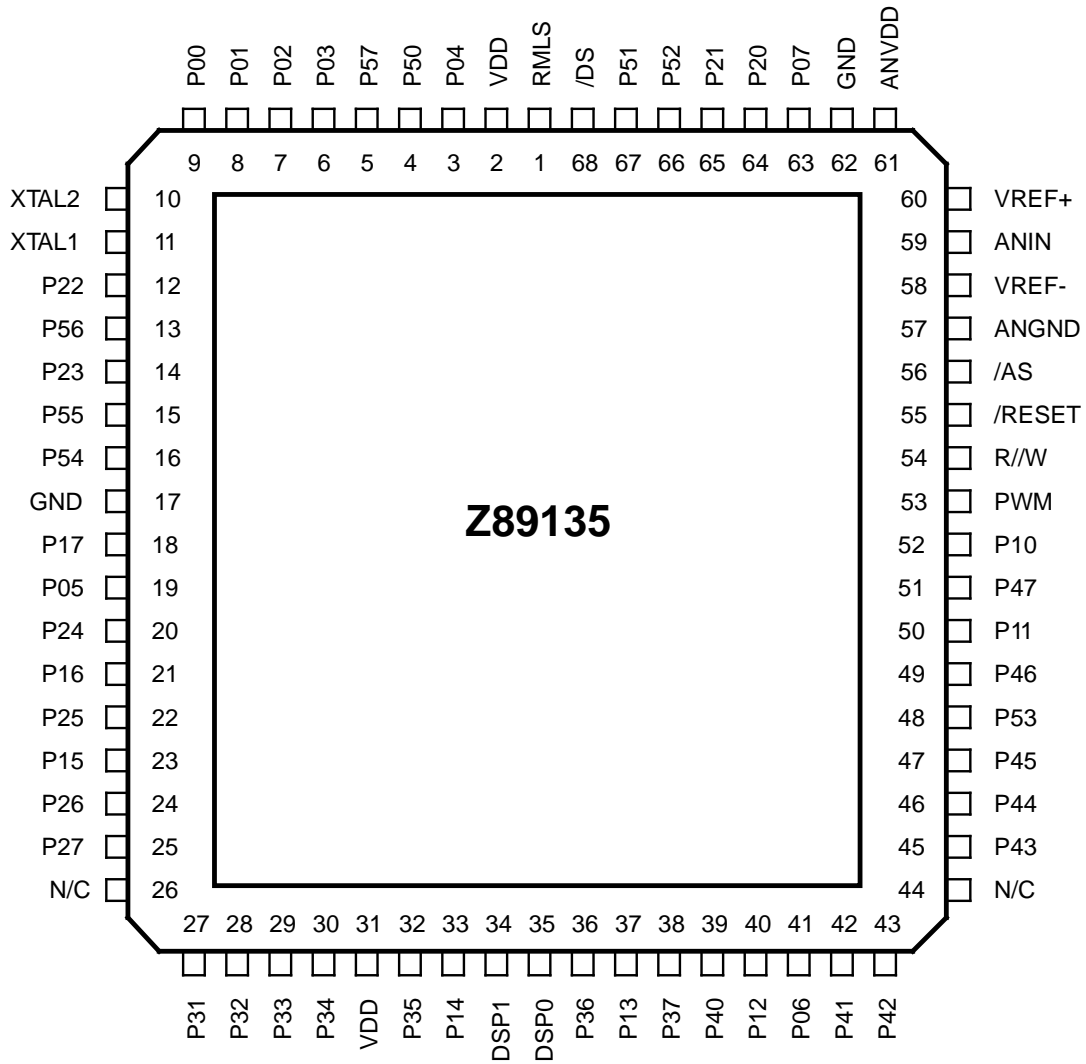


Figure 2. Z89135 68-Pin PLCC Pin Assignments

Table 1. Z89135 68-Pin Plastic Leaded Chip Carrier,
Pin Identification

Pin #	Symbol	Function	Direction
1	RMLS	ROMless	Control Input
2	V _{DD}	Power Supply	
3	P04	Port 0, Bit 4	Input/Output
4	P50	Port 5, Bit 0	Input/Output
5	P57	Port 5, Bit 7	Input/Output
6	P03	Port 0, Bit 3	Input/Output
7	P02	Port 0, Bit 2	Input/Output
8	P01	Port 0, Bit 1	Input/Output
9	P00	Port 0, Bit 0	Input/Output
10	XTAL2	Crystal Oscillator Clock	Output
11	XTAL1	Crystal Oscillator Clock	Input
12	P22	Port 2, Bit 2	Input/Output
13	P56	Port 5, Bit 6	Input/Output
14	P23	Port 2, Bit 3	Input/Output
15	P55	Port 5, Bit 5	Input/Output
16	P54	Port 5, Bit 4	Input/Output
17	GND	Ground	
18	P17	Port 1, Bit 7	Input/Output
19	P05	Port 0, Bit 5	Input/Output
20	P24	Port 2, Bit 4	Input/Output
21	P16	Port 1, Bit 6	Input/Output
22	P25	Port 2, Bit 5	Input/Output
23	P15	Port 1, Bit 5	Input/Output
24	P26	Port 2, Bit 6	Input/Output
25	P27	Port 2, Bit 7	Input/Output
26	N/C	Not Connected	
27	P31	Port 3, Bit 1	Input
28	P32	Port 3, Bit 2	Input
29	P33	Port 3, Bit 3	Input
30	P34	Port 3, Bit 4	Output
31	V _{DD}	Power Supply	
32	P35	Port 3, Bit 5	Output
33	P14	Port 1, Bit 4	Input/Output
34	DSP1	DSP User Output 1	Output

Table 1. Z89135 68-Pin Plastic Leaded Chip Carrier,
Pin Identification

Pin #	Symbol	Function	Direction
35	DSP0	DSP User Output 0	Output
36	P36	Port 3, Bit 7	Output
37	P13	Port 1, Bit 3	Input/Output
38	P37	Port 3, Bit 7	Output
39	P40	Port 4, Bit 0	Input/Output
40	P12	Port 1, Bit 2	Input/Output
41	P06	Port 0, Bit 6	Input/Output
42	P41	Port 4, Bit 1	Input/Output
43	P42	Port 4, Bit 2	Input/Output
44	N/C	Not Connected	
45	P43	Port 4, Bit 3	Input/Output
46	P44	Port 4, Bit 4	Input/Output
47	P45	Port 4, Bit 5	Input/Output
48	P53	Port 5, Bit 3	Input/Output
49	P46	Port 4, Bit 6	Input/Output
50	P11	Port 1, Bit 1	Input/Output
51	P47	Port 4, Bit 7	Input/Output
52	P10	Port 1, Bit 0	Input/Output
53	PWM	Pulse Width Modulator	Output
54	R/W	Read/Write	Output
55	/RESET	Reset	Input/Output
56	/AS	Address Strobe	Output
57	ANGND	Analog Ground	
58	V _{REF-}	Analog Voltage Ref.	Input
59	AN _{IN}	Analog Input	Input
60	V _{REF+}	Analog Voltage Ref.	Input
61	ANV _{DD}	Analog Power Supply	
62	GND	Ground	
63	P07	Port 0, Bit 7	Input/Output
64	P20	Port 2, Bit 0	Input/Output
65	P21	Port 2, Bit 1	Input/Output
66	P52	Port 5, Bit 2	Input/Output
67	P51	Port 5, Bit 1	Input/Output
68	/DS	Data Strobe	Output

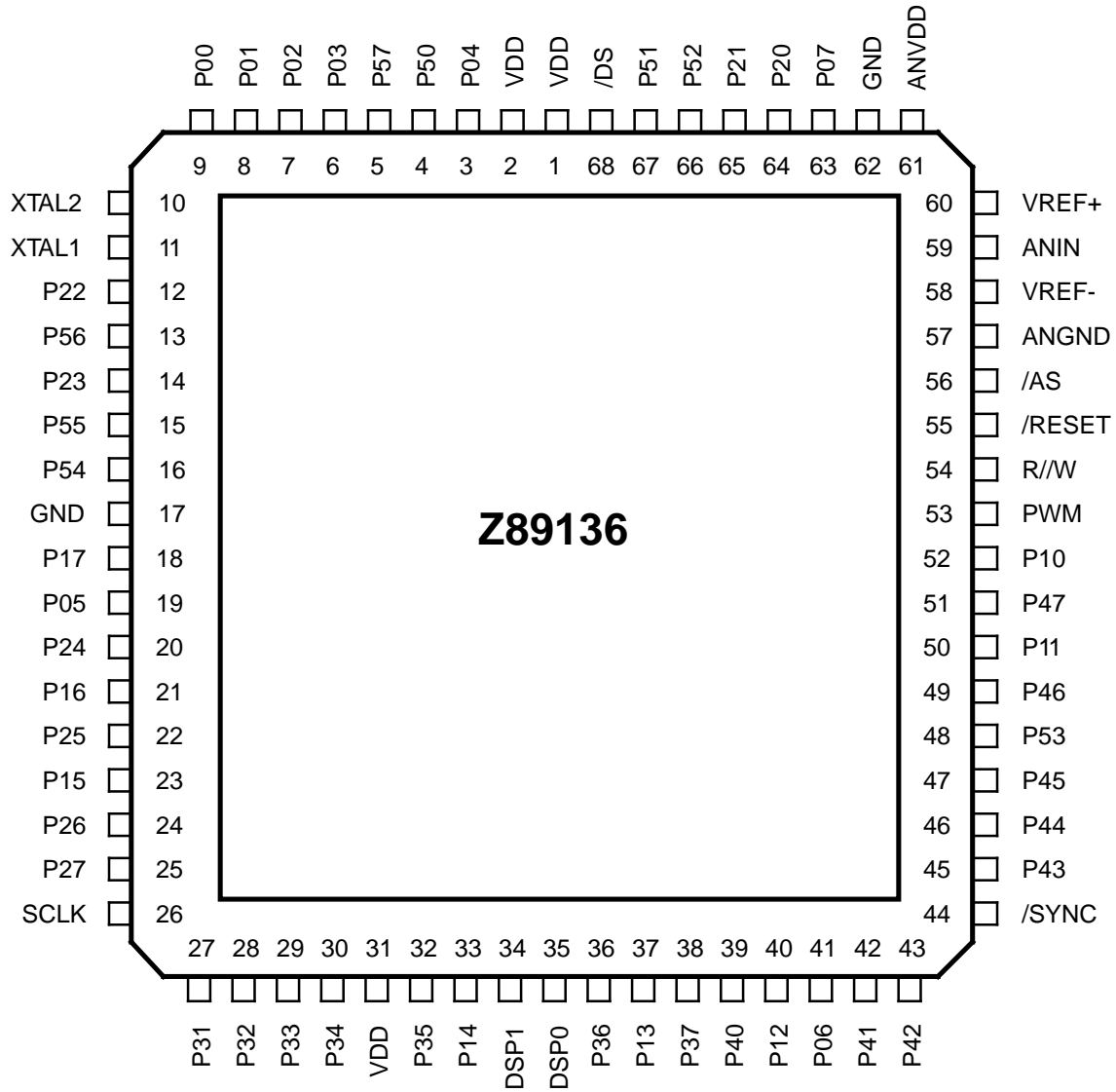


Figure 3. Z89136 68-Pin PLCC Pin Assignments

Table 2. Z89136 68-Pin Plastic Leaded Chip Carrier,
Pin Identification

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7	P02	Port 0, Bit 2	Input/Output
8	P01	Port 0, Bit 1	Input/Output
9	P00	Port 0, Bit 0	Input/Output
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13	P56	Port 5, Bit 6	Input/Output
14	P23	Port 2, Bit 3	Input/Output
15	P55	Port 5, Bit 5	Input/Output
16	P54	Port 5, Bit 4	Input/Output
17	GND	Ground	
18	P17	Port 1, Bit 7	Input/Output
19	P05	Port 0, Bit 5	Input/Output
20	P24	Port 2, Bit 4	Input/Output
21	P16	Port 1, Bit 6	Input/Output
22	P25	Port 2, Bit 5	Input/Output
23	P15	Port 1, Bit 5	Input/Output
24	P26	Port 2, Bit 6	Input/Output
25	P27	Port 2, Bit 7	Input/Output
26	SCLK	System Clock	Output
27	P31	Port 3, Bit 1	Input
28	P32	Port 3, Bit 2	Input
29	P33	Port 3, Bit 3	Input
30	P34	Port 3, Bit 4	Output
31	V _{DD}	Power Supply	
32	P35	Port 3, Bit 5	Output
33	P14	Port 1, Bit 4	Input/Output
34	DSP1	DSP User Output 1	Output

Table 2. Z89136 68-Pin Plastic Leaded Chip Carrier,
Pin Identification

Pin #	Symbol	Function	Direction
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36	P36	Port 3, Bit 7	Output
37	P13	Port 1, Bit 3	Input/Output
38	P37	Port 3, Bit 7	Output
39	P40	Port 4, Bit 0	Input/Output
40	P12	Port 1, Bit 2	Input/Output
41	P06	Port 0, Bit 6	Input/Output
42	P41	Port 4, Bit 1	Input/Output
43	P42	Port 4, Bit 2	Input/Output
44	/SYNC	Synchronization Pin	Output
45	P43	Port 4, Bit 3	Input/Output
46	P44	Port 4, Bit 4	Input/Output
47	P45	Port 4, Bit 5	Input/Output
48	P53	Port 5, Bit 3	Input/Output
49	P46	Port 4, Bit 6	Input/Output
50	P11	Port 1, Bit 1	Input/Output
51	P47	Port 4, Bit 7	Input/Output
52	P10	Port 1, Bit 0	Input/Output
53	PWM	Pulse Width Modulator	Output
54	R/W	Read/Write	Output
55	/RESET	Reset	Input/Output
56	/AS	Address Strobe	Output
57	ANGND	Analog Ground	
58	V _{REF-}	Analog Voltage Ref.	Input
59	AN _{IN}	Analog Input	Input
60	V _{REF+}	Analog Voltage Ref.	Input
61	ANV _{DD}	Analog Power Supply	
62	GND	Ground	
63	P07	Port 0, Bit 7	Input/Output
64	P20	Port 2, Bit 0	Input/Output
65	P21	Port 2, Bit 1	Input/Output
66	P52	Port 5, Bit 2	Input/Output
67	P51	Port 5, Bit 1	Input/Output
68	/DS	Data Strobe	Output

A/D CONVERTER (ADC)

Figure 4 shows the input circuit of the ADC. When conversion starts, the analog input voltage from the input is connected to the MSB and LSB flash converter inputs as shown in the Input Impedance CKT diagram. Shunting 31 parallel internal resistances of the analog switches and simultaneously charging 31 parallel 1 pF capacitors is equivalent to a 400 Ohms input impedance in parallel with a 31 pF capacitor. Other input stray capacitance adds about 10

pF to the input load. Input source resistances up to 2 Kohms can be used under normal operating conditions without any degradation of the input settling time. For larger input source resistance, longer conversion cycle times may be required to compensate the input settling time problem. V_{REF} is set using the $V_{REF} +$ pin.

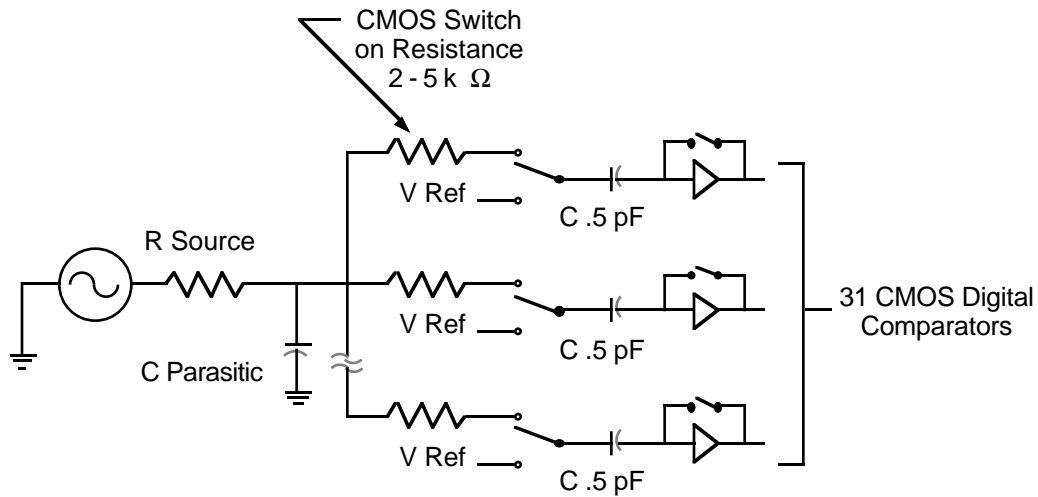


Figure 4. Input Impedance of ADC

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage (*)	-0.3	+7.0	V
T_{STG}	Storage Temp	-65°	+150°	C
T_A	Oper Ambient Temp		†	C

Notes:

Voltage on all pins with respect to GND.

† See Ordering Information.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 5).

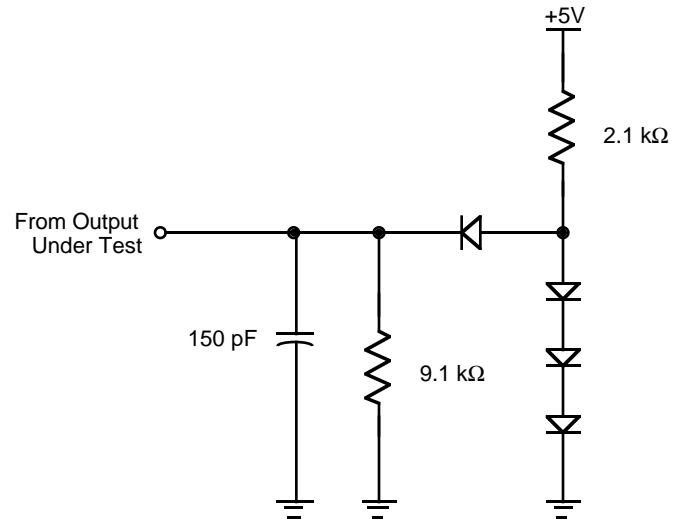


Figure 5. Test Load Diagram

CAPACITANCE

$T_A = 25^\circ\text{C}$, $V_{CC} = \text{GND} = 0\text{V}$, $f = 1.0\text{ MHz}$, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V_{CC}	$T_A = 0^\circ\text{C to } +55^\circ\text{C}$		Typical @ 25°C	Units
			Min	Max		
I_{CC}	Supply Current	5.0V		65	40	mA
I_{CC1}	HALT Mode Current	5.0V		20	6	mA
I_{CC2}	STOP Mode Current	5.0V		400	300	μA

Note: 5.0V \pm 0.25V.

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V _{CC}	T _A = 0° C to +55° C		Typical @ 25°C	Units	Conditions
			Min	Max			
V _{MAX}	Max Input Voltage	5.0V		7			
V _{CH}	Clock Input High Voltage	5.0V	0.9 V _{CC}	V _{CC} +0.3	2.5	V	Driven by External Clock Generator
V _{CL}	Clock Input Low Voltage	5.0V	GND-0.3	0.1 V _{CC}	1.5	V	Driven by External Clock Generator
V _{IH}	Input High Voltage	5.0V	0.7 V _{CC}	V _{CC} +0.3	2.5	V	
V _{IL}	Input Low Voltage	5.0V	GND-0.3	0.2 V _{CC}	1.5	V	
V _{OH}	Output High Voltage	5.0V	V _{CC} -0.4		4.8	V	I _{OH} = -2.0 mA
V _{OL1}	Output Low Voltage	5.0V		0.4	0.1	V	I _{OL} = +4.0 mA
V _{OL2}	Output Low Voltage	5.0V		1.2	0.3	V	I _{OL} = +12 mA, 3 Pin Max
V _{RH}	Reset Input High Voltage	5.0V	0.8 V _{CC}	V _{CC}	2.1	V	
V _{RI}	Reset Input Low Voltage	5.0V	GND-0.3	0.2 V _{CC}	1.7		
V _{OFFSET}	Comparator Input Offset Voltage	5.0V		25	10	mV	
I _{IL}	Input Leakage	5.0V	-5	5	25	μA	V _{IN} = 0V, V _{CC}
I _{OL}	Output Leakage	5.0V	-5	5	25	μA	V _{IN} = 0V, V _{CC}
I _{IR}	Reset Input Current	5.0V		-55	-30	μA	

Note: 5.0V ±0.25V

DC ELECTRICAL CHARACTERISTICS

Z89165 A/D Converter

Sym	Parameter	V _{DD}	T _A = 0°C to +55°C		Units	Conditions			
			Min	Max					
I _{IL}	Input Leakage Analog Input	5.0V		40	μA	ANV _{DD}	=	5.50	V
						V _{IN}	=	0.00	V
						V _{REFH}	=	5.50	V
						V _{REFL}	=	0.00	V
I _{IH}	Input Leakage Analog Input	5.25V		2.00	μA	ANV _{DD}	=	5.50	V
						V _{IN}	=	5.50	V
						V _{REFH}	=	5.50	V
						V _{REFL}	=	0.00	V
I _{VREFH}	Input Current	5.25V		2.00	mA	V _{IN}	=	5.50	V
						V _{REFL}	=	0.00	V
						ANV _{DD}	=	5.50	V
I _{VREFL}	Input Current	5.25V		80	μA	V _{IN}	=	5.50	V
						V _{REFL}	=	5.50	V
						ANV _{DD}	=	5.50	V
I _{VEFL}	Input Current	5.25V		-2.00	mA	V _{IN}	=	0.00	V
						V _{REFH}	=	5.50	V
						ANV _{DD}	=	0.00	V
I _{VREFL}	Input Current	5.25V		-80	μA	V _{IN}	=	0.00	V
						V _{REFH}	=	5.50	V
						ANV _{DD}	=	5.50	V

DC ELECTRICAL CHARACTERISTICS

21 Other Non-Regular I/O

Sym	Parameter	V _{DD}	T _A = 0°C to +55°C		Units	Conditions
			Min	Max		
I _{IRH}	Input Current ROMless Pin	5.25V		6.00	μA	V _{IN} = 5.25 V
I _{IR1}	Input Current ROMless Pin	5.25V		6.00	μA	V _{IN} = 0.00 V
I _{IR}	Input Current ROMless Pin During Reset Active	5.25V		1.00	mA	V _{IN} = 5.25 V
I _{IHX2}	Input Current XTAL2 pin in STOP Mode	5.25V		1.00	μA	V _{IN} = 0.00 V
I _{ILX2}	Input Current XTAL2 Pin in STOP Mode	5.25V		1.00	μA	V _{IN} = 5.25 V
I _{IHX1}	Input current XTAL1 Pin	5.25V		30	μA	V _{IN} = 0.00 V
I _{ILX1}	Input Current XTAL1 Pin	5.25V		30	μA	V _{IN} = 5.25 V
V _{OLXR}	Output Low Voltage XTAL2 Reset Inactive	5.25V		1.20	V	I _{OL} = 4.00 mA
V _{OLX}	Output Low Voltage XTAL2 Reset Inactive	5.25V		0.60	V	I _{OL} = 1.00 mA
V _{OHXR}	Output High Voltage XTAL2 Reset Inactive	5.25V	4.00		V	I _{OH} = 4.00 mA
V _{OHX}	Output High Voltage XTAL2 Reset Inactive	5.25V	4.00		V	I _{OH} = 1.00 mA
I _{IH}	Input Current P31,P32,P33	5.25V		1.00	μA	V _{IN} = 5.25 V
I _{IL}	Input Current P31, P32, P33	5.25V		1.00	μA	V _{IN} = 0.00 V

AC CHARACTERISTIC

External I/O or Memory Read and Write Timing Diagram

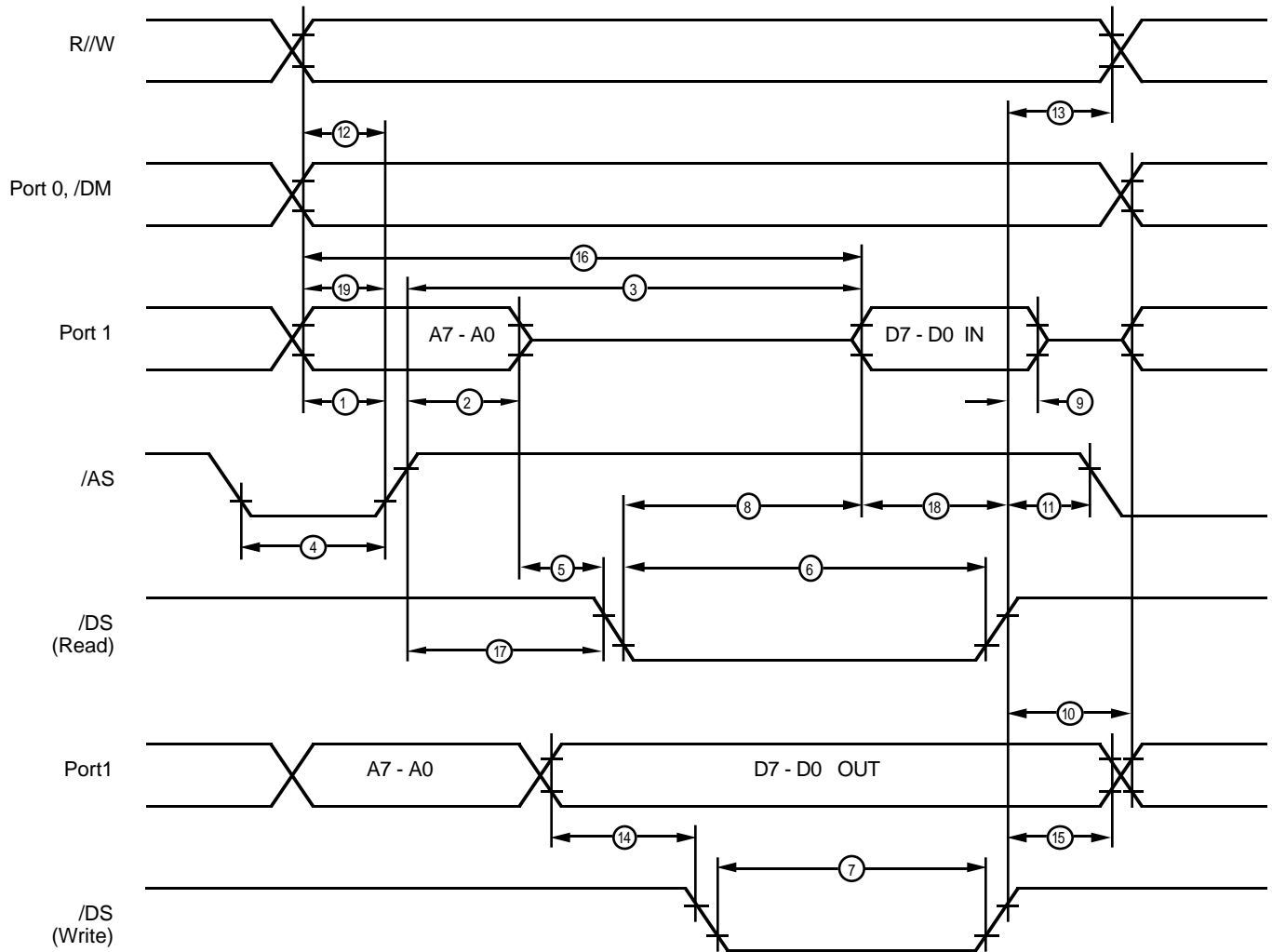


Figure 6. External I/O or Memory Read/Write Timing

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Table

No	Symbol	Parameter	V _{CC}	T _A =0°C to +55°C		Units	Notes
				Min	Max		
1	TdA(AS)	Address Valid to /AS Rise Delay	5.0V	25		ns	2,3
2	TdAS(A)	/AS Rise to Address Float Delay	5.0V	35		ns	2,3
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid	5.0V		150	ns	1,2,3
4	TwAS	/AS Low Width	5.0V	35		ns	2,3
5	TdAZ(DS)	Address Float to /DS Fall	5.0V	0		ns	
6	TwDSR	/DS (Read) Low Width	5.0V	125		ns	1,2,3
7	TwDSW	/DS (Write) Low Width	5.0V	75		ns	1,2,3
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid	5.0V		90	ns	1,2,3
9	ThDR(DS)	Read Data to /DS Rise Hold Time	5.0V	0		ns	2,3
10	TdDS(A)	/DS Rise to Address Active Delay	5.0V	40		ns	2,3
11	TdDS(AS)	/DS Rise to /AS Fall Delay	5.0V	35		ns	2,3
12	TdR/W(AS)	R/W Valid to /AS Rise Delay	5.0V	25		ns	2,3
13	TdDS(R/W)	/DS Rise to R/W Not Valid	5.0V	35		ns	2,3
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	5.0V	40		ns	2,3
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	5.0V	25		ns	2,3
16	TdA(DR)	Address Valid to Read Data Req'd Valid	5.0V		180	ns	1,2,3
17	TdAS(DS)	/AS Rise to /DS Fall Delay	5.0V	48		ns	2,3
18	TdDI(DS)	Data Input Setup to /DS Rise	5.0V	50		ns	1,2,3
19	TdDM(AS)	/DM Valid to /AS Fall Delay	5.0V	20		ns	2,3

Notes:

1. When using extended memory timing, add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. See clock cycle dependent characteristics table.

5.0V ±0.25V

Standard Test Load

All timing references use 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.

AC ELECTRICAL CHARACTERISTICS

Additional Timing Diagram

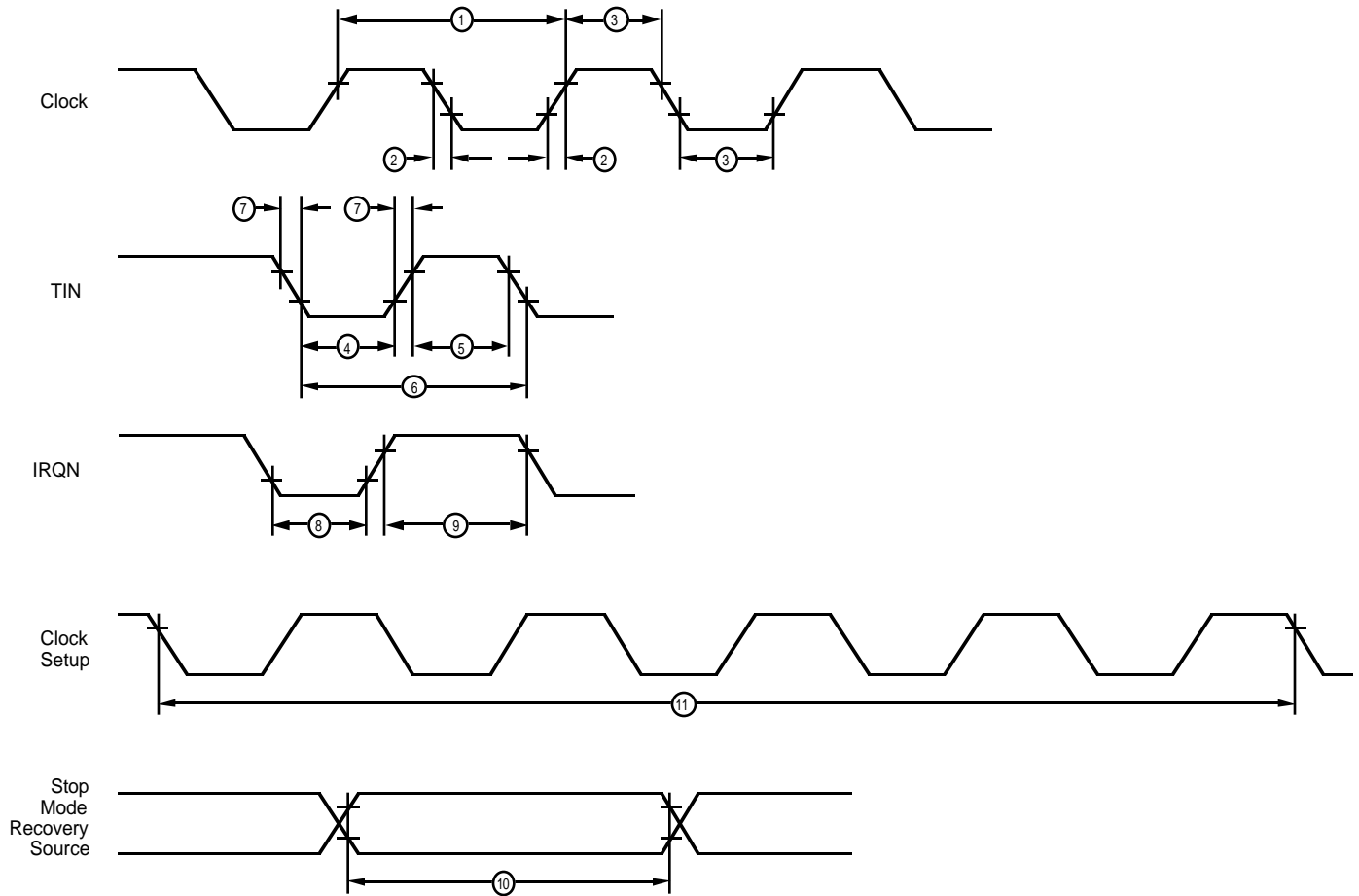


Figure 7. Additional Timing

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table

No	Symbol	Parameter	V _{CC}	T _A =0°C to +55°C		Units	Notes
				Min	Max		
1	TpC	Input Clock Period	5.0V	48.83		ns	1
2	TrC,TfC	Clock Input Rise & Fall Times	5.0V		6	ns	1
3	TwC	Input Clock Width	5.0V	17		ns	1
4	TwTinL	Timer Input Low Width	5.0V	70		ns	
5	TwTinH	Timer Input High Width	5.0V	3TpC			1
6	TpTin	Timer Input Period	5.0V	8TpC			1
7	TrTin, TfTin	Timer Input Rise & Fall Timer	5.0V		100	ns	1
8A	TwIL	Int. Request Low Time	5.0V	70		ns	1,2
8B	TwIL	Int. Request Low Time	5.0V	3TpC			1
9	TwIH	Int. Request Input High Time	5.0V	3TpC			1
10	Twsm	Stop-Mode Recovery Width Spec	5.0V	12 5TpC		ns	1
11	Tost	Oscillator Start-up Time	5.0V	5TpC			3
12	Twdt	Watch-Dog Timer	5.0V	5		ms	D1 = 0, D0 = 0 [4]
			5.0V	15		ms	D1 = 0, D0 = 1 [4]
			5.0V	25		ms	D1 = 1, D0 = 0 [4]
			5.0V	100		ms	D1 = 1, D0 = 1 [4]

Notes:

1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
 2. Interrupt request through Port 3 (P33-P31)
 3. SMR-D5 = 0
 4. Reg. WDT
- 5.0V ±0.25V

AC ELECTRICAL CHARACTERISTICS

Handshake Timing Diagrams

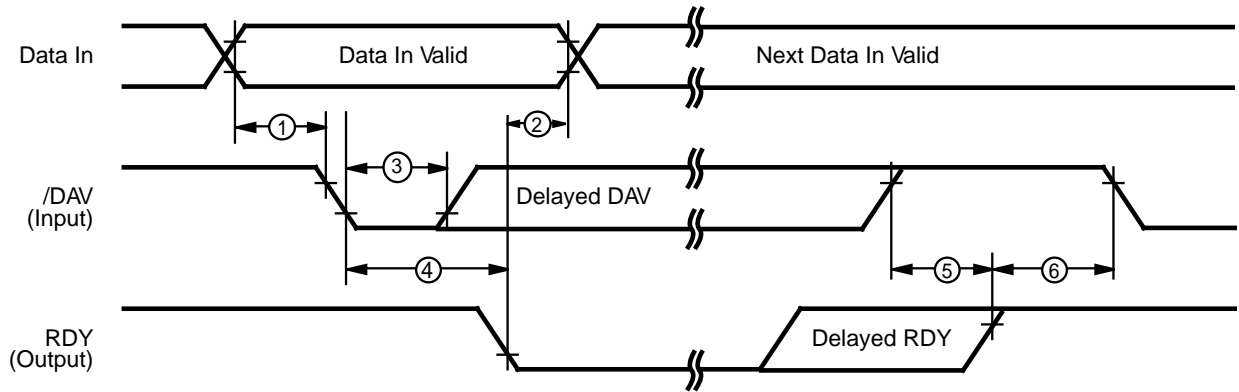


Figure 8. Input Handshake Timing

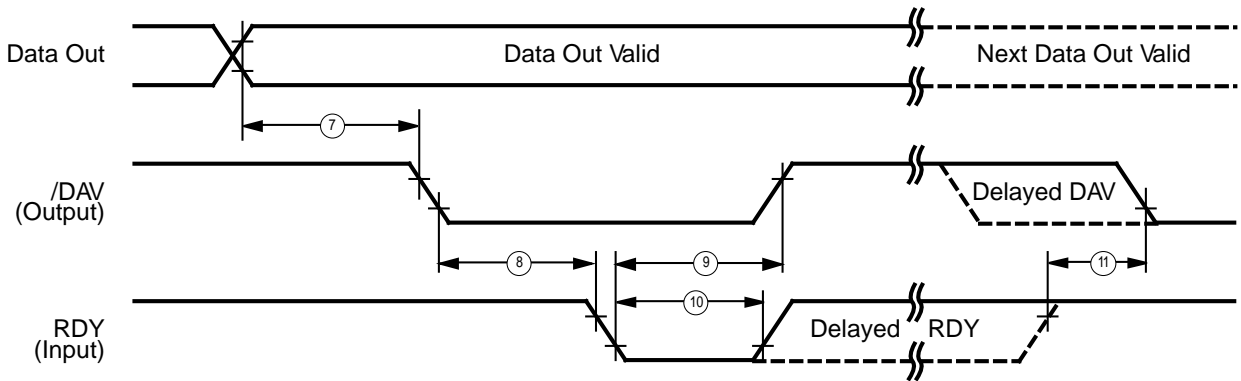


Figure 9. Output Handshake Timing

AC ELECTRICAL CHARACTERISTICS (Continued)

Handshake Timing Table

No	Symbol	Parameter	V _{CC}	T _A = 0°C to +55°C		Units	Data Direction
				Min	Max		
1	TsDI(DAV)	Data In Setup Time	5.0V	0		ns	IN
2	ThDI(DAV)	RDY to Data Hold Time	5.0V	0		ns	IN
3	TwDAV	Data Available Width	5.0V	40		ns	IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay	5.0V		70	ns	IN
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay	5.0V		40	ns	IN
6	TdDO(DAV)	RDY Rise to DAV Fall Delay	5.0V	0		ns	IN
7	TcLDAV0(RDY)	Data Out to DAV Fall Delay	5.0V	TpC		ns	OUT
8	TcLDAV0(RDY)	DAV Fall to RDY Fall Delay	5.0V	0		ns	OUT
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay	5.0V		70	ns	OUT
10	TwRDY	RDY Width	5.0V	40		ns	OUT
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay	5.0V		40	ns	OUT

Note: 5.0V ±0.25V

AC ELECTRICAL CHARACTERISTICS

A/D Electrical Characteristics

 $T_A = 0^{\circ}\text{C} - 55^{\circ}\text{C}; V_{CC} = 5.0\text{V} \pm 0.25\text{V}$

Parameter	Min	Max	Typical	Units
Resolution			8	bits
Integral non-linearity		1	0.5	lsb
Differential non-linearity		0.5		lsb
Zero Error at 25°C		50		mV
Power Dissipation		75	35	mW
Clock Frequency		20.48		MHz
Clock Pulse Width	35			ns
Analog Input Voltage Range	AN_{GND}	$AN_{V_{CC}}$		V
Conversion Time		2		μs
Input Capacitance on		60		pF
VA_{HI} range damage	AN_{GND}	$AN_{V_{CC}}$		V
VA_{LO} range damage	AN_{GND}	$AN_{V_{CC}}$		V
AN_{GND}	V_{SS}	$AN_{V_{CC}}$		V
$AN_{V_{CC}}$	AN_{GND}	V_{CC}		V

PIN FUCTIONS

/RESET. (input/output, active Low). This pin initializes the MCU. Reset is accomplished either through Power-On Reset (POR), Watch-Dog Timer reset, Stop-Mode Recovery, or external reset. During POR and WDT Reset, the internally generated reset is driving the reset pin Low for the POR time. Any devices driving the reset line must be open drain to avoid damage from a possible conflict during reset conditions. A /RESET will reset both the Z8 and the DSP.

For the Z8:

After the POR time, /RESET is a Schmitt-triggered input. To avoid asynchronous and noisy reset problems, the Z8 is equipped with a reset filter of four external clocks (4TpC). If the external reset signal is less than 4TpC in duration, no reset occurs. On the fifth clock after the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external reset, whichever is longer. Program execution begins at location 000CH (Hexadecimal), 5-10 TpC cycles after the /RESET is released. The Z8 does not reset WDT, SMR, P2M, and P3M registers on a Stop-Mode Recovery operation.

For the DSP:

A low level on the /RESET pin generates an internal reset signal. The /RESET signal must be kept low for at least one clock cycle. The CPU will fetch a new Program Counter (PC) value from program memory address 0FFCH after the reset signal is released.

RMLS. *ROMless* (input, active High). This pin, when connected to VDD, disables the internal Z8 ROM. (Note that, when pulled Low to GND that part functions normally as the ROM version). The DSP can not be configured as ROMless. This pin is only available on the Z89135.

R/W. *Read/Write* (output, write Low). The R/W signal defines the signal flow when the Z8 is reading or writing to external program or data memory. The Z8 is reading when this pin is High and writing when this pin is Low.

/AS. *Address Strobe* (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle. Address output is through Port 0/Port 1 for all external programs. Memory address transfers are valid at the trailing edge of /AS. Under program control, /AS is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

/DS. *Data Strobe* (output, active Low). Data Strobe is activated once for each external memory transfer. For read operations, data must be available prior to the trailing edge of /DS. For write operations, the falling edge of /DS indicates that output data is valid.

XTAL1. *Crystal 1* (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, RC network or an external single-phase clock to the on-chip oscillator input.

XTAL2. *Crystal 2* (time-based output). This pin connects a parallel-resonant, crystal, ceramic resonator, or LC network to the on-chip oscillator output.

DSP0. (output). DSP0 is a general-purpose output pin connected to bit 6 of the Analog Control Register (DSP EXT4). This bit has no special significance and may be used to output data by writing to bit 6 of the ACR.

DSP1. (output). DSP1 is a general-purpose output pin connected to bit 7 of the Analog Control Register (DSP EXT4). This bit has no special significance and may be used to output data by writing to bit 7 of the ACR.

SCLK. *System Clock* (output). SCLK outputs the system clock. This pin is available on the Z89136.

/SYNC. *Synchronize* (output). This signal indicates the last clock cycle of the current executing Z8 instruction. This pin is only available on the Z89136.

PWM. *Pulse Width Modulator* (output). The PWM is a 10-bit resolution D/A converter. This output is a digital signal with CMOS output levels.

AN_{IN}. (input). Analog input for the A/D converter.

AN_{VDD}. Analog power supply for the A/D converter.

AN_{GND}. Analog ground for the A/D converter.

V_{REF+}. (input). Reference voltage (High) for the A/D converter.

V_{REF-}. (input). Reference voltage (Low) for the A/D converter.

V_{DD}. Digital power supply for the Z89135.

GND. Digital ground for the Z89135.

Port 0. (P07-P00). Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port, or as an address port for interfacing external memory. The input buffers are Schmitt-triggered and the output drivers are push-pull. Port 0 is placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0. Handshake signal direction is dictated by the I/O direction to Port 0 of the upper nibble P07-P04. The lower nibble must have the same direction as the upper nibble.

The Auto Latch on Port 0 puts valid CMOS levels on all CMOS inputs which are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

For external memory references, Port 0 provides address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nib-

ble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they are configured by writing to the Port 0 mode register.

In ROMless mode, after a hardware reset, Port 0 is configured as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode. (In ROM mode, Port 0 is defined as input after reset.)

Port 0 is set in the high-impedance mode if selected as an address output state along with Port 1 and the control signals /AS, /DS and R/W (Figure 10).

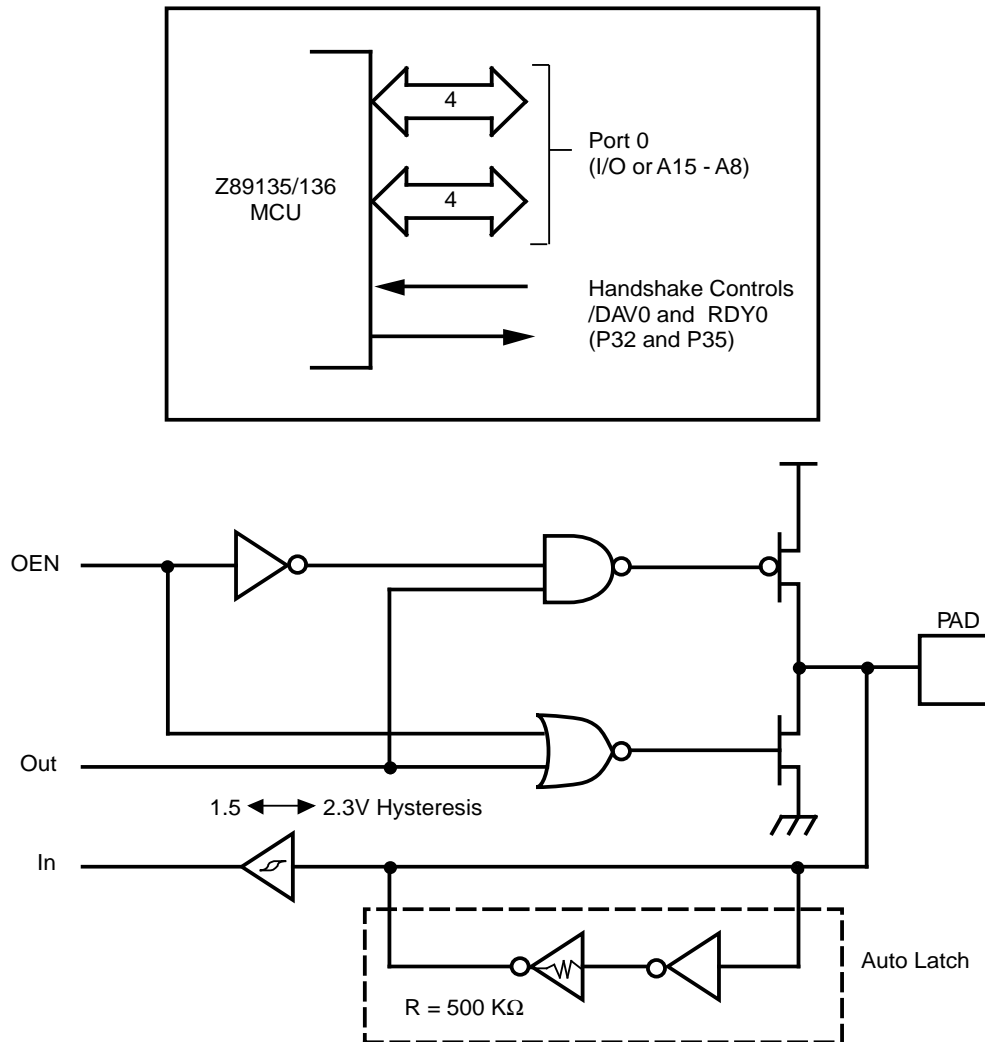


Figure 10. Port 0 Configuration

PIN FUCTIONS (Continued)

Port 1. (P17-P10). Port 1 is an 8-bit, bidirectional, CMOS-compatible port (Figure11). It has multiplexed Address (A7-A0) and Data (D7-D0) ports. These eight I/O lines are programmed as inputs or outputs, or can be configured under software control as an Address/Data port for interfacing external memory. The input buffers are Schmitt triggered and the output drivers are push-pull.

Port 1 may be placed under handshake control. In this configuration, Port 3, lines P33 and P34 are used as the handshake controls RDY1 and /DAV1 (Ready and Data Available). Memory locations greater than 24575 (in ROM

mode) are referenced through Port 1. To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines.

Port 1 can be placed in the high-impedance state along with Port 0, /AS, /DS and R/W, allowing the Z89135/136 to share common resources in multiprocessor and DMA applications.

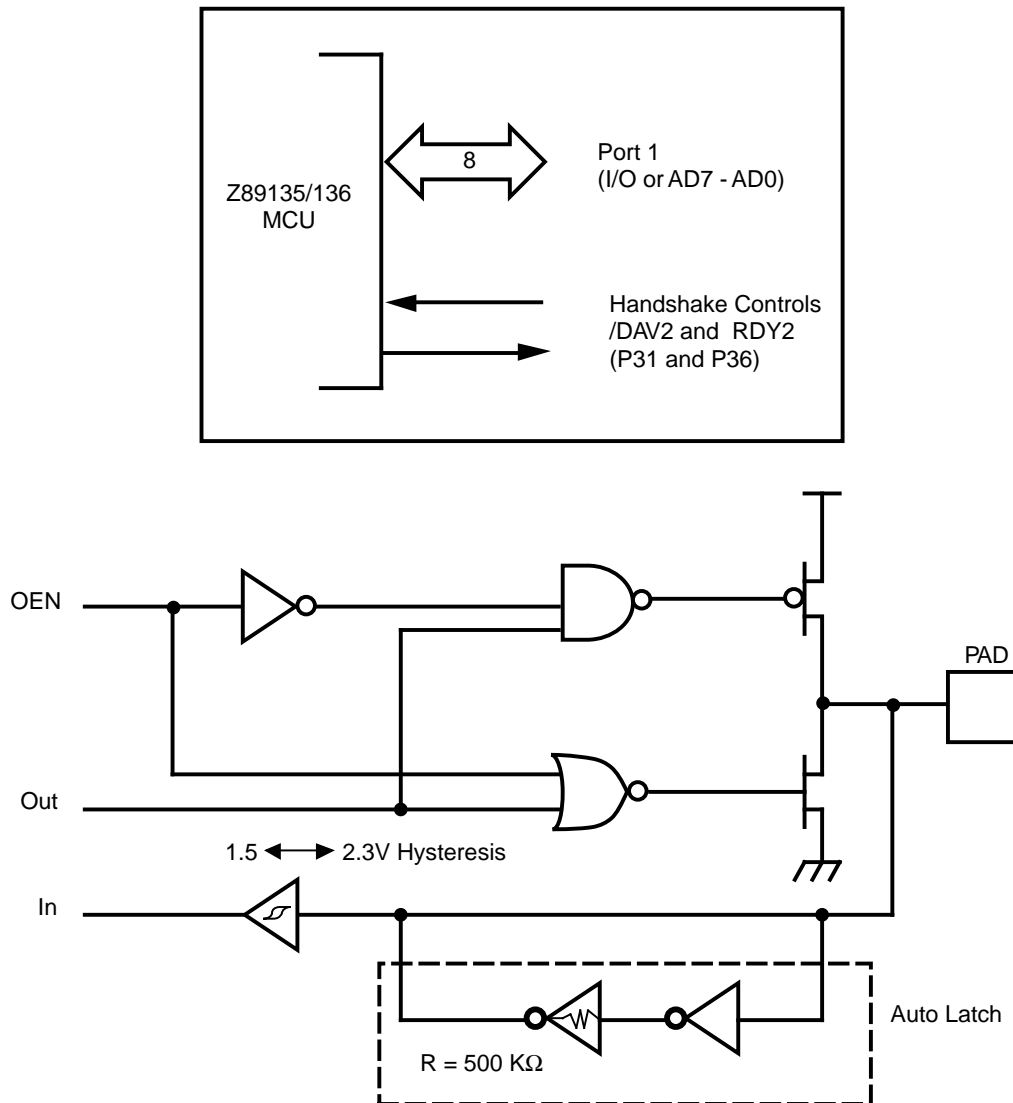


Figure 11. Port 1 Configuration

Port 2. (P27-P20). Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port. These eight I/O lines are configured under software control as an input or output, independently. Port 2 is always available for I/O operation. The input buffers are Schmitt triggered. Bits programmed as outputs may be globally programmed as either push-pull or open-drain.

Port 2 may be placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake controls lines /DAV2 and RDY2. The handshake

signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to bit 7, Port 2 (Figure 12).

The Auto Latch on Port 2 puts valid CMOS levels on all CMOS inputs which are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

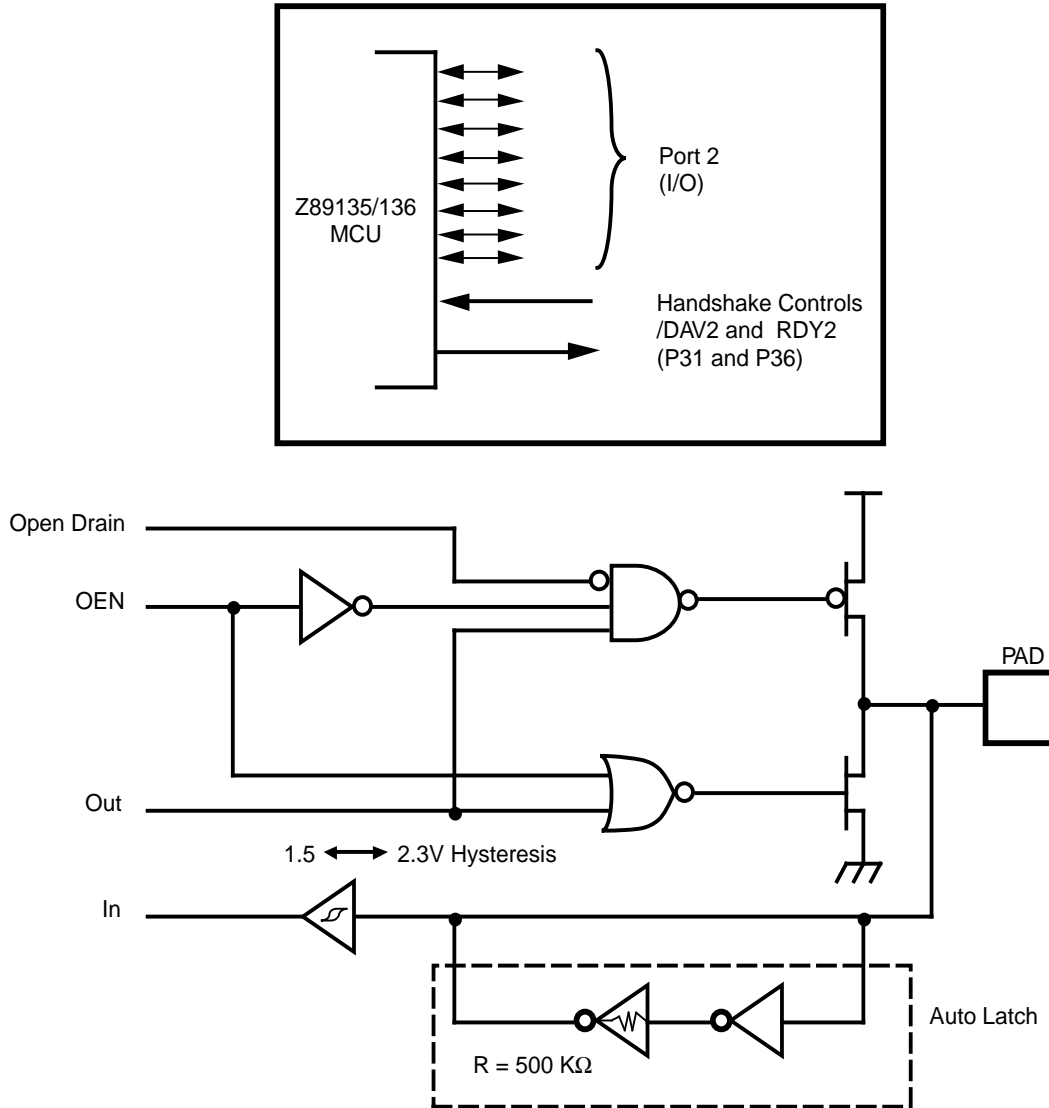


Figure 12. Port 2 Configuration

PIN FUCTIONS (Continued)

Port 3. (P37-P31). Port 3 is a 7-bit, CMOS-compatible port with three fixed inputs (P33-P31) and four fixed outputs (P37-P34). It is configured under software control for input/output, counter/timers, interrupt, and port handshakes. Pins P31, P32, and P33 are standard CMOS inputs; outputs are push-pull.

Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). Port 3, pin 3 is a falling edge interrupt input. P31 and P32 are programmable as rising, falling or both edge-triggered interrupts (IRQ register bits 6 and 7). P33 is the comparator reference voltage input. Access to counter/timers 1 is through P31 (T_{IN}) and P36 (T_{OUT}).

Handshake lines for Ports 0, 1, and 2 are available on P31 through P36.

Port 3 also provides the following control functions: handshake for Ports 0, 1, and 2 (/DAV and RDY); three external interrupt request signals (IRQ3-IRQ1); timer input and output signals (T_{IN} and T_{OUT}); (Figure 13).

Comparator Inputs. Port 3, Pins P31 and P32 each have a comparator front end. The comparator reference voltage, Pin P33, is common to both comparators. In analog mode, the P31 and P32 are the positive inputs to the comparators and P33 is the reference voltage supplied to both comparators. In digital mode, pin P33 can be used as a P33 register input or IRQ1 source.

Table 3. Port 3 Pin Assignments

Pin	I/O	CTC1	AN IN	Int.	P0 HS	P1 HS	P2 HS	EXT
P31	IN	T _{IN}	AN1	IRQ2			D/R	
P32	IN		AN2	IRQ0	D/R			
P33	IN		REF	IRQ1		D/R		
P34	OUT					R/D		DM
P35	OUT				R/D			
P36	OUT	T _{OUT}					R/D	
P37	OUT							

Notes:

HS = Handshake Signals
D = DAV
R = RDY

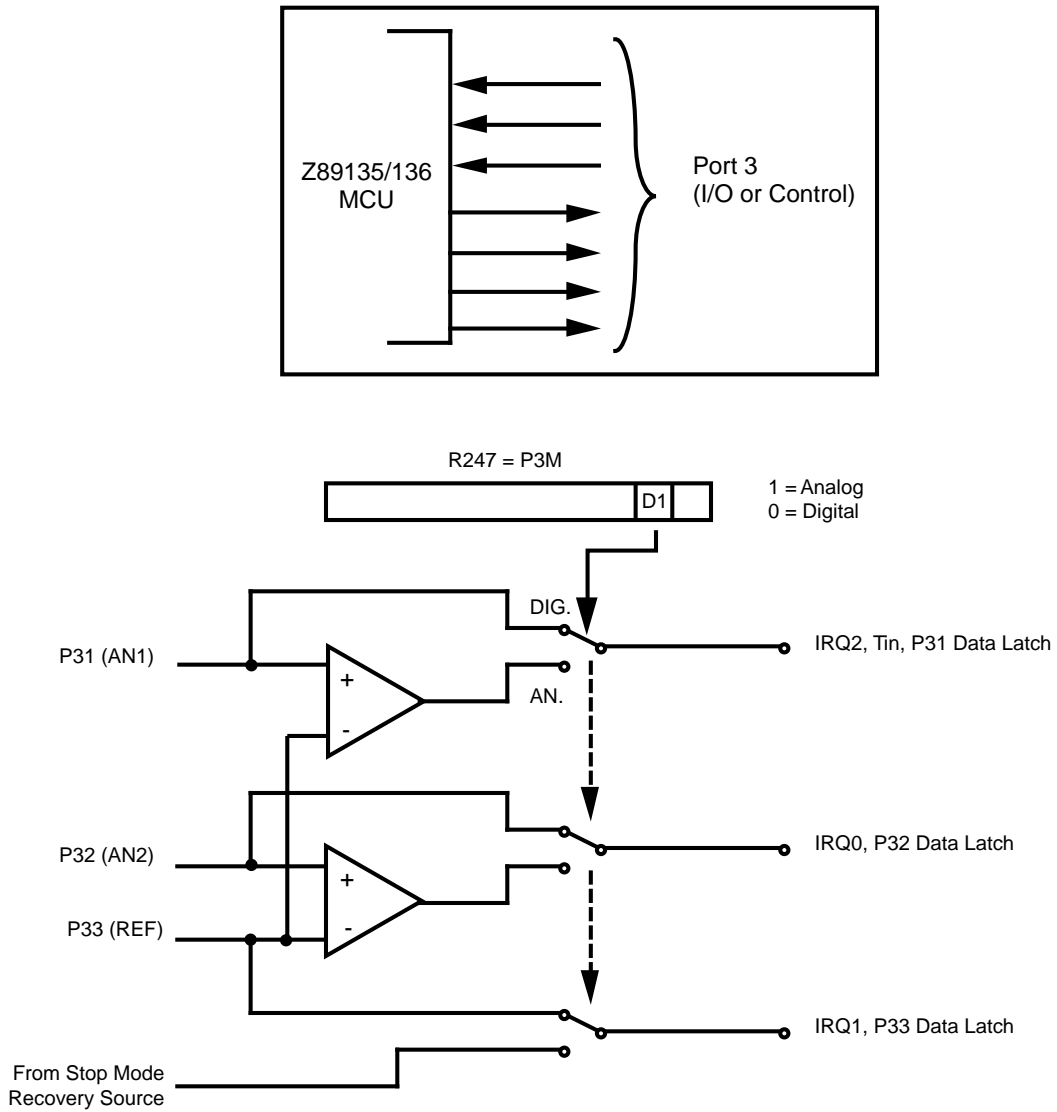


Figure 13. Port 3 Configuration

PIN FUCTIONS (Continued)

Port 4. (P47-P40). Port 4 is an 8-bit, bidirectional, CMOS-compatible I/O port (Figure 14). These eight I/O lines are configured under software control as an input or output, independently. Port 4 is always available for I/O operation. The input buffers are Schmitt-triggered. Bits programmed as outputs may be globally programmed as either push-pull or open-drain.

Port 4 is a bit programmable general-purpose I/O port. The control registers for Port 4 are mapped into the expanded register file (Bank F) of the Z8.

Auto Latch. The Auto Latch on Port 4 puts valid CMOS levels on all CMOS inputs which are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

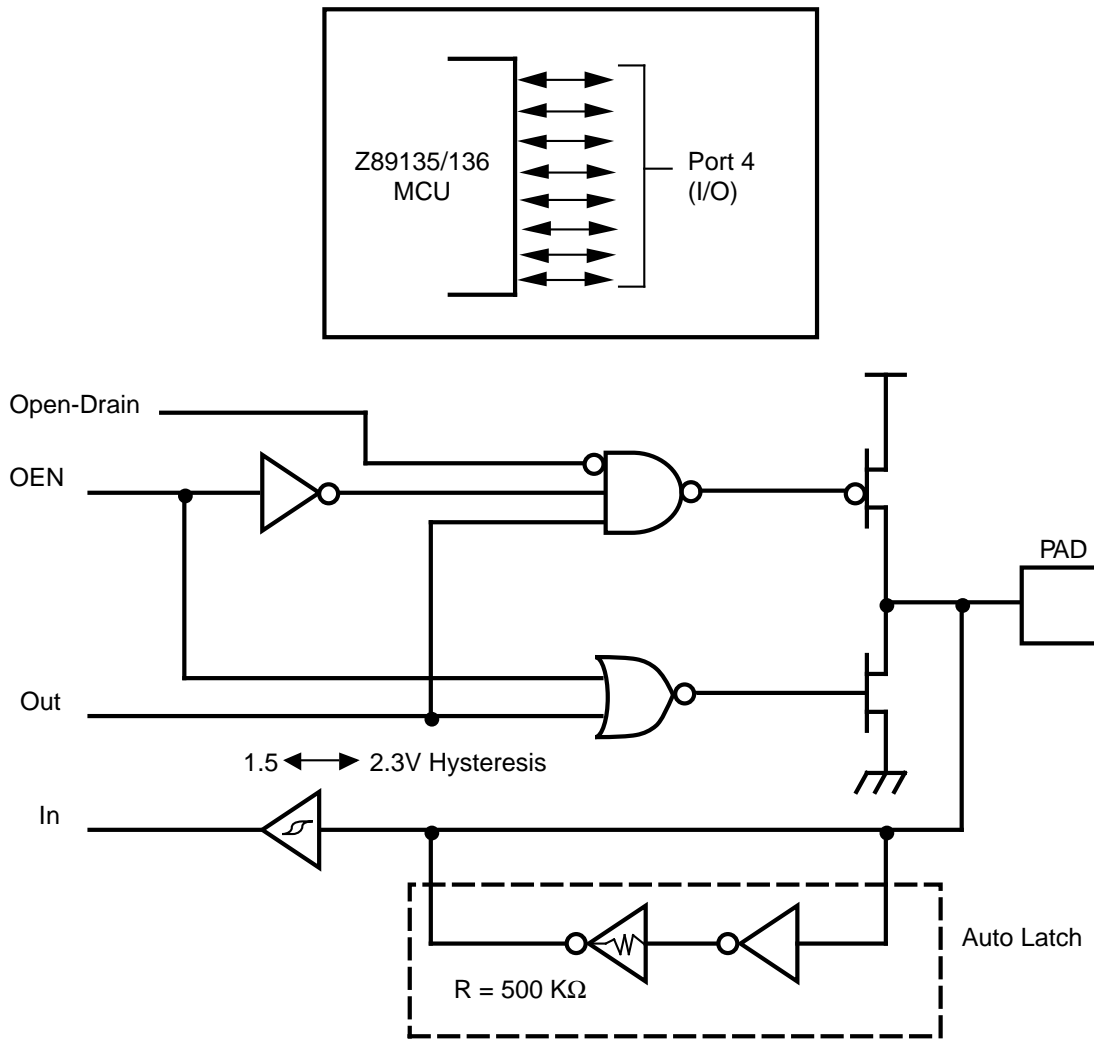


Figure 14. Port 4 Configuraton

Port 5. (P57-P50). Port 5 is an 8-bit, bidirectional, CMOS-compatible I/O port (Figure 15). These eight I/O lines are configured under software control as an input or output, independently. Port 5 is always available for I/O operation. The input buffers are Schmitt-triggered. Bits programmed as outputs may be globally programmed as either push-pull or open-drain.

Port 5 is a bit programmable general-purpose I/O port. The control registers for Port 5 are mapped into the expanded register file (Bank F) of the Z8.

Auto Latch. The Auto Latch on Port 5 puts valid CMOS levels on all CMOS inputs which are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

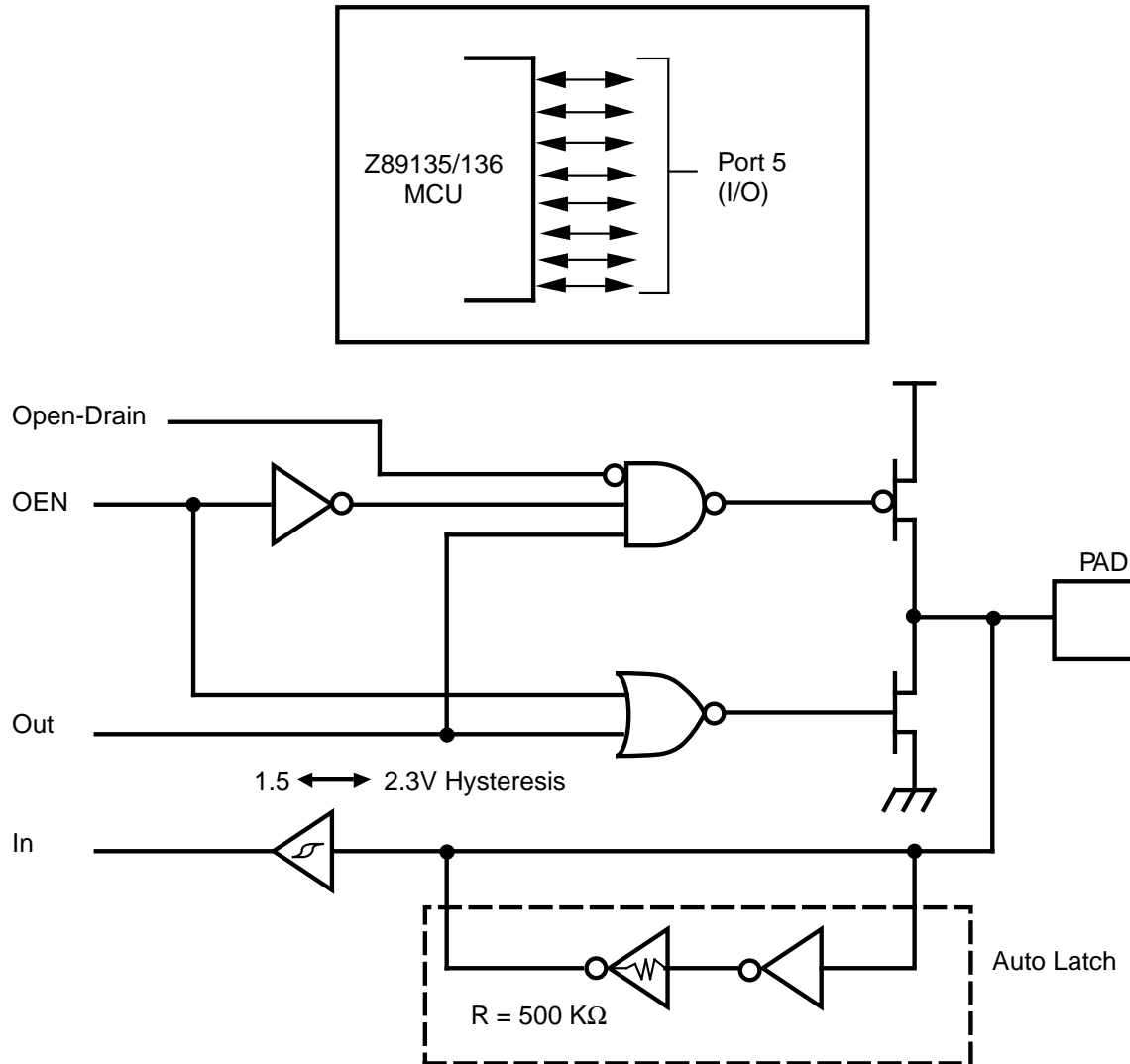


Figure 15. Port 5 Configuration

FUNCTIONAL DESCRIPTION

The Z8 CCP™ core incorporates special functions to enhance the Z8's application in industrial, scientific research and advanced technologies applications.

Reset. The device is reset in one of the following conditions:

- Power-On Reset
- Watch-Dog Timer
- Stop-Mode Recovery Source
- External Reset

Program Memory. The Z8 addresses up to 24 KB of internal program memory and 40 KB external memory (Figure 16). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the five user interrupts and one DSP interrupt. Byte 12 to byte 24575 consists of on-chip mask-programmed ROM. At addresses 24576 and greater, the Z8 executes external program memory. In ROM-less mode, the Z8 will execute external program memory beginning at byte 12 and continuing through byte 65535.

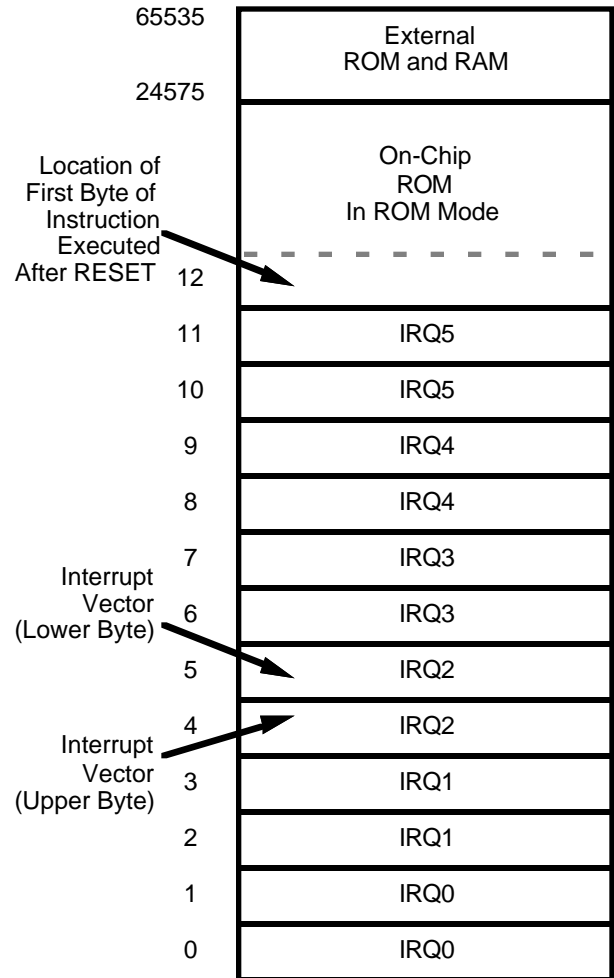


Figure 16. Program Memory Map

ROM Protect. The 24 KB of internal program memory for the Z8 is mask programmable. A ROM protect feature prevents “dumping” of the ROM contents of Program Memory by inhibiting execution of LDC, LDCI, LDE, and LDEI instructions. The ROM Protect option is mask-programmable, to be selected by the customer at the time when the ROM code is submitted.

Data Memory. (/DM). In ROM Mode, the Z8 can address up to 40 KB of external data memory beginning at location 24576 (Figure 17). In ROMless mode, the Z8 can address the full 64 KB of external data memory beginning at location 12. External data memory may be included with, or separated from, the external program memory space. /DM, an optional I/O function that can be programmed to appear on Port 34, is used to distinguish between data and program memory space. The state of the /DM signal is controlled by the type of instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references data (/DM active Low) memory.

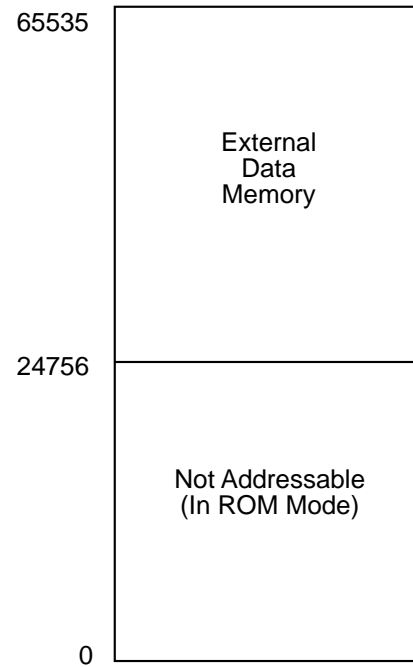


Figure 17. Data Memory Map

FUNCTIONAL DESCRIPTION (Continued)

Register File. The standard Z8 register file consists of four I/O port registers, 236 general-purpose registers, and 15 control and status registers (R3-R0, R239-R4, and R255-R241, respectively). The instructions access registers directly or indirectly through an 8-bit address field. This allows a short, 4-bit register address using the Register Pointer (Figure 18). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group (Figure 19).

Note: Register Group E (Registers E0-EF) is only accessed through a working register and indirect addressing modes.

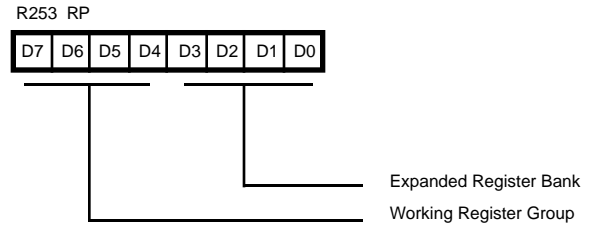


Figure 18. Register Pointer Register

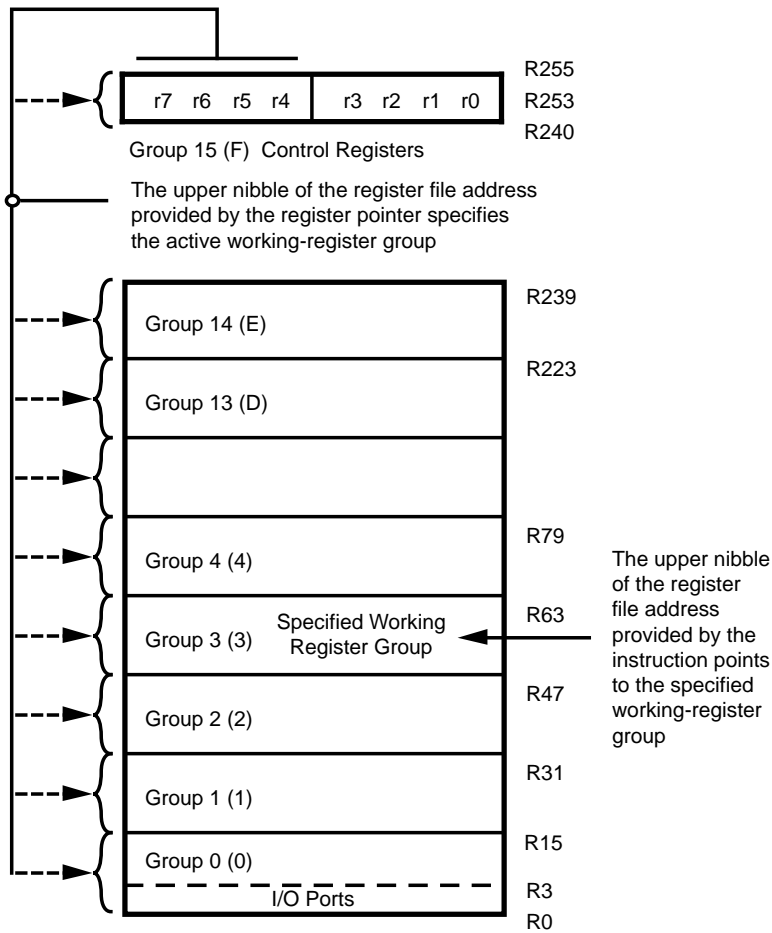


Figure 19. Register Pointer

RAM Protect. The upper portion of the Z8's RAM address spaces 80FH to EFH (excluding the control registers) are protected from reading and writing. The RAM Protect bit option is mask-programmable and is selected by the customer when the ROM code is submitted. After the mask option is selected, the user activates from the internal ROM code to turn off/on the RAM Protect by loading a bit D6 in the IMR register to either a 0 or a 1, respectively. A 1 in D6 indicates RAM Protect enabled.

Stack. The Z8's external data memory or the internal register file is used for the stack. The 16-bit Stack Pointer (R255-R254) is used for the external stack which can reside only from 24576 to 65535 in ROM Mode or 0 to 65535 in ROMless mode. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R239-R4). SPH can be used as a general-purpose register when using internal stack only.

Expanded Register File. The register file on the Z8 has been expanded to allow for additional system control registers, and for mapping of additional peripheral devices along with I/O ports into the register address area. The Z8 register address space has now been implemented as 16 banks of 16 registers groups per bank (Figure 20). These register banks are known as the ERF (Expanded Register File). Bits 7-4 of register RP (Register Pointer) select the working register group. Bits 3-0 of register RP select the expanded register bank (Figure 20).

The SMR register, WDT register, control and data registers for Port 4 and Port 5, and the DSP control register are located in Bank F of the Expanded Register File. Bank B of the Expanded Register File consists of the Mailbox Interface in which the Z8 and the DSP communicate. The rest of the Expanded Register is not physically implemented and is open for future expansion.

FUNCTIONAL DESCRIPTION (Continued)

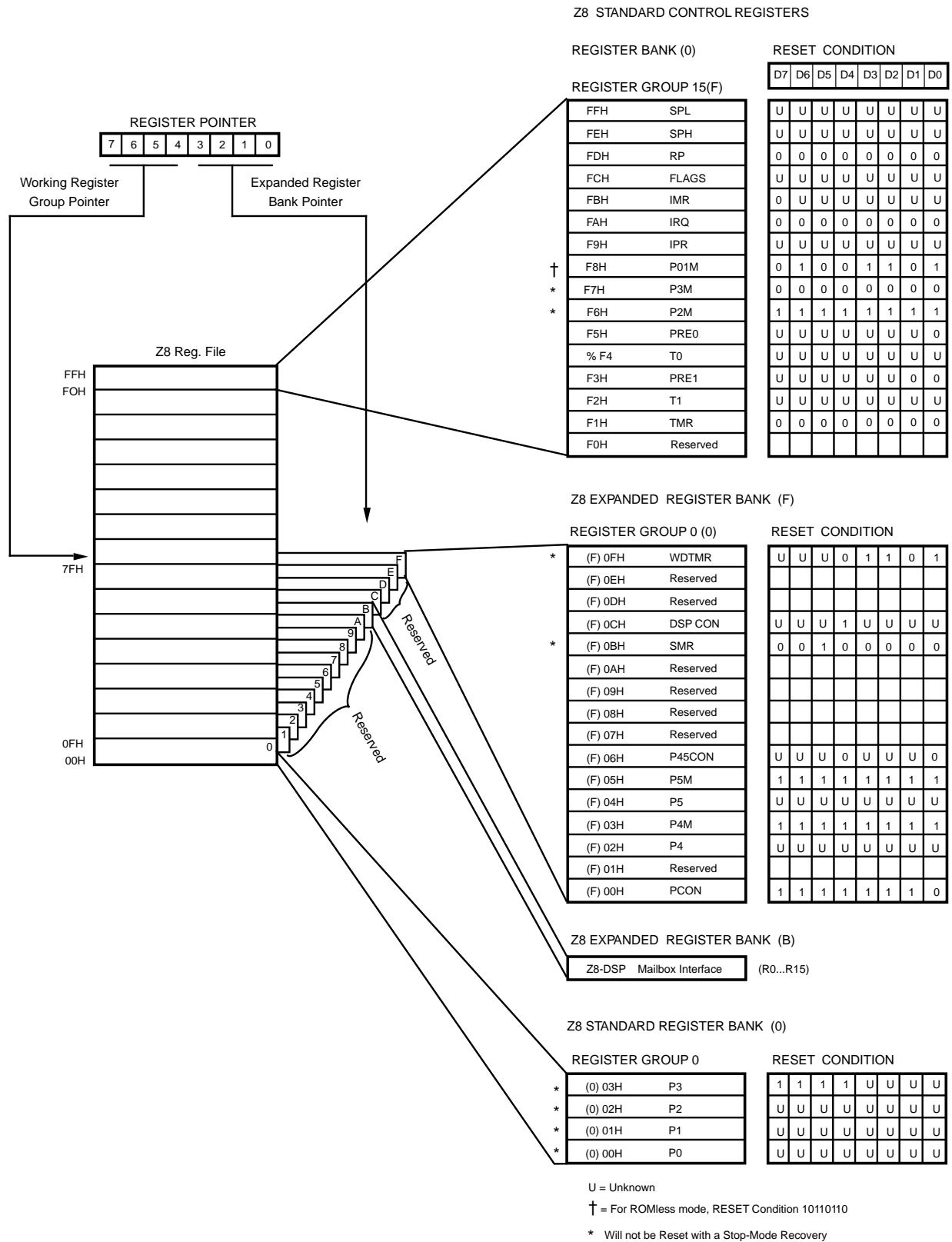


Figure 20. Expanded Register File Architecture

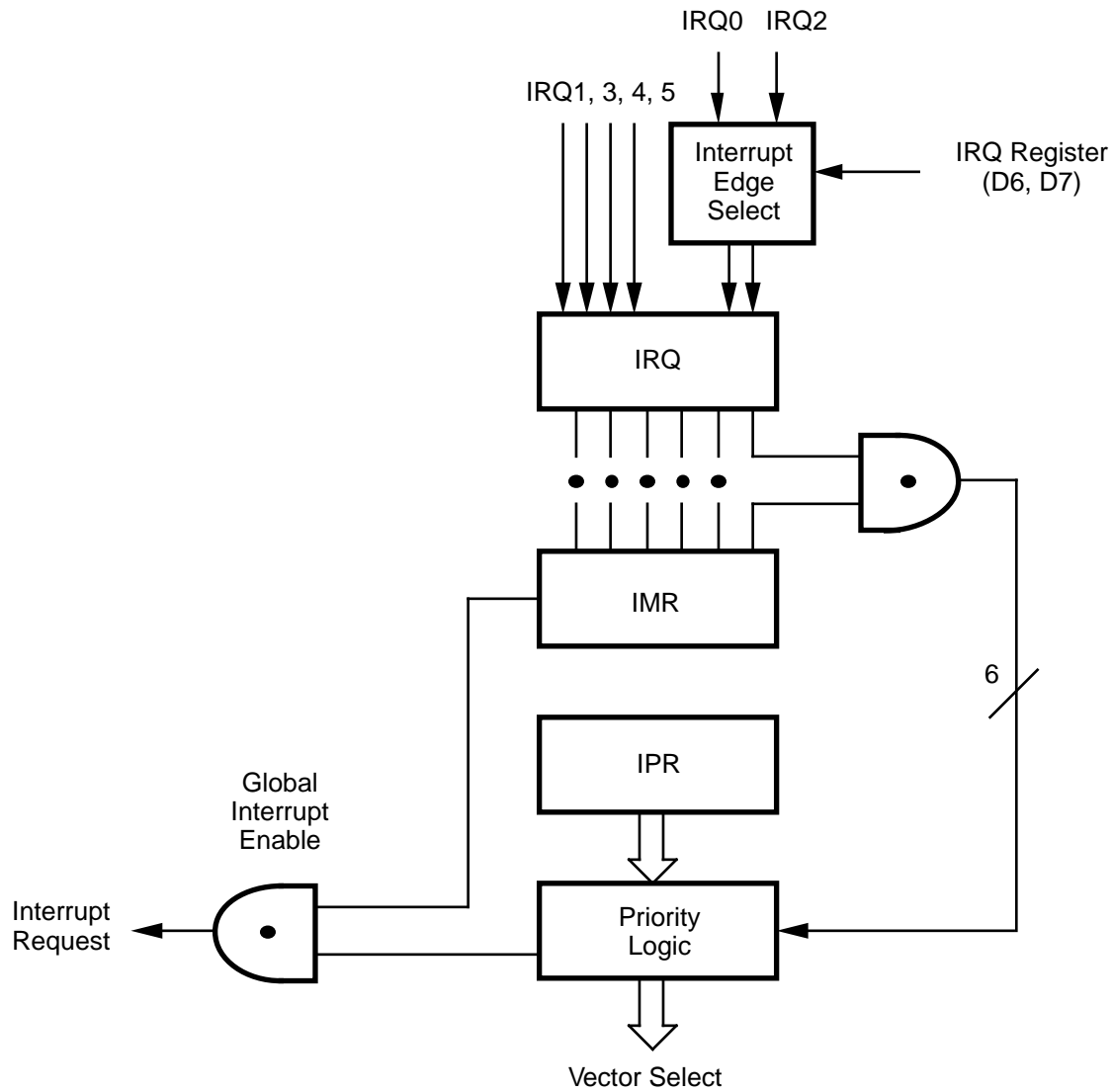


Figure 21. Interrupt Block Diagram

Table 4. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	/DAV0, P32, AN2	0, 1	External (P32), Programmable Rise or Fall Edge Triggered
IRQ1	/DAV1, P33	2, 3	External (P33), Fall Edge Triggered
IRQ2	/DAV2, P31, T _{IN} , AN2	4, 5	External (P31), Programmable Rise or Fall Edge Triggered
IRQ3	IRQ3	6, 7	Internal (DSP activated), Fall Edge Triggered
IRQ4	T0	8, 9	Internal
IRQ5	TI	10, 11	Internal

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z8 has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 21). The six sources are divided as follows; three sources are claimed by Port 3 lines P33-P31, two in counter/timers, and one by the DSP (Table 4). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority Register. An interrupt machine cycle is activated when an interrupt request is granted. This disables all subsequent interrupts, pushes the Program Counter and Status Flags to the stack, and then branches to the program memory vector location reserved for that interrupt.

All Z8 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request Register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling or both edge triggered, and are programmable by the user. The software may poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select is located in the IRQ Register (R250), bits D7 and D6. The configuration is shown in Table 5.

Table 5. IRQ Register

IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:

F = Falling Edge

R = Rising Edge

Clock. The Z89135/136 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 20.48 MHz max., with a series resistance (RS) less than or equal to 100 Ohms. The system clock (SCLK) is one half the crystal frequency.

The crystal is connected across XTAL1 and XTAL2 using capacitors from each pin to ground.

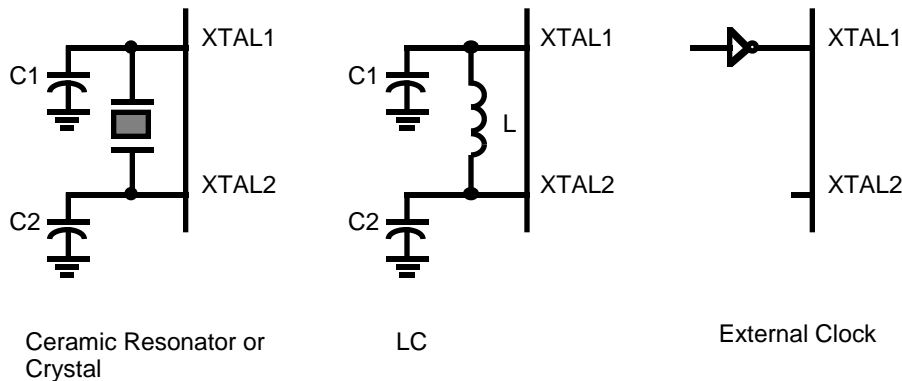


Figure 22. Oscillator Configuration

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 23).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single

pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input through Port 31. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. The counter/timers can be cascaded by connecting the T0 output to the input of T1.

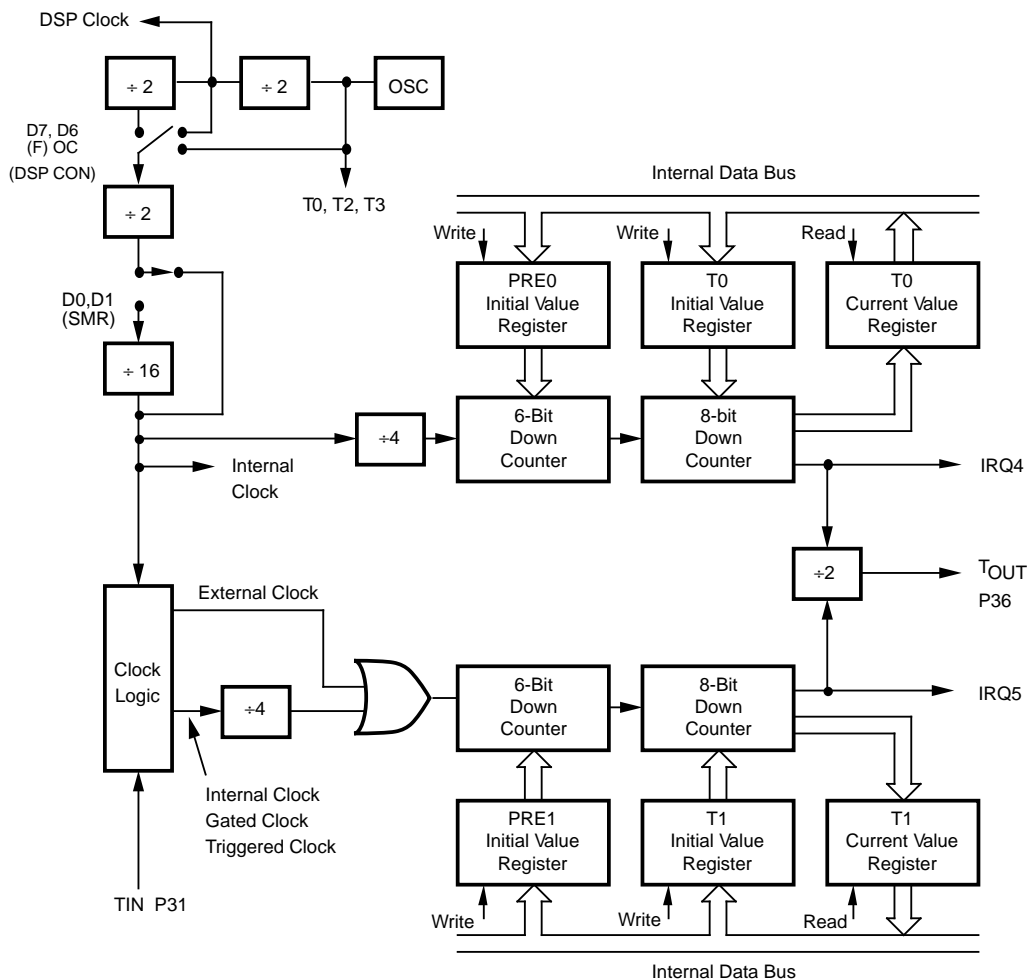
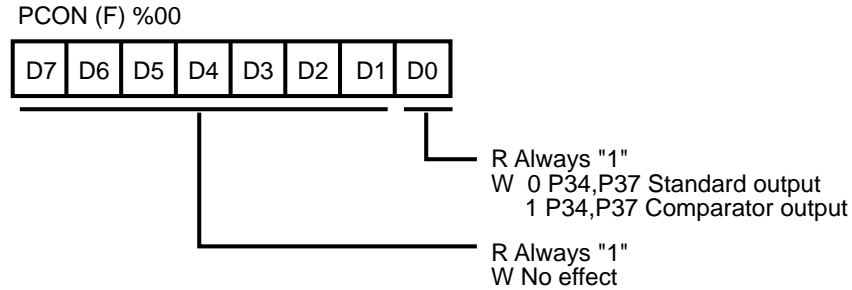


Figure 23. Counter/Timer Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Port Configuration Register (PCON). The PCON register configures the port individually; comparator output is on Port 3. The PCON register is located in the Expanded Register File at Bank F, location 00H (Figure 24).

Comparator Output Port 3 (D0). Bit 0 controls the comparator use in Port 3. A 1 in this location brings the comparator outputs to P34 and P35, and a 0 releases the Port to its standard I/O configuration.



Note: Reset condition is 11111110

Figure 24. Port Configuration Register (PCON)

Port 4 and 5 Configuration Register (P45CON). The P45CON register configures Port 4 and Port 5, individually, to open-drain or push-pull active. This register is located in the Expanded Register File at Bank F, location 06H (Figure 25).

push-pull active by setting this bit (D0 = 1). The default value is 1.

Port 4 Open-Drain (D0). Port 4 can be configured as an open-drain by resetting this bit (D0 = 0) or configured as

Port 5 Open-Drain (D4). Port 5 can be configured as an open-drain by resetting this bit (D4 = 0) or configured as push-pull active by setting this bit (D4 = 1). The default value is 1.

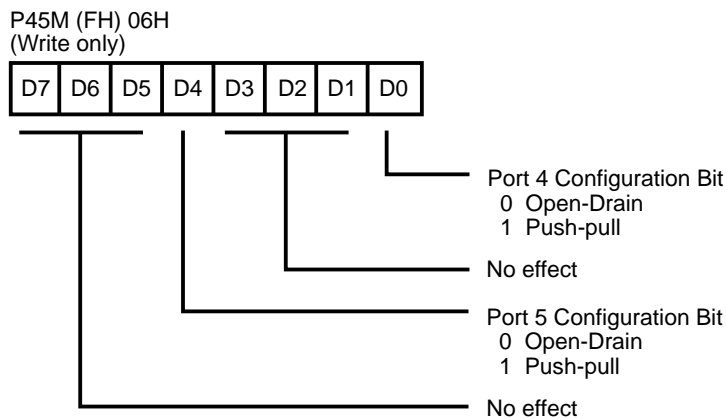


Figure 25. Port 4 and 5 Configuration Register (F) 06H (Write Only)

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power fail to Power OK status
- Stop-Mode Recovery (if D5 of SMR=1)
- WDT time-out.

The POR time is a nominal 5 ms. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock, RC/LC oscillators).

HALT. HALT turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated.

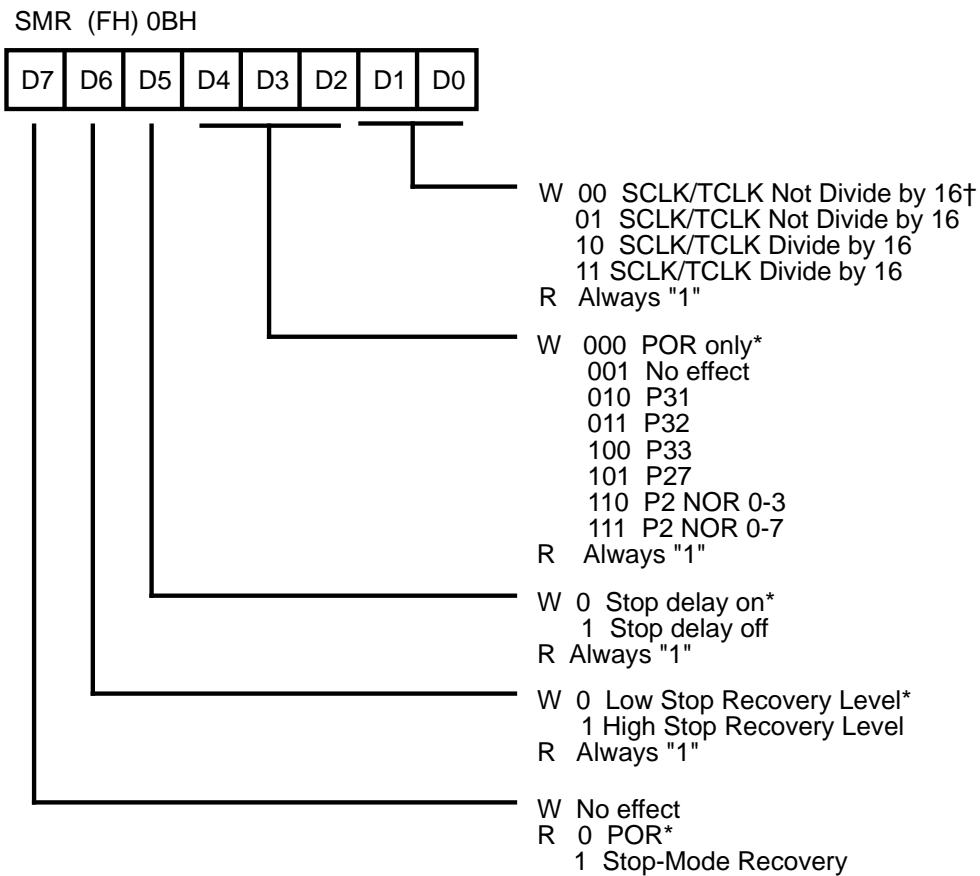
STOP. This instruction turns off the internal clock and external crystal oscillation. It reduces the standby current to 300 μ A or less. The STOP Mode is terminated by a reset only, either by WDT time-out, POR, SMR recovery or external reset. This causes the processor to restart the application program at address 000CH. In order to enter STOP (or HALT) Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode=FFH) immediately before the appropriate sleep instruction, for example:

FF	NOP	;clear the pipeline
6F	STOP	;enter STOP Mode or
FF	NOP	;clear the pipeline
7F	HALT	;enter HALT Mode

FUNCTIONAL DESCRIPTION (Continued)

Stop-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 26). All bits are Write Only, except bit 7 which is Read Only. Bit 7 is a flag bit that is hardware set on the condition of Stop recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level is required from the recovery source. Bit 5 con-

trols the reset delay after recovery. Bits 2, 3, and 4, or the SMR register, specify the source of the Stop-Mode Recovery signal. Bits 0 and 1 determine the time-out period of the WDT. The SMR is located in Bank F of the Expanded Register Group at address 0BH.



* Default Setting After Reset
† Reset After Stop-Mode Recovery

Figure 26. Stop-Mode Recovery Register (SMR)

SCLK/TCLK divide-by-16 Select (D0). D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK

control) and/or HALT Mode (where TCLK sources counter/timers and interrupt logic).

Stop-Mode Recovery Source (D4-D2). These three bits of the SMR specify the wake-up source of the Stop-Mode Recovery (Figure 27 and Table 6).

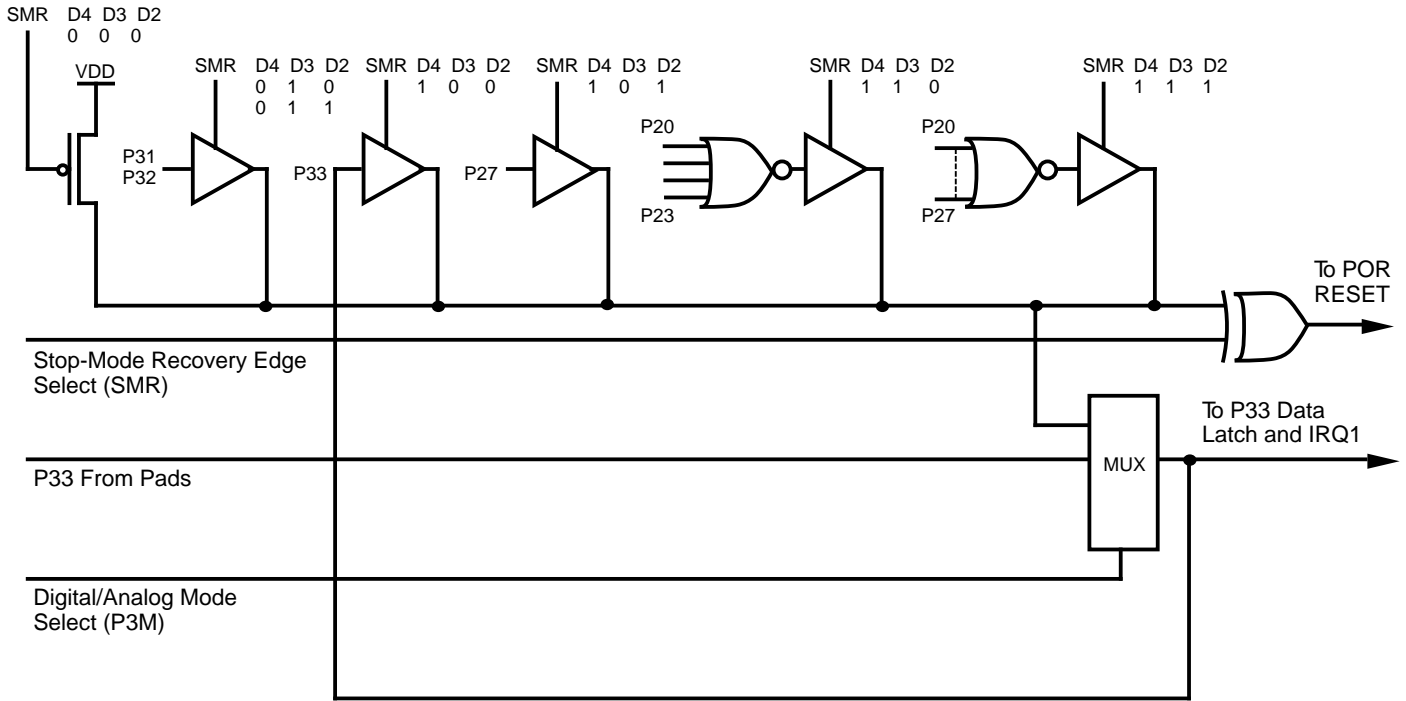


Figure 27. Stop-Mode Recovery Source

Table 6. Stop-Mode Recovery Source

SMR:432			Operation Description of Action
D4	D3	D2	
0	0	0	POR and/or external reset recovery
0	0	1	No effect
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

Stop-Mode Recovery Delay Select (D5). This bit, if High, disables the 5 ms /RESET delay after Stop-Mode Recovery. The default configuration of this bit is one. If the “fast” wake-up is selected, the Stop-Mode Recovery source is kept active for at least 5 TpC.

Stop-Mode Recovery Edge Select (D6). A 1 in this bit position indicates that a high level on any one of the recovery sources wakes the Z89165 from STOP Mode. A 0 indicates low level recovery. The default is 0 on POR .

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. It is active High, and is 0 (cold) on POR/WDT /RESET. This bit is Read Only. It is used to distinguish between cold or warm start.

FUNCTIONAL DESCRIPTION (Continued)

DSP Control Register (DSPCON). The DSPCON register controls various aspects of the Z8 and the DSP. It can configure the internal system clock (SCLK) or the Z8, RESET,

and HALT of the DSP, and control the interrupt interface between the Z8 and the DSP (Table 7).

**Table 7. DSP Control Register
(F) 0CH [Read/Write]**

Field DSPCON (F)0CH	Position	Attrib	Value	Label
Z8_SCLK	76-----	R/W	00	2.5 MHz (OSC/8)
			01	5 MHz (OSC/4)
			1x	10 MHz (OSC/2)
DSP_Reset	--5-----	R W		Return "0"
			0	No effect
			1	Reset DSP
DSP_Run	---4----	R/W	0	HALT_DSP
			1	Run_DSP
Reserved	----32--	W R		No effect
				Return "0"
				No effect
IntFeedback	-----1-	R W		FB_DSP_INT2
			1	Set DSP_INT2
			0	No effect
IntFeedback	-----0	R W		FB_Z8_IRQ3
			1	Clear IRQ3
			0	No effect

Z8 IRQ3 (D0). This bit, when read, indicates the status of Z8 IRQ3. Z8 IRQ3 is set by the DSP by writing to D9 of DSP External Register 4 (ICR). By writing a 1 to this bit, Z8 IRQ3 is Reset.

DSP INT2 (D1). This bit is linked to DSP INT2. Writing a 1 to this bit sets DSP INT2. Reading this bit indicates the status of DSP INT2.

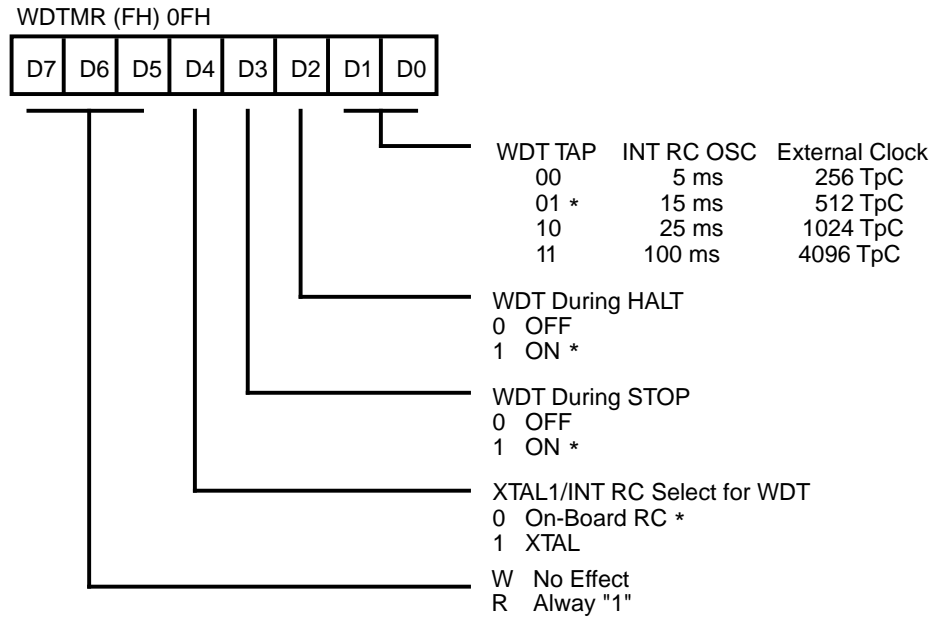
DSP RUN (D4). This bit defines the HALT Mode of the DSP. If this bit is set to 0, then the DSP clock is turned off to minimize power consumption. After this bit is set to 1, then the DSP will continue code execution from where it was halted. After a hardware reset, this bit is reset to 1.

DSP RESET (D5). Setting this bit to 1 will reset the DSP. If the DSP was in HALT Mode, this bit is automatically pre-set to 1. Writing a 0 has no effect.

Z8 SCLK (D8-D7). These bits define the SCLK frequency of the Z8. The oscillator can be divided by 8, 4, or 2. After a reset, both of these bits are defaulted to 00.

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit

is driven by an on-board RC oscillator or external oscillator from the XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register (Figure 28). The WDTMR is accessible only within 64 Z8 clock cycles after POR.



* Default setting after RESET

Figure 28. Watch-Dog Timer Mode Register

WDT Time Select (D0,D1). Selects the WDT time period. It is configured as shown in Table 8.

Table 8. WDT Time Select

D1	D0	Time-out of Internal RC OSC	Time-out of XTAL clock
0	0	5 ms min	256 TpC
0	1	15 ms min	512 TpC
1	0	25 ms min	1024 TpC
1	1	100 ms min	4096 TpC

Notes:

TpC = XTAL clock cycle
The default on reset is 15 ms.

WDT During Halt (D2). This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1.

WDT During Stop (D3). This bit determines whether or not the WDT is active during STOP Mode. Since XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the POR counter. A 1 indicates active during STOP. The default is 1.

Clock Source for WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0 which selects the RC oscillator

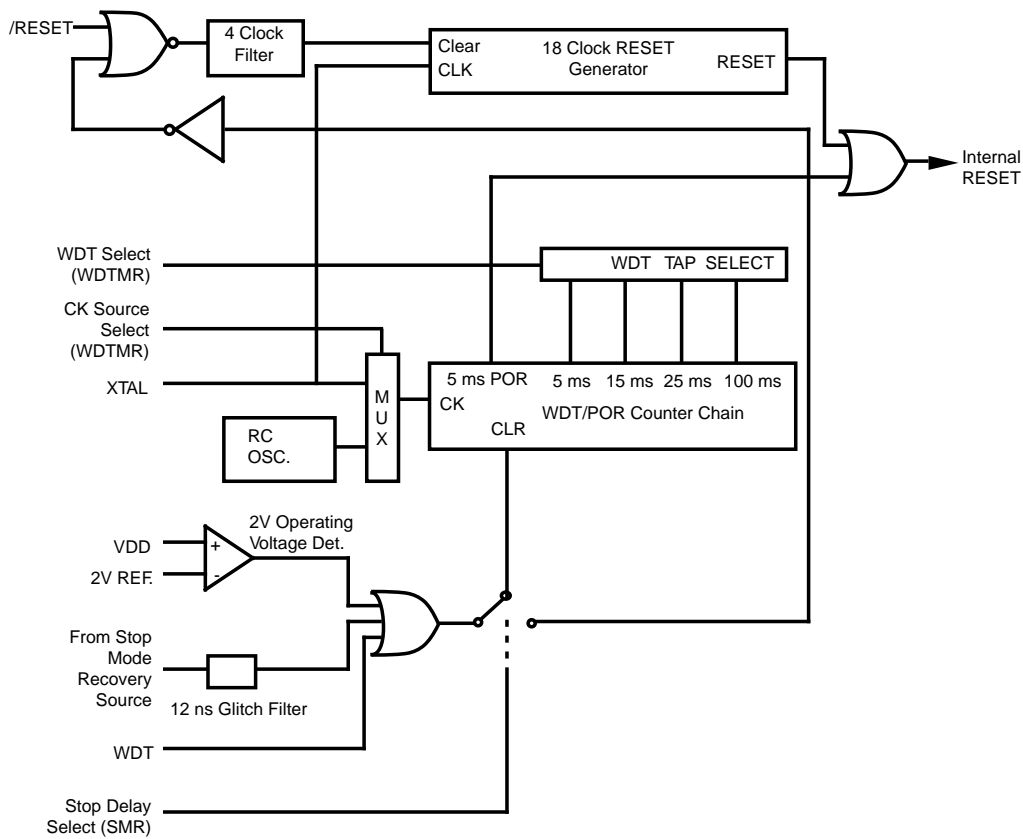


Figure 29. Resets and WDT

DSP REGISTERS DESCRIPTION

General. The DSP is a high-performance second generation CMOS Digital Signal Processor with a modified Harvard-type architecture with separate program and data ports. The design has been optimized for processing power and saving silicon space.

Registers. The DSP has eight internal registers and seven external registers. The external registers are for the A/D and D/A converters, and the mailbox and interrupt interfac-

ing between DSP to the Z8. External registers are accessed in one machine cycle, the same as internal registers.

DSP Registers

There are 15 internal and extended 16-bit registers which are defined in Table 9.

Table 9. DSP Registers

Register	Attribute	Register Definition
BUS	Read	Data-Bus
X	Read/Write	X Multiplier Input, 16-Bit
Y	Read/Write	Y Multiplier Input, 16-Bit
A	Read/Write	Accumulator, 24-Bit
SR	Read/Write	Status Register
SP	Read/Write	Stack Pointer
PC	Read/Write	Program Counter
P	Read	Output of MAC, 24-Bit
EXT0	Read Write	Z8 ERF Bank B, Register 00-01 (from Z8) Z8 ERF Bank B, Register 08-09 (to Z8)
EXT1	Read Write	Z8 ERF Bank B, Register 02-03 (from Z8) Z8 ERF Bank B, Register 0A-0B (to Z8)
EXT2	Read Write	Z8 ERF Bank B, Register 04-05 (from Z8) Z8 ERF Bank B, Register 0C-0D (to Z8)
EXT3	Read Write	Z8 ERF Bank B, Register 06-07 (from Z8) Z8 ERF Bank B, Register 0E-0F (to Z8)
EXT4	Read/Write	DSP Interrupt Control Register
EXT5	Read Write	A/D Converter D/A Converter
EXT6	Read/Write	Analog Control Register

EXT3-EXT0. (External Registers 3-0) are the MailBox Registers in which the DSP and the Z8 communicate. These four 16 bit registers correspond to the eight outgoing and eight incoming 8-bit registers in Bank B of the Z8's Expanded Register File.

EXT4. (DSP Interrupt Control Register (ICR)) controls the interrupts in the DSP as well as the interrupts in common between the DSP and the Z8. It is accessible by the DSP only, except for the bit F and bit 9.

EXT5. (D/A and A/D Data Register) is used by both D/A and A/D converters. The D/A converter will be loaded by writing to this register, while the A/D converter will be addressed by reading from this register. The Register EXT5 is accessible by the DSP only.

EXT6. (Analog Control Register) controls the D/A and A/D converters. It is a read/write register accessible by the DSP only.

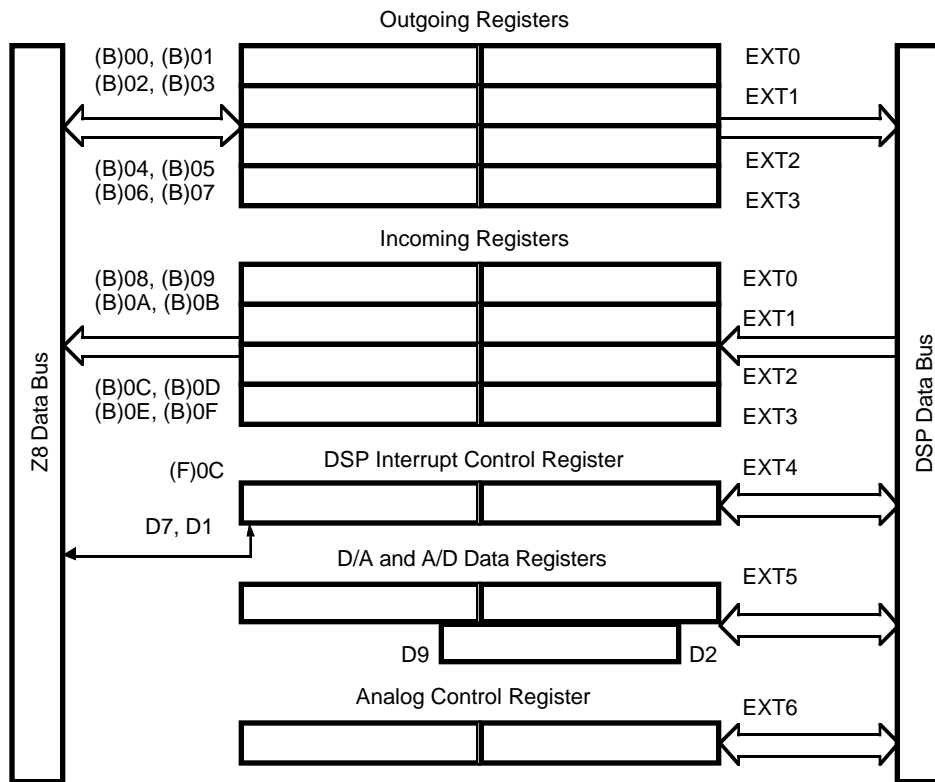


Figure 30. Z8-DSP Interface

DSP-Z8 MAILBOX

To receive information from the DSP, the Z8 uses eight incoming registers which are mapped in the Z8 extended Register File (Bank B, 08 to 0F). The DSP treats these as four 16-bit registers that correspond to the eight incoming Z8 registers (Figure 30).

Both the outgoing registers and the incoming registers share the same DSP address (EXT3-EXT0).

The Z8 can supply the DSP with data through eight outgoing registers mapped into both the Z8 Expanded Register File (Bank B, Registers 00 to 07) and the external register interface of the DSP. These registers are Read/Write and can be used as general-purpose registers of the Z8. The DSP can only read information from these registers. Since the DSP uses a 16-bit data format and the Z8 an 8-bit data format, eight outgoing registers of the Z8 correspond to four DSP registers. The DSP can only read information from the outgoing registers.

Note: The Z8 can read and write to ERF Bank B R00-R07, Registers 08-0F are Read Only from the Z8.

**Table 10. Z8 Outgoing Registers
(Read Only from DSP)**

Field	Position	Attrib	Value	Label
Outgoing [0] (B)00	76543210	R/W	%NN	(B)00/DSP_ext0_hi
Outgoing [1] (B)01	76543210	R/W	%NN	(B)01/DSP_ext0_lo
Outgoing [2] (B)02	76543210	R/W	%NN	(B)02/DSP_ext1_hi
Outgoing [3] (B)03	76543210	R/W	%NN	(B)03/DSP_ext1_lo
Outgoing [4] (B)04	76543210	R/W	%NN	(B)04/DSP_ext2_hi
Outgoing [5] (B)05	76543210	R/W	%NN	(B)05/DSP_ext2_lo
Outgoing [6] (B)06	76543210	R/W	%NN	(B)06/DSP_ext3_hi
Outgoing [7] (B)07	76543210	R/W	%NN	(B)07/DSP_ext3_lo

**Table 11. Z8 Incoming Registers
(Write Only from DSP)**

Field	Position	Attrib	Value	Label
Incoming [8] (B)08	76543210	R	%NN	DSP_ext0_hi
		W		No Effect
Incoming [9] (B)09	76543210	R	%NN	DSP_ext0_lo
		W		No Effect
Incoming [a] (B)0A	76543210	R	%NN	DSP_ext1_hi
		W		No Effect
Incoming [b] (B)0B	76543210	R	%NN	DSP_ext1_lo
		W		No Effect
Incoming [c] (B)0C	76543210	R	%NN	DSP_ext2_hi
		W		No Effect
Incoming [d] (B)0D	76543210	R	%NN	DSP_ext2_lo
		W		No Effect
Incoming [e] (B)0E	76543210	R	%NN	DSP_ext3_hi
		W		No Effect
Incoming [f] (B)0F	76543210	R	%NN	DSP_ext3_lo
		W		No Effect

Table 12. DSP Mailbox Registers

Field	Position	Attrib	Value	Label
DSP_ext0	fedcba9876543210	R	%NNNN	(B)00, (B)01
Mail Box		W		(B)08, (B)09
DSP_ext1	fedcba9876543210	R	%NNNN	(B)02, (B)03
Mail Box		W		(B)0A, (B)0B
DSP_ext2	fedcba9876543210	R	%NNNN	(B)04, (B)05
Mail Box		W		(B)0C, (B)0D
DSP_ext3	fedcba9876543210	R	%NNNN	(B)06, (B)07
Mail Box		W		(B)0E, (B)0F

DSP INTERRUPTS

The DSP processor has three interrupt sources (INT2, INT1, INT0) (Figure 31). These sources have different priority levels (Figure 32). The highest priority, the next lower and the lowest priority level are assigned to INT2, INT1 and INT0, respectively. The DSP does not allow interrupt nesting (interrupting service routines that are currently be-

ing executed). When two interrupt requests occur simultaneously the DSP starts servicing the interrupt with the highest priority level. Figure 33 shows the interprocessor interrupts mechanism.

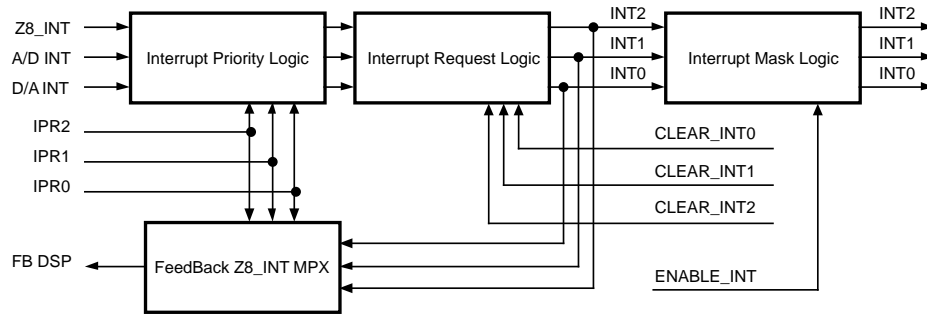


Figure 31. DSP Interrupts

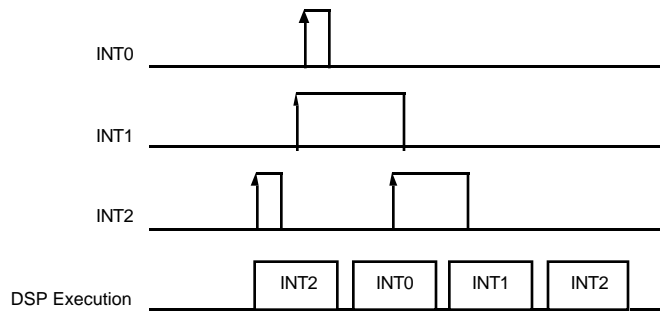


Figure 32. DSP Interrupt Priority Structure

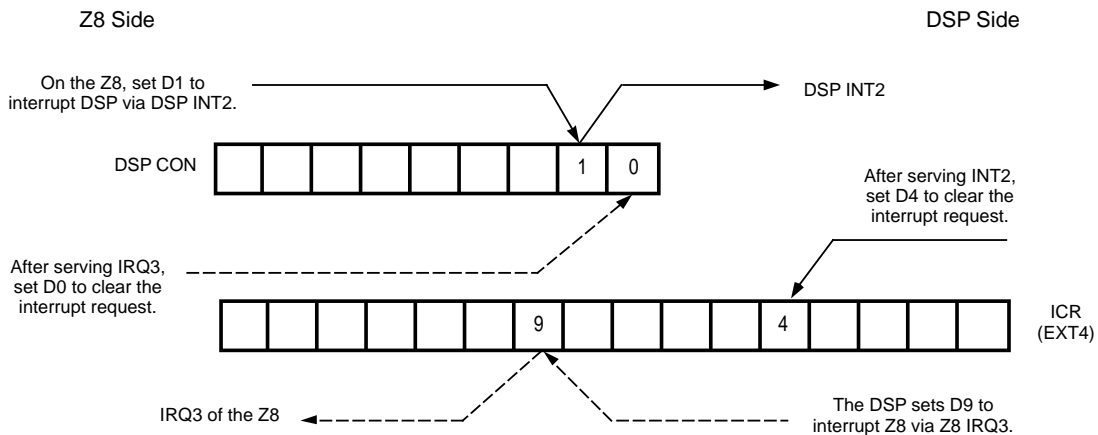


Figure 33. Interprocessor Interrupts Structure

Table 13. EXT4 DSP Interrupt Control Register (ICR) Definition

Field	Position	Attrib	Value	Label	
DSP_IRQ2	f-----	R	1	Set_IRQ2	
			0	Reset_IRQ2	
				No effect	
DSP_IRQ1	-e-----	R	1	Set_IRQ1	
			0	Reset_IRQ1	
				No effect	
DSP_IRQ0	--d-----	R	1	Set_IRQ0	
			0	Reset_IRQ0	
				No effect	
DSP_MaskINT2	---c-----	R/W	1	Enable_INT2	
			0	Disable_INT2	
				No effect	
DSP_MaskINT1	----b-----	R/W	1	Enable_INT1	
			0	Disable_INT1	
				No effect	
DSP_MaskINT0	-----a-----	R/W	1	Enable_INT0	
			0	Disable_INT0	
				No effect	
Z8_IRQ3	-----9-----	R		Return "0"	
			W	1	Set_Z8_IRQ3
				0	Reset_Z8_IRQ3
DSPintEnable	-----8-----	R/W	1	Enable	
			0	Disable	
				No effect	
DSP_IPR2	-----7-----	R/W	Binary	IPR2	
DSP_IPR1	-----6-----	R/W	Binary	IPR1	
DSP_IPR0	-----5-----	R/W	Binary	IPR0	
Clear_IRQ2	-----4----	R		Return "0"	
			W	1	Clear_IRQ2
				0	Has_no_effect
Clear_IRQ1	-----3----	R		Return "0"	
			W	1	Clear_IRQ1
				0	No effect
Clear_IRQ0	-----2--	R		Return "0"	
			W	1	Clear_IRQ0
				0	No effect
Reserved	-----10	W		No effect "0"	
		R		No effect "0"	

Interrupt Control Register (ICR). The ICR is mapped into EXT4 of the DSP (Table 13). The bits are defined as follows:

DSP_IRQ2 (Z8 Interrupt). This bit can be read by both Z8 and DSP and can be set only by writing to the Z8 expanded Register File (Bank F, ROC, bit 0). This bit asserts IRQ2 of the DSP and can be cleared by writing to the Clear_IRQ2 bit.

DSP_IRQ1 (A/D Interrupt). This bit can be read by the DSP only and is set when valid data is present at the A/D

output register (conversion done). This bit asserts IRQ1 of the DSP and can be cleared by writing to the Clear_IRQ1 bit.

DSP_IRQ0 (D/A Interrupt). This bit can be read by DSP only and is set by Timer3. This bit asserts IRQ0 of the DSP and can be cleared by writing to the Clear_IRQ0 bit.

DSP_MaskIntX. These bits can be accessed by the DSP only. Writing a 1 to these locations allows the INT to be serviced, while writing a 0 masks the corresponding INT off.

Z8_IRQ3. This bit can be read from both Z8 and DSP and can be set by DSP only. Addressing this location accesses bit D3 of the Z8 IRQ register, hence this bit is not implemented in the ICR. During the interrupt service routine executed on the Z8 side, the User has to reset the Z8_IRQ3 bit by writing a 1 to bit D0 of the DSPCON. The hardware of the Z89165/C66 automatically resets Z8_IRQ3 bit three instructions of the Z8 after 1 is written to its location in register bank 0F. This delay provides the timing synchronization between the Z8 and the DSP sides during interrupts. In summary, the interrupt service routine of the Z8 for IRQ3 should be finished by:

```
LD      ;RP,#%0F
OR      ;r12,#%01
POP     ;RP
IRET    ;
```

DSP Enable_INT. Writing a 1 to this location enables global interrupts of the DSP while writing 0 disables them. A system Reset globally disables all interrupts.

DSP_IPRX. This three-bit group defines the Interrupt Selection logic according to Table 14.

Clear_IRQX. These bits can be accessed by the DSP only. Writing a 1 to these locations rests the corresponding DSP_IRQX bits to 0. Clear_IRQX are virtual bits and are not implemented.

Table 14. DSP Interrupt Selection

DSP_IPR[2-0] 2 1 0	Z8_INT is switched to	A/D_INT is switched to	D/A_INT is switched to
0 0 0	INT2	INT1	INT0
0 0 1	INT1	INT2	INT0
0 1 0	INT2	INT0	INT1
0 1 1	INT1	INT0	INT2
1 0 0	INT0	INT2	INT1
1 0 1	INT0	INT1	INT2
1 1 0	Reserved	Reserved	Reserved
1 1 1	Reserved	Reserved	Reserved

DSP ANALOG DATA REGISTERS

The D/A conversion is DSP driven by sending 10-bit data to the EXT5 of the DSP. The six remaining bits of EXT5 are not used (Figure 34).

A/D supplies 8-bit data to the DSP through the register EXT5 of the DSP. From the 16 bits of EXT5, only bits 2 through 9 are used by the A/D (Figure 35). Bits 0 and 1 are padded with zeroes

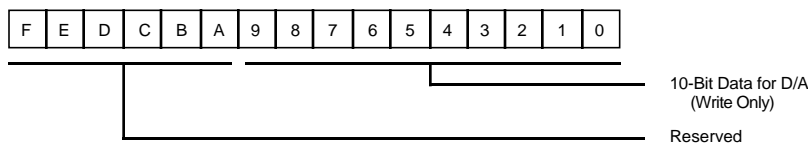


Figure 34. EXT5 Register D/A Mode Definition

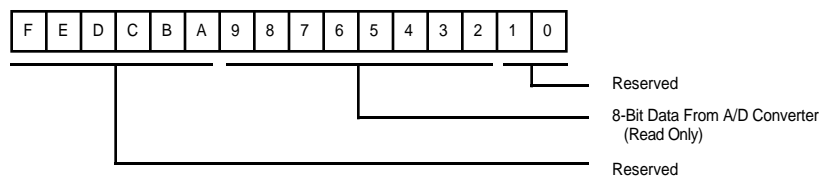


Figure 35. EXT5 Register A/D Mode Definition

ANALOG CONTROL REGISTER (ACR)

The Analog Control register is mapped to register EXT6 of the DSP (Table 15). This read/write register is accessible by the DSP only.

The 16-bit field of EXT6 defines modes of both the A/D and the D/A. The High Byte configures the D/A, while the Low Byte controls the A/D mode.

Table 15. EXT6 Analog Control Register (ACR)

Field	Position	Attrib	Value	Label
MPX_DSP_INT0	f-----	R/W	1	P26
			0	Timer3
Reserved	-edcb-----	R		Return "0"
		W		No Effect
D/A_SamplingRate	-----a98-----	R/W	11x	Reserved
			101	Reserved
			100	64 kHz
			010	16 kHz
			011	10 kHz
			001	4 kHz
			000	Reserved
DSP_port	-----76-----	R/W		User defined DSP Outputs
Enable A/D	-----5-----	R/W	1	A/D Enabled
			0	A/D Disabled
ConversionDone	-----4-----	W		No effect
		R	1	Done
StartConversion	-----3-----	R/W	1	Start
			0	Wait Timer
A/D_SamplingRate	-----210-----	R/W	11x	Reserved
			101	Reserved
			100	128 kHz
			010	64 kHz
			011	32 kHz
			001	16 kHz
			000	8 kHz

DSP IRQ0. This bit defines the source of DSP IRQ0 interrupt.

D/A_Sampling Rate. This field defines the sampling rate of the D/A output. It changes the period to Timer3 interrupt and the maximum possible accuracy of the D/A (Table 16).

Table 16. D/A Data Accuracy

D/A_Sampling Rate	D/A Accuracy	Sampling Rate
1 0 0	64 kHz	8 Bits
0 1 0	16 kHz	10 Bits
0 1 1	10 kHz	10 Bits
0 0 1	4 kHz	10 Bits

DSP0. DSP0 is a general-purpose output pin connected to Bit 6. This bit has no special significance and may be used to output data by writing to bit 6.

DSP1. DSP1 is a general-purpose output pin connected to Bit 7. This bit has no special significance and may be used to output data by writing to bit 7.

Enable A/D. Writing a 0 to this location disables the A/D converter, a 1 will enable it. A hardware reset forces this bit to be 0.

Conversion Done. This Read Only flag indicates that the A/D conversion is complete. Upon reading EXT5 (A/D data), the Conversion Done flag is cleared.

Start A/D Conversion. Writing a 1 to this location immediately starts one conversion cycle. If this bit is reset to 0 the input data is converted upon successive Timer2 time-outs. A hardware reset forces this bit to be 1.

A/D_Sampling Rate. This field defines the sampling rate of the A/D. It changes the period of Timer2 interrupt (Table 17).

Table 17. A/D Sampling Rate

A/D_Sampling Rate	ADC Sampling Rate
1 0 0	128 kHz
0 1 1	64 kHz
0 1 0	32 kHz
0 0 1	16 kHz
0 0 0	8 kHz

DSP TIMERS

Timer2 is a free running counter that divides the XTAL frequency (20.48 MHz) to support different sampling rates for the A/D converter. The sampling rate is defined by the Analog Control Register. Upon reaching the end of a count, the timer generates an interrupt request to the DSP.

Analogous to Timer2, Timer3 generates the different sampling rates for the D/A converter. Timer3 also generates an interrupt request to the DSP upon reaching its final count value (Figure 36).

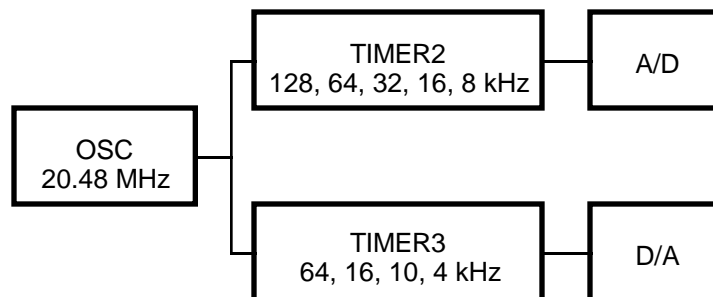


Figure 36. Timer2 and Timer3

PULSE WIDTH MODULATOR (PWM)

The PWM supports four different sampling rates (4, 10, 16, and 64 kHz), according to the settings of Bit 8, 9, 10 of the ACR. The output of PWM can be assigned to logic 1 only during the active region (which is 4/5 of the output signal period). The output will be at logic 0 for the rest of the time. An exception occurs in 10 kHz PWM, where the active region covers the whole output signal period (Figure 37). The active region is divided into 1024 time slots. In each of these time slots, the output can be set to logic 1 or logic 0.

In order to increase the effective sampling rate, the PWM employs a special technique of distributing the “logic 1” period over the active region.

The 10-bit PWM data is divided into two parts: the upper 5 bits (High_Val) and the lower 5 bits (Low_Val). The 1024 time slots in the active region are divided into 32 equal groups, with 32 time slots in each group. The first slot of each of the 32 groups represents Low_Val, while High_Val

is represented by the remaining 31 time slots in each group.

For example, a value of %13a is loaded into PWM data register EXT 5:

$$\%13a = 01\ 0011\ 1010B = 314$$

$$\text{High_Val} = 01001B = 9$$

$$\text{Low_Val} = 11010B = 26$$

26 out of 32 groups will then have their first slots set to logic 1. The remaining slots in each group have 9 time slots set to logic 1.

For 10 kHz PWM, the effective output frequency is $10K \times 32 = 320\text{ kHz}$. Figure 38 illustrates the waveform by using a 6-bit PWM data (3-bit High_Val and 3-bit Low_Val).



Figure 37. PWM Waveform
(shaded area shows the active region)



Figure 38. PWM Waveform of the Active Region
(for a 6-bit PWM data)

A/D CONVERTER (ADC)

Analog To Digital Converter

The A/D converter is an 8-bit half flash converter which uses two reference resistor ladders for its upper four bits (MSBs) and lower four bits (LSBs) conversion. Two reference voltage pins, V_{REF+} (High) and V_{REF-} (Low), are provided for external reference voltage supplies. During the sampling period, the converter is auto-zeroed before starting the conversion time depending on the external clock frequency and the selection of the A/D sampling rate. The

sampling rates are in the order of 8, 10, 16, 64, or 128 kHz (XTAL = 20.48 MHz) in order to provide oversampling. The rates are software controlled by the ACR (DSP External Register 6). Timer2 supports the ADC. The maximum conversion time is 2 μ s.

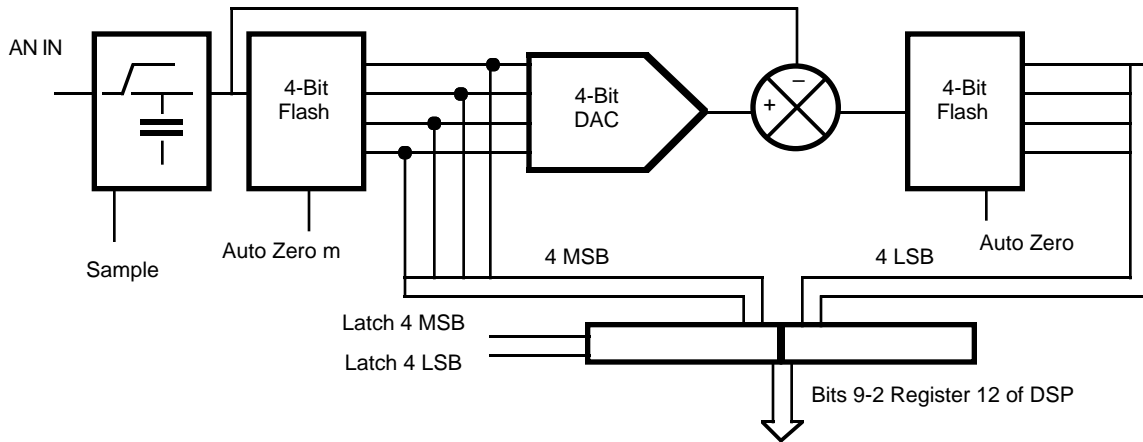


Figure 39. A/D Converter

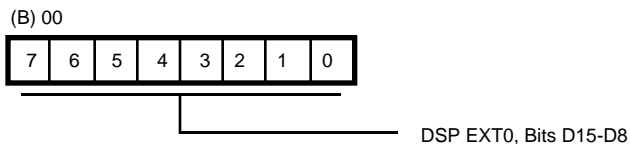
Conversion begins by writing to the appropriate bit in the Analog Control Register (ACR). The start commands are implemented in such a way as to begin a conversion at any time. If a conversion is in progress and a new start command is received, then the conversion in progress is aborted and a new conversion initiated. This allows the programmed values to be changed without affecting a conversion in progress. The new values take effect only after a new start command is received.

The ADC can be disabled (for low power) or enabled by an analog Control Register bit.

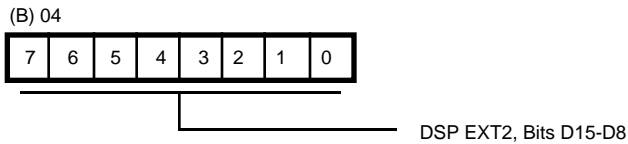
Though the ADC functions for a smaller input voltage and voltage reference, the noise and offsets remain constant over the specified electrical range. The errors of the converter will increase and the conversion time may also take slightly longer due to smaller input signals.

Z8 EXPANDED REGISTER FILE REGISTERS

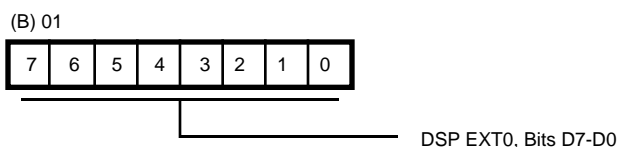
Expanded Register Bank B



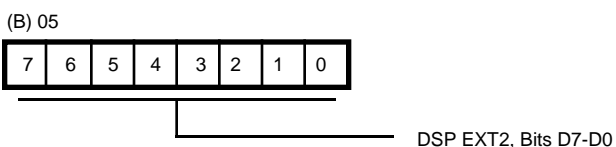
**Figure 40. Outgoing Register to DSP EXT0 (High Byte)
(B) 00H [Read/Write]**



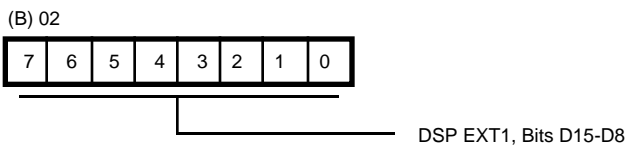
**Figure 44. Outgoing Register to DSP EXT2 (High Byte)
(B) 04H [Read/Write]**



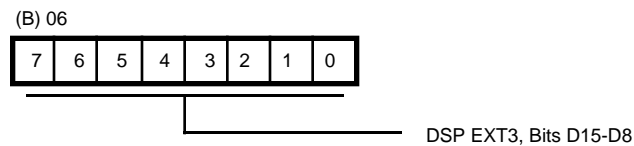
**Figure 41. Outgoing Register to DSP EXT0 (Low Byte)
(B) 01H [Read/Write]**



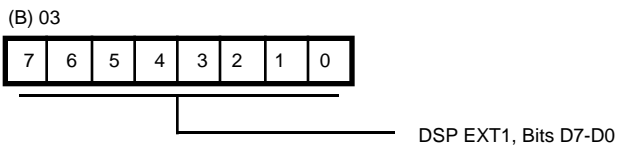
**Figure 45. Outgoing Register to DSP EXT2 (Low Byte)
(B) 05H [Read/Write]**



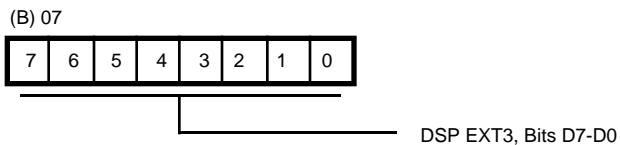
**Figure 42. Outgoing Register to DSP EXT1 (High Byte)
(B) 02H [Read/Write]**



**Figure 46. Outgoing Register to DSP EXT3 (High Byte)
(B) 06H [Read/Write]**

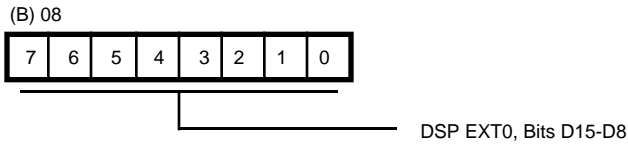


**Figure 43. Outgoing Register to DSP EXT1 (Low Byte)
(B) 03H [Read/Write]**

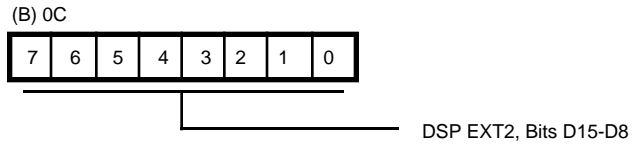


**Figure 47. Outgoing Register to DSP EXT3 (Low Byte)
(B) 07H [Read/Write]**

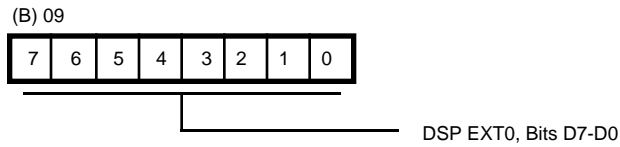
Z8 EXPANDED REGISTER FILE REGISTERS (Continued)



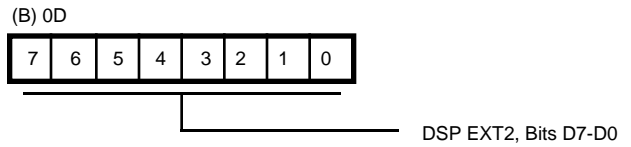
**Figure 48. Incoming Register to DSP EXT0
(High Byte)
(B) 08H [Read/Write]**



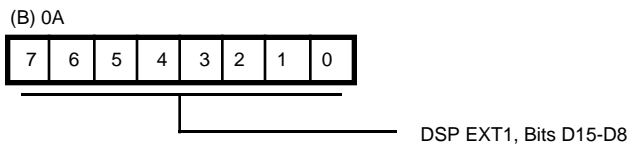
**Figure 52. Incoming Register to DSP EXT2
(High Byte)
(B) 0CH [Read/Write]**



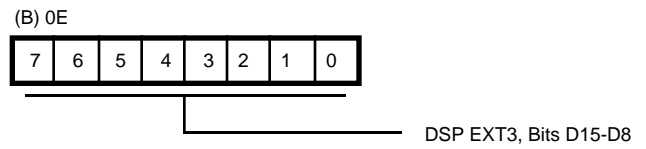
**Figure 49. Incoming Register to DSP EXT0
(Low Byte)
(B) 09H [Read/Write]**



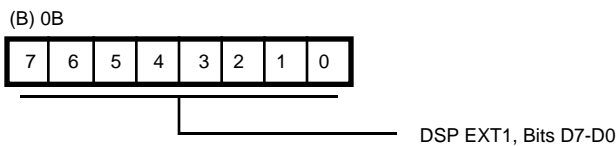
**Figure 53. Incoming Register to DSP EXT2
(Low Byte)
(B) 0DH [Read/Write]**



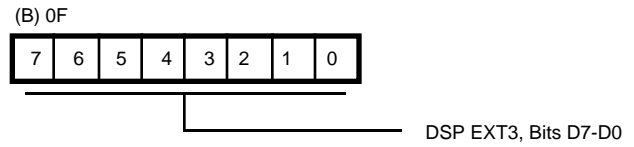
**Figure 50. Incoming Register to DSP EXT1
(High Byte)
(B) 0AH [Read/Write]**



**Figure 54. Incoming Register to DSP EXT3
(High Byte)
(B) 0EH [Read/Write]**



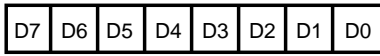
**Figure 51. Incoming Register to DSP EXT1
(Low Byte)
(B) 0BH [Read/Write]**



**Figure 55. Incoming Register to DSP EXT3
(Low Byte)
(B) 0FH [Read/Write]**

Expanded Register Bank F

PCON (FH) 00H

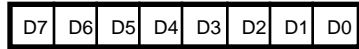


- R Always "1"
- W 0 P34,P37 Standard output
- 1 P34,P37 Comparator output
- R Always "1"
- W No effect

Note: Reset condition is 11111110

Figure 56. Port Configuration Register (PCON) (F) 00H [Write Only]

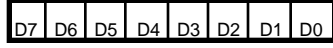
P4D (FH) 02H



Data

Figure 57. Port 4 Data Register (F) 02H [Write Only]

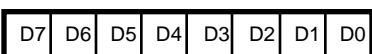
P4M (FH) 03H



- P40-P47 I/O Definition
- 0 Defines Bit as Output
- 1 Defines Bit as Input
- Returns "FF" Upon Read

Figure 58. Port 4 Mode Register (F) 03H [Write Only]

P5D (FH) 04H



Data

Figure 59. Port 5 Data Register (PCON) (F) 04H [Read/Write]

P5M (FH) 05H

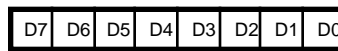


- P50-P57 I/O Definition
- 0 Defines Bit as Output
- 1 Defines Bit as Input*
- Returns "FF" Upon Read

* Default setting after Reset

Figure 60. Port 5 Mode Register (PCON) (F) 05H [Write Only]

P45CON (FH) 06H



- Port 4 Configuration Bit
- 0 Open Drain *
- 1 Push-pull Active
- Reserved
- Port 5 Configuration Bit
- 0 Open Drain *
- 1 Push-pull Active
- Reserved

* Default setting after Reset

Figure 61. Port 4 and 5 Configuration Register (F) 06H [Write Only]

SMR (FH) 0BH



- W 00 SCLK/TCLK Not Divide by 16†
- 01 SCLK/TCLK Not Divide by 16
- 10 SCLK/TCLK Divide by 16
- 11 SCLK/TCLK Divide by 16
- R Always "1"
- W 000 POR only*
- 001 No effect
- 010 P31
- 011 P32
- 100 P33
- 101 P27
- 110 P2 NOR 0-3
- 111 P2 NOR 0-7
- R Always "1"
- W 0 Stop delay on*
- 1 Stop delay off
- R Always "1"
- W 0 Low Stop Recovery Level*
- 1 High Stop Recovery Level
- R Always "1"
- W No effect
- R 0 POR*
- 1 Stop-Mode Recovery

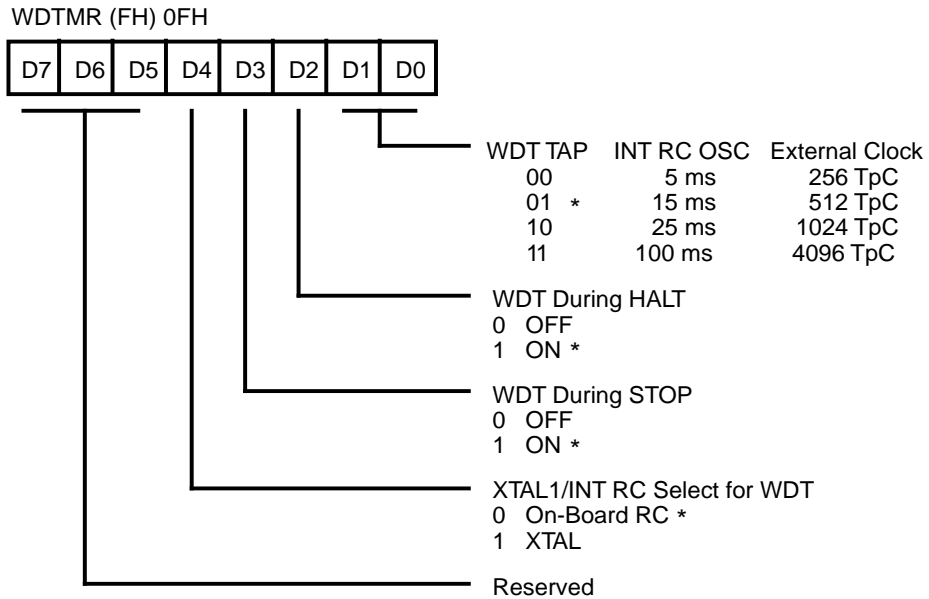
* Default Setting After Reset

† Reset After Stop-Mode Recovery

Figure 62. Stop-Mode Recovery Register (F) 07H [Read/Write]

**Table 18. DSP Control Register
(F) 0FH [Read/Write]**

Field DSPCON (F)0CH	Position	Attrib	Value	Label
Z8_SCLK	76-----	R/W	00	2.5 MHz (OSC/8)
			0.1	5 MHz (OSC/4)
			1x	10 MHz (OSC/2)
DSP_Reset	--5-----	R W		Return "0"
			0	No effect
			1	Reset DSP
DSP_Run	---4----	R/W	0	Halt_DSP
			1	Run_DSP
Reserved	----32--		xx	Return "0"
				No effect
IntFeedback	-----1-	R W		FB_DSP_INT2
			1	Set DSP_INT2
			0	No effect
	-----0	R W		FB_Z8_IRQ3
			1	Clear IRQ 3
			0	No effect



* Default setting after RESET

Note: The WDTMR Register is only accessed within 64 Z8® clock cycles after POR.

**Figure 63. Watch-Dog Timer Mode Register
(F) 0FH [Read/Write]**

Z8 CONTROL REGISTERS

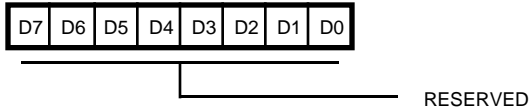


Figure 64. Reserved (F0H)

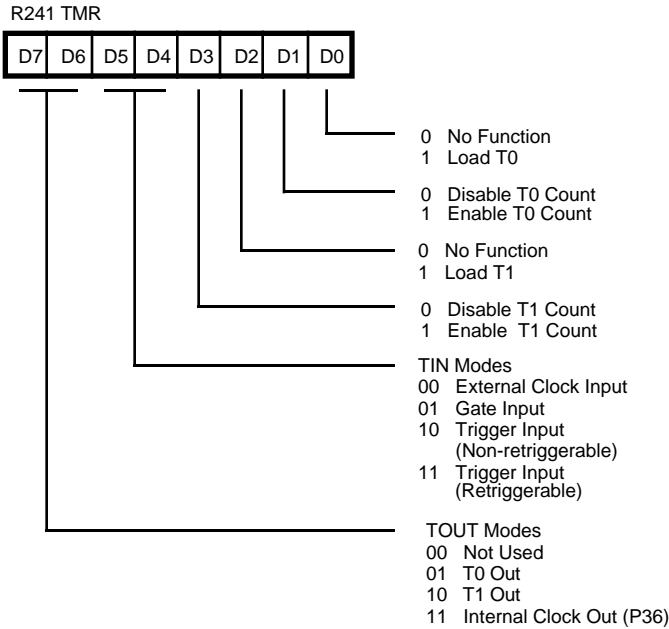


Figure 65. Timer Mode Register (F1H: Read/Write)

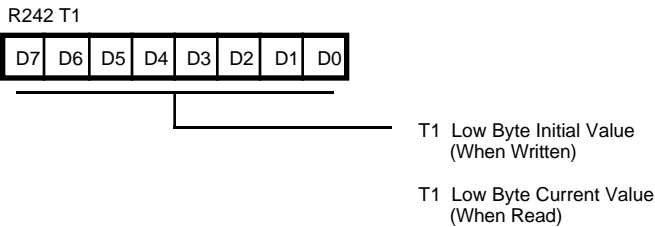


Figure 66. Counter/Timer 1 Register (F2H: Read/Write)

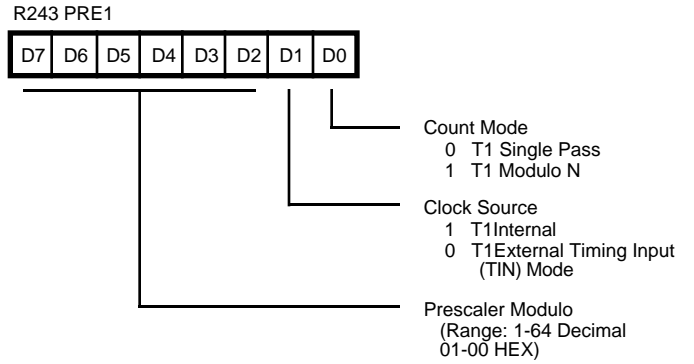


Figure 67. Prescaler 1 Register (F3H: Write Only)

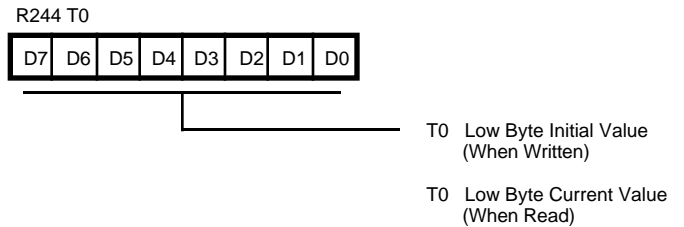


Figure 68. Counter/Timer 0 Register (F4H: Read/Write)

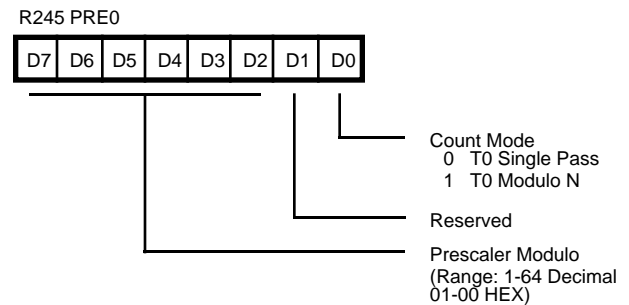


Figure 69. Prescaler 0 Register (F5H: Write Only)

Z8 CONTROL REGISTERS (Continued)

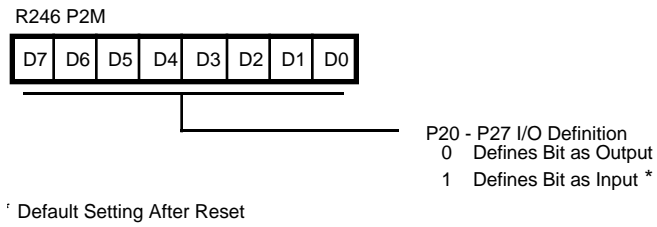


Figure 70. Port 2 Mode Register (F6H: Write Only)

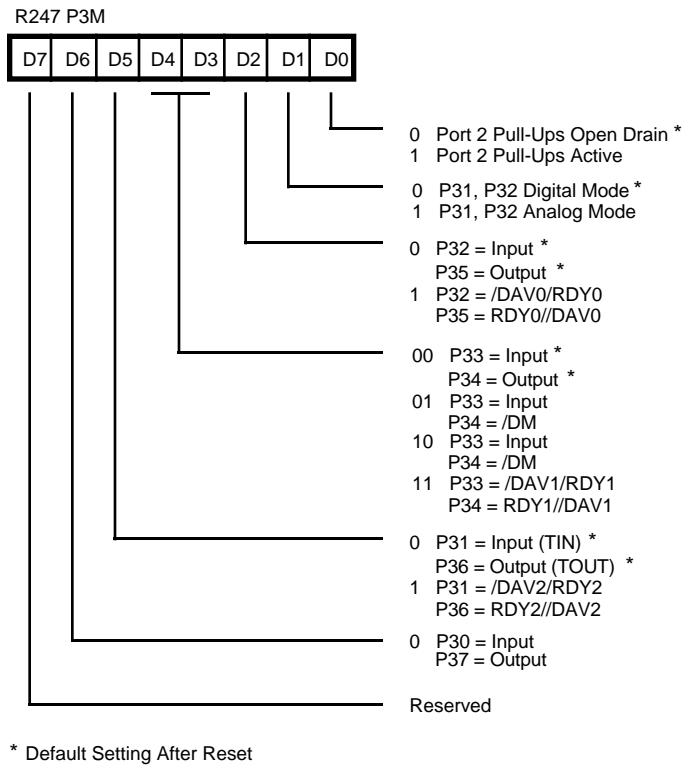


Figure 71. Port 3 Mode Register (F7H: Write Only)

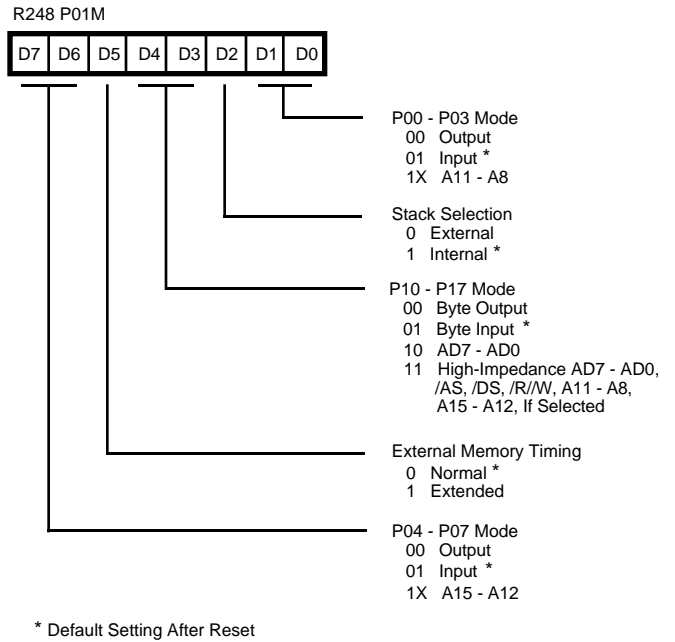


Figure 72. Port 0 Mode Register (F8H: Write Only)

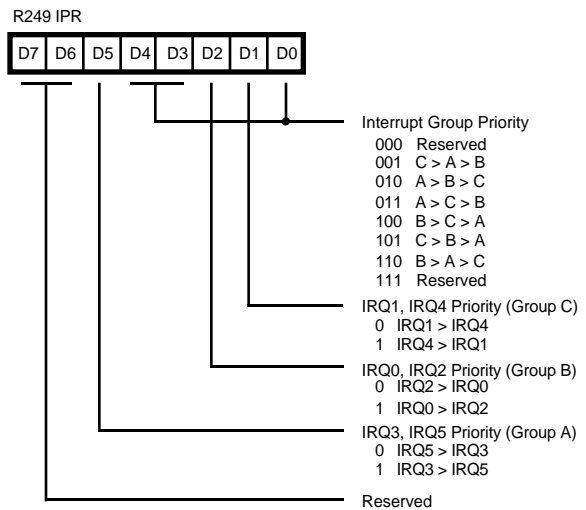


Figure 73. Interrupt Priority Register (F9H: Write Only)

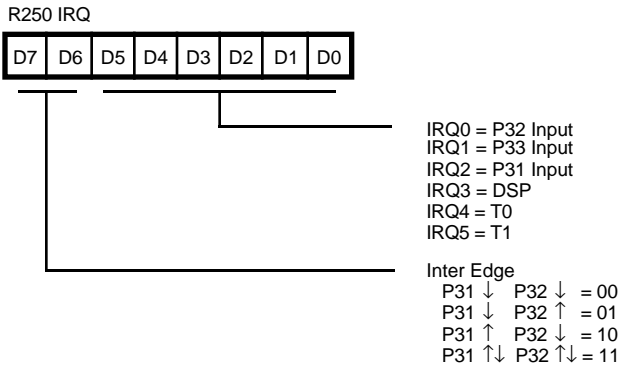


Figure 74. Interrupt Request Register

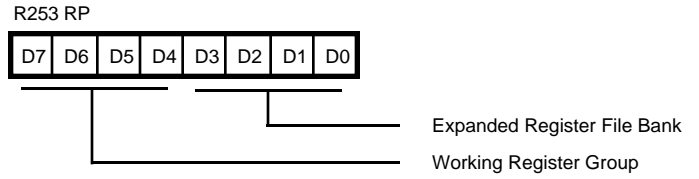


Figure 77. Register Pointer (FDH: Read/Write)

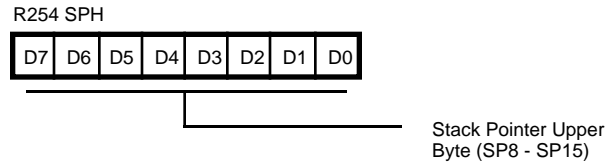


Figure 78. Stack Pointer High (FEH: Read/Write)

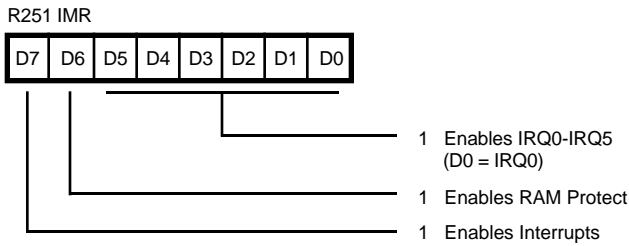


Figure 75. Interrupt Mask Register (FBH: Read/Write)

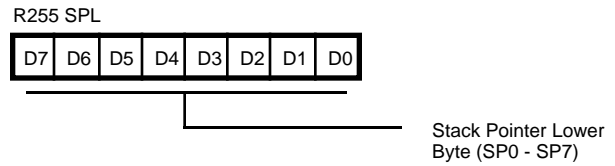


Figure 79. Stack Pointer Low (FFH: Read/Write)

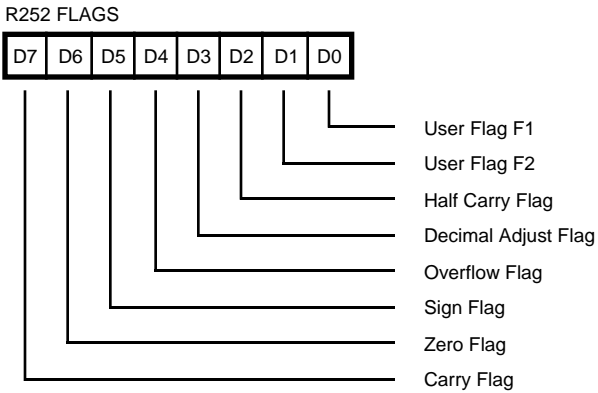


Figure 76. Flag Register (FCH: Read/Write)

PACKAGE INFORMATION

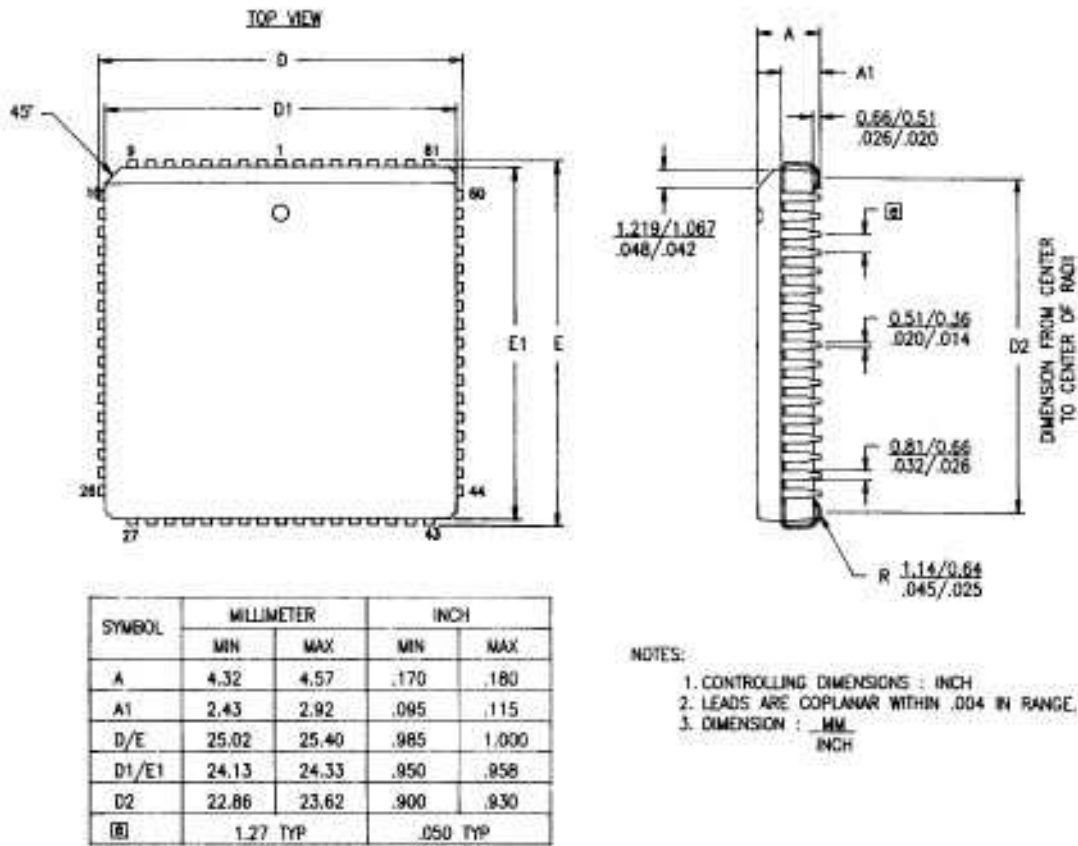


Figure 80. 68-Pin PLCC Package Diagram

ORDERING INFORMATION

Z89135	Z89136
20 MHz	20 MHz
68-Pin PLCC	68-Pin PLCC
Z8913520VSC	Z8913620VSC

Speed

20 = 20.48 MHz

Package

V = Plastic Leaded Chip Carrier (PLCC)

Temperature

S = 0°C to +55°C

Environmental

C = Plastic Standard

Example:

Z 89135 20 V S C is a Z89135, 20.48 MHz, PLCC, 0°C to +55°C, Plastic Standard Flow

