◆Structure : Silicon Monolithic integrated circuit
◆Product name : Voice Synthesis LSI
◆Type : BU6939FV

◆Features

1) Single playback mode, Available bit-rate is 16kbps(High compression) - 128kbps(High Quarity) at 32kHz sampling or 16kHz sampling).
2) Voice/audio data is stored in serial Flash ROM which is connected to BU6939FV through SPI-serial Interface. Duration for playback is 32seconds/Mbits(standard) or max 64s/Mbits(Maximum).
3) Input system clock: 16.384MHz/8.192MHz/4.096MHz/2.048MHz.
4) Audio sampling rate is 32kHz or 16kHz and Built-in 16bits DAC
5) Operation by single power supply. Available voltage:2.7 to 3.6V.
6) Max numbers of tunes : 512
7) Maximum 10 phrase numbers memory as a ROM-phrase Number,and playback them only one command.(ROM_phrase number is available 0-46)
8) HOST-I/F is selectable from serial interface with status or direct-pin mode.
9) Enable to access(read/write) data stored in serial Flash ROM connected directly to BU6939FV.
10) Various play modes are available.

【play modes from serial Interface】

-available ROM-phrase function.
-adjustable volume at each track independently
-enable to playback tunes which are registered in the sequencer list. Order of tunes are randomly selected. Max 16 tunes can be registered.
-For each track, enable to playback a selected tune or to playback tunes in the sequencer list with/without loop.
-fade-in and fade-out functions are supported.

【Play modes from direct pin control】

-available ROM-phrase function.
-maximum 23 tunes are registered to play.

★Radiation resistance design is not arranged.

◆Absolute maximum ratings (Ta = 25 ˚C)

Item	Symbol	Ratings	Unit
Power dissipation*)	Pd	640	mW
Applied voltage	V_{DD}	-0.2～7.0	V
Input voltage	V_{IN}	-0.2～VDD+0.3	V
Operating temperature range	T_{OPR}	-40～+85	℃
Storage temperature range	TSTG	-50～125	℃

*) Over Ta = 25℃ or more, reducing 6.4mW per ℃.

★Radiation resistance design is not arranged.

◆Operation Conditions

(Ta= -40～+85℃ unless otherwise specified)

Item	Symbol	Specified value			Unit	Condition
		Min	Typ	Max		
Operation power-supply voltage	VDD_IN	2.7	—	3.6	V	—

◆Electric characteristic (DC characteristic)

DC Characteristics

■VDD_IN=3V（Ta=25℃）

Item	Symbol	Specified value			Unit	Condition	Circuit form
		Min	Typ	Max			
"H" Input Voltage	V_{IH}	0.7VDD	—	—	V		2
"L" Input Voltage	V_{IL}	—	—	0.3VDD	V		2
"H" Output Voltage	V_{OH}	VDD-0.4	—	—	V	IO=2.0mA	2
"L" Output Voltage	V_{OL}	—	—	0.4	V	IO=2.0mA	2
"H" Input current	I_{IH}	—	—	10	μA	VIH=VDD	1
"L" Input current	I_{IL}	—	—	-10	μA	VIL=GND	1
Static consumption current	I_{ST}	—	—	10	μA	V_i=V_{DD}orGND	3

DAC characteristics

■VDD_IN=3V (Ta=25℃)

Item	Symbol	Specified Value			Unit	Condition
		Min.	Typ.	max.		
DACOUToutput load registance	R_{AOUT}	10	—	—	KΩ	at No signal
DACOUT Output Voltage	V_{AOUT}	GND	—	VDD	V	at No load

◆External dimensions・Block diagram

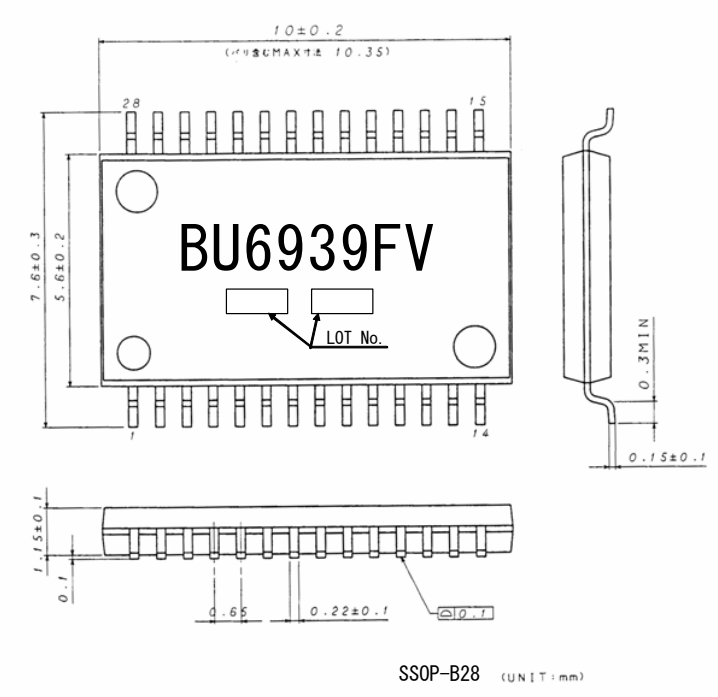


Figure1　External dimention

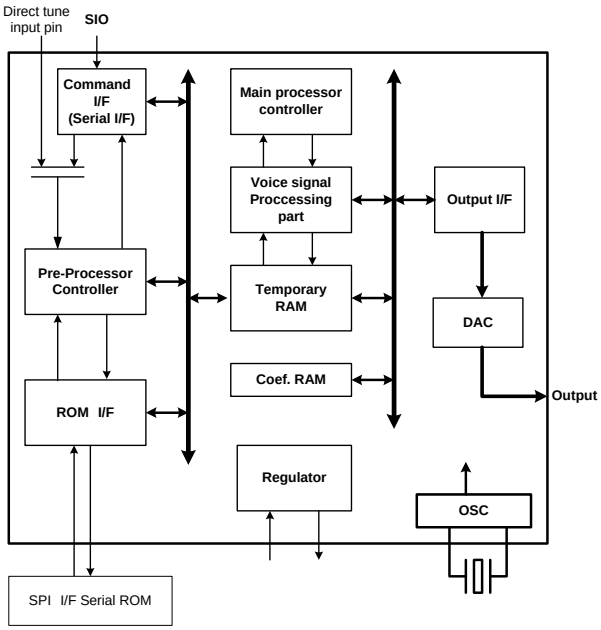


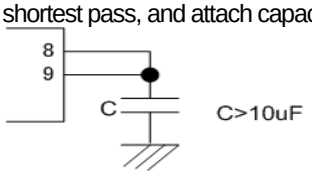
Figure 2.　Block diagram

◆Pin name

Table Pin name Detailed table

PIN NO.	Pin Name	I/O	Function
1	GND	—	GND
2	VSEL2/TXD	IO	tune number pin#2 / Serial Interface output data
3	VSEL1/RXD	I	tune number pin#1 / Serial Interface input data
4	VSEL0/RXCB	I	tune number pin#0 / Serial Interface CLK
5	TSEVENT/BUSY	O	Playing / ending flag("H":playing "L":stop) accessing Flash ROM ("H" : busy "L" : not busy)
6	VSEL3/SYNCREQ	IO	tune number pin#3 / Synchronous character request ("H" synchronization error)
7	GND	—	GND
8	VDD1.8_IN	I	Core power supply input※3)
9	REG18	O	Core power supply output※3)
10	STBY	I	Standby ("H" oscillation stop) normally “L”
11	TESTEN	I	Test Input(“L” fixation)
12	VDD_IN	—	Power supply input
13	SPISCK	O	Clock for serial SPI-ROM
14	SPISO	O	Serial output data to serial SPI-ROM
15	SPISI	I	Serial Input data from serial SPI-ROM
16	SPICEB	O	chip enable for serial SPI-ROM
17	GND	—	GND
18	VSEL4/BFULLB	IO	tune number pin#4 /command buffer Full signal
19	APOFF	I	Analog Circuit Power off
20	CLK16SEL	I	Clock selection “H”:16.384Mhz mode “L”:4.096MHzmode
21	REFOUT	O	LSI TEST Pin (attach capacitance(>10uF))
22	DACOUT	O	DAC Output
23	GND	—	GND
24	VDD_IN	—	Power supply input
25	RESETB	I	Reset pin (low active)
26	SIO_ENBL	I	Selection of host interface(SIO or direction pin input*1))
27	XIN	I	Oscillation cell input *2
28	XOUT	O	Oscillation cell Output *2

*1) At SIO_ENBL ="L", VSEL4, VSEL3, VSEL2, VSEL1, VSEL0 is valid, and SIO is invalid.
*2) At no setting CLK setting Register, Clock is 16.384MHz at CLK16SEL="H",,4.096MHz at CLK16SEL ="L".
*3) pin #8 and pin #9 should be connected in a shortest pass, and attach capacitance(>10uF) as following figure.



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