CADEKA
Amplify the Human Experience

Comlinear™ CLC1604

Single, Low Power, 110MHz Amplifier with Disable

FEATURES

- 110MHz -3dB bandwidth at G=2
- 0.65mA supply current
- 0.04mA supply current (disabled)
- 230V/µs slew rate
- 5nV/√Hz input voltage noise
- 80mA output current
- Fully specified at 5V and ±5V supplies
- CLC1604: Lead-free SOT23-6, SOIC-8

APPLICATIONS

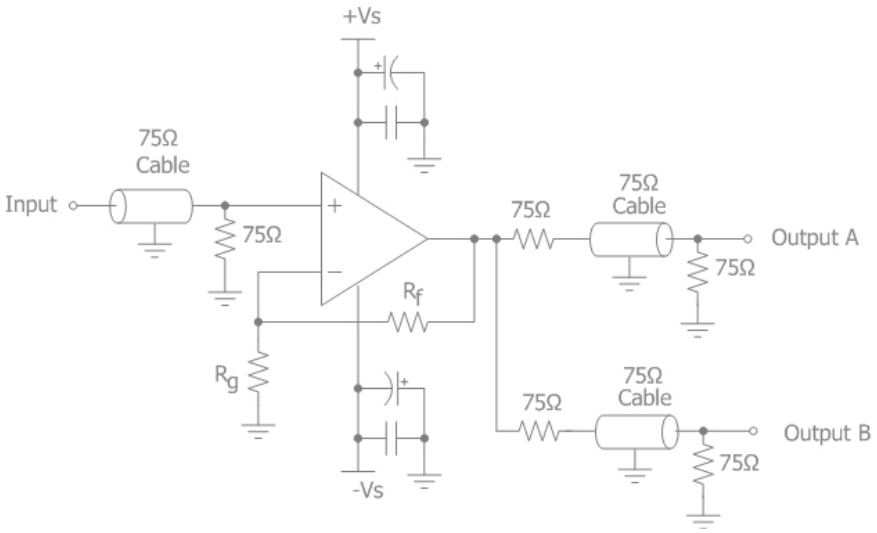
- Video line drivers
- Imaging applications
- Portable video applications
- Differential line receivers
- Photodiode preamps
- Radar or communication receivers
- Battery-powered equipment
- Current-to-voltage converters

General Description

The *Comlinear* CLC1604 is a high-performance, current feedback amplifier that offers 110MHz bandwidth and 230V/µs slew rate while consuming only 0.65mA of supply current. The *Comlinear* CLC1604 high-performance amplifier also features a power saving disable option, dropping the supply current to 0.04mA.

The *Comlinear* CLC1604 is designed to operate from ±5V or +5V supplies. It provides 80mA of output current, making it well suited for video line driving or cable driving applications. The CLC1604 is available in a space saving SOT23 and SOIC packages.

Typical Application - Driving Dual Video Loads

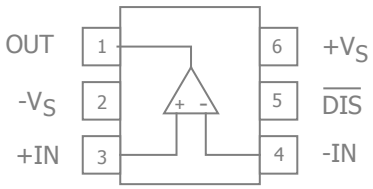


Ordering Information

Part Number	Package	Pb-Free	Operating Temperature Range	Packaging Method
CLC1604IST6X	SOT23-6	Yes	-40°C to +85°C	Reel
CLC1604ISO8X*	SOIC-8	Yes	-40°C to +85°C	Reel
CLC1604ISO8*	SOIC-8	Yes	-40°C to +85°C	Rail

*Preliminary Product Information
Moisture sensitivity level for all parts is MSL-1.

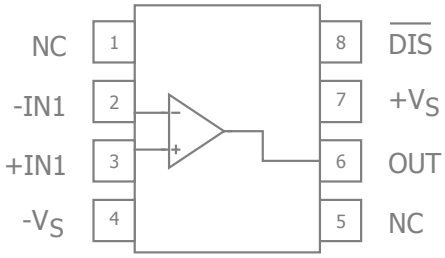
SOT23 Pin Configuration



SOT23 Pin Assignments

Pin No.	Pin Name	Description
1	OUT	Output
2	$-V_S$	Negative supply
3	+IN	Positive input
4	-IN	Negative input
5	$\overline{DIS}$	Disable. Enabled if pin is left floating or pulled above V_{ON}, disabled if pin is grounded or pulled below V_{OFF}.
6	$+V_S$	Positive supply

SOIC Pin Configuration



SOIC Pin Assignments

Pin No.	Pin Name	Description
1	NC	No connect
2	-IN1	Negative input, channel 1
3	+IN1	Positive input, channel 1
4	$-V_S$	Negative supply
5	NC	No connect
6	OUT	Output
7	$+V_S$	Positive supply
8	$\overline{DIS}$	Disable. Enabled if pin is left floating or pulled above V_{ON}, disabled if pin is grounded or pulled below V_{OFF}.

Disable Pin Truth Table

Pin	High* (> (V_S - 1.5V))	Low (< (V_S - 3.5V))
$\overline{DIS}$	Enabled	Disabled

*Default Open State

Absolute Maximum Ratings

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table defines the conditions for actual device operation.

Parameter	Min	Max	Unit
Supply Voltage	0	14	V
Input Voltage Range	$-V_S$ -0.5V	$+V_S$ +0.5V	V

Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			150	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			300	°C
Package Thermal Resistance				
6-Lead SOT23		177		°C/W
8-Lead SOIC		100		°C/W

Notes:
Package thermal resistance (θ_{JA}), JDEC standard, multi-layer test boards, still air.

ESD Protection

Product	SOT23-6	SOIC-8
Human Body Model (HBM)	2kV	2kV
Charged Device Model (CDM)	1kV	1kV

Notes:
0.8kV between the input pairs +IN and -IN pins only. All other pins are 2kV.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+85	°C
Supply Voltage Range	4.5		12	V

Electrical Characteristics at +5V

T_A = 25°C, V_S = +5V, R_f = 1.2kΩ, R_L = 100Ω to V_S/2, G = 2; $\overline{DIS}$ pin open (enabled) unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
UGBW	-3dB Bandwidth	G = +1, V_{OUT} = 0.2V_{pp}		TBD		MHz
BW_{SS}	-3dB Bandwidth	G = +2, V_{OUT} = 0.2V_{pp}		110		MHz
BW_{LS}	Large Signal Bandwidth	G = +2, V_{OUT} = 1V_{pp}		70		MHz
$BW_{0.1dBSS}$	0.1dB Gain Flatness	G = +2, V_{OUT} = 0.2V_{pp}		10		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 1V step; (10% to 90%)		8		ns
t_S	Settling Time to 0.1%	V_{OUT} = 1V step		25		ns
OS	Overshoot	V_{OUT} = 0.2V step		TBD		%
SR	Slew Rate	2V step		180		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	1V_{pp}, 5MHz		-57		dBc
HD3	3rd Harmonic Distortion	1V_{pp}, 5MHz		-53		dBc
THD	Total Harmonic Distortion	1V_{pp}, 5MHz		-49		dB
IP3	Third-Order Intercept	0.5V_{pp}, 10MHz		35		dBm
SFDR	Spurious-Free Dynamic Range	1V_{pp}, 5MHz		55		dBc
D_G	Differential Gain	NTSC (3.58MHz), DC-coupled, R_L = 150Ω		0.08		%
D_P	Differential Phase	NTSC (3.58MHz), DC-coupled, R_L = 150Ω		0.2		°
e_n	Input Voltage Noise	> 1MHz		5		nV/√Hz
i_{ni}	Input Voltage Noise - Inverting	> 1MHz, Inverting		25		pA/√Hz
		> 1MHz, Non-inverting		25		pA/√Hz
DC Performance						
V_{IO}	Input Offset Voltage			0		mV
dV_{IO}	Average Drift			6.0		µV/°C
I_{bn}	Input Bias Current - Non-Inverting			±3.0		µA
dI_{bn}	Average Drift			40		nA/°C
I_{bi}	Input Bias Current - Inverting			±0.4		µA
dI_{bi}	Average Drift			10		nA/°C
PSRR	Power Supply Rejection Ratio	DC		60		dB
A_{OL}	Open-Loop Transresistance			TBD		mΩ
I_S	Supply Current			0.55		mA
Disable Characteristics						
t_{ON}	Turn On Time			TBD		ns
t_{OFF}	Turn Off Time			TBD		ns
OFF_{ISO}	Off Isolation			TBD		dB
$OFFC_{OUT}$	Off Output Capacitance			TBD		pF
$OFFR_{OUT}$	Off Output Resistance			TBD		Ω
V_{OFF}	Power Down Input Voltage	$\overline{DIS}$ pin, disabled if pin is grounded or pulled below V_{OFF} = V_s - 3.5V	Disabled if < (V_s - 3.5V)			V
V_{ON}	Enable Input Voltage	$\overline{DIS}$ pin, enabled if pin is left open or pulled above V_{ON} = V_s - 1.5V	Enabled if > (V_s - 1.5V)			V
I_{SD}	Disable Supply Current	No Load, $\overline{DIS}$ pin tied to ground		0.04		mA
Input Characteristics						
R_{IN}	Input Resistance	Non-inverting		4		MΩ
		Inverting		350		Ω
C_{IN}	Input Capacitance			1.0		pF
CMIR	Common Mode Input Range			±1.5		V
CMRR	Common Mode Rejection Ratio	DC		55		dB

Electrical Characteristics at +5V

T_A = 25°C, V_s = +5V, R_f = 1.2kΩ, R_L = 100Ω to V_S/2, G = 2; $\overline{DIS}$ pin open (enabled) unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Output Characteristics						
R_O	Output Resistance	Closed Loop, DC		0.02		Ω
V_{OUT}	Output Voltage Swing	R_L = 150Ω		±1.4		V
		R_L = 1kΩ		TBD		V
I_{OUT}	Output Current			±80		mA
I_{SC}	Short-Circuit Output Current	$V_{OUT} = V_S / 2$		TBD		mA

Notes:

1.

Electrical Characteristics at ±5V

T_A = 25°C, V_S = ±5V, R_f = 1.2kΩ, R_L = 100Ω to GND, G = 2; $\overline{DIS}$ pin open (enabled) unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
UGBW	-3dB Bandwidth	G = +1, V_{OUT} = 0.2V_{pp}		TBD		MHz
BW_{SS}	-3dB Bandwidth	G = +2, V_{OUT} = 0.2V_{pp}		110		MHz
BW_{LS}	Large Signal Bandwidth	G = +2, V_{OUT} = 2V_{pp}		90		MHz
$BW_{0.1dBSS}$	0.1dB Gain Flatness	G = +2, V_{OUT} = 0.2V_{pp}		15		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 2V step; (10% to 90%)		9		ns
t_S	Settling Time to 0.1%	V_{OUT} = 2V step		35		ns
OS	Overshoot	V_{OUT} = 0.2V step		TBD		%
SR	Slew Rate	2V step		230		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	2V_{pp}, 5MHz		-57		dBc
HD3	3rd Harmonic Distortion	2V_{pp}, 5MHz		-53		dBc
THD	Total Harmonic Distortion	2V_{pp}, 5MHz		-49		dB
IP3	Third-Order Intercept	2V_{pp}, 10MHz		35		dBm
SFDR	Spurious-Free Dynamic Range	2V_{pp}, 5MHz		55		dBc
D_G	Differential Gain	NTSC (3.58MHz), DC-coupled, R_L = 150Ω		0.08		%
D_P	Differential Phase	NTSC (3.58MHz), DC-coupled, R_L = 150Ω		0.2		°
e_n	Input Voltage Noise	> 1MHz		5		nV/√Hz
i_{ni}	Input Voltage Noise - Inverting	> 1MHz, Inverting		25		pA/√Hz
		> 1MHz, Non-inverting		25		pA/√Hz
DC Performance						
V_{IO}	Input Offset Voltage (1)		-8	0	8	mV
dV_{IO}	Average Drift			6.0		µV/°C
I_{bn}	Input Bias Current - Non-Inverting (1)		-20	±3.0	20	µA
dI_{bn}	Average Drift			40		nA/°C
I_{bi}	Input Bias Current - Inverting (1)		-20	±0.4	20	µA
dI_{bi}	Average Drift			10		nA/°C
PSRR	Power Supply Rejection Ratio (1)	DC	50	60		dB
A_{OL}	Open-Loop Transresistance			TBD		mΩ
I_S	Supply Current (1)			0.65	1.2	mA
Disable Characteristics						
t_{ON}	Turn On Time			900		ns
t_{OFF}	Turn Off Time			400		ns
OFF_{ISO}	Off Isolation			TBD		dB
$OFFC_{OUT}$	Off Output Capacitance			TBD		pF
$OFFR_{OUT}$	Off Output Resistance			TBD		Ω
V_{OFF}	Power Down Input Voltage	$\overline{DIS}$ pin, disabled if pin is grounded or pulled below V_{OFF} = V_s - 3.5V	Disabled if < (V_s - 3.5V)			V
V_{ON}	Enable Input Voltage	$\overline{DIS}$ pin, enabled if pin is left open or pulled above V_{ON} = V_s - 1.5V	Enabled if > (V_s - 1.5V)			V
I_{SD}	Disable Supply Current (1)	No Load, $\overline{DIS}$ pin tied to ground		0.04	0.3	mA
Input Characteristics						
R_{IN}	Input Resistance	Non-inverting		4		MΩ
		Inverting		350		Ω
C_{IN}	Input Capacitance			1.0		pF
CMIR	Common Mode Input Range			±4.0		V
CMRR	Common Mode Rejection Ratio (1)	DC	50	55		dB

Electrical Characteristics at +5V

T_A = 25°C, V_s = +5V, R_f = 1.2kΩ, R_L = 100Ω to V_S/2, G = 2; $\overline{DIS}$ pin open (enabled) unless otherwise noted.

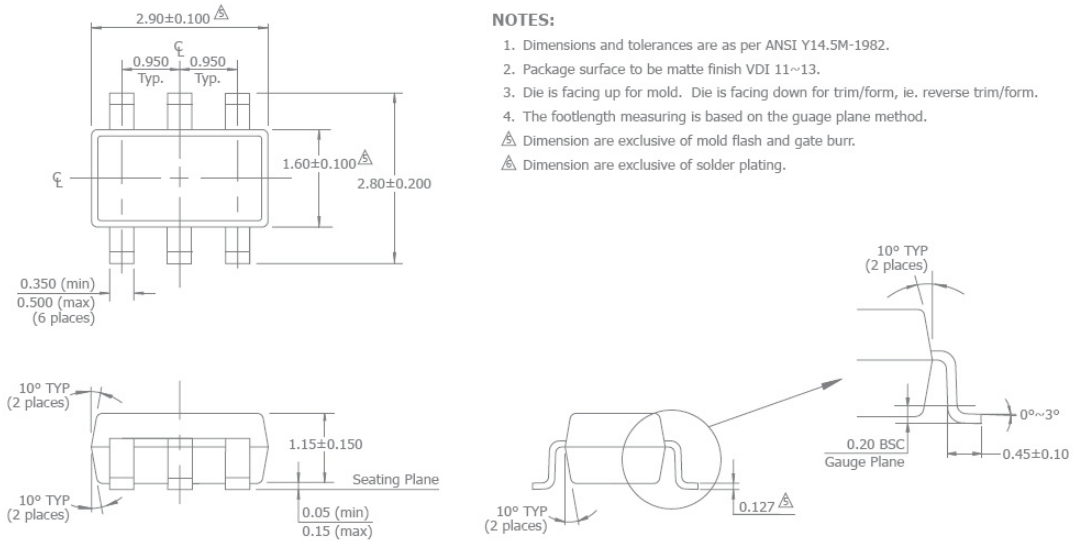
Symbol	Parameter	Conditions	Min	Typ	Max	Units
Output Characteristics						
R_O	Output Resistance	Closed Loop, DC		0.03		Ω
V_{OUT}	Output Voltage Swing	R_L = 150Ω (1)		±3.5		V
		R_L = 1kΩ		TBD		V
I_{OUT}	Output Current			±80		mA
I_{SC}	Short-Circuit Output Current	$V_{OUT} = V_S / 2$		TBD		mA

Notes:

1. 100% tested at 25°C.

Mechanical Dimensions

SOT23-6 Package



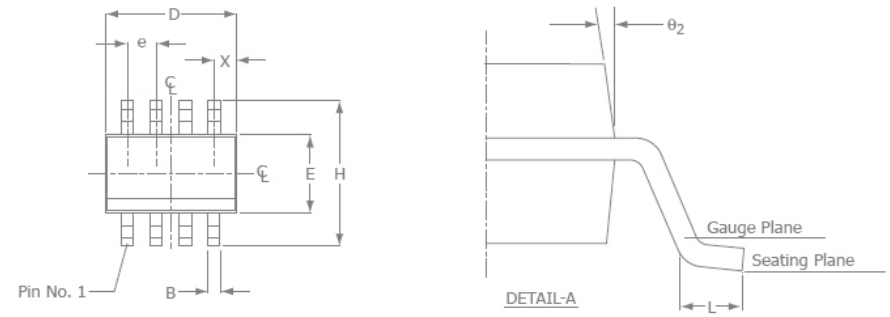
NOTES:

1. Dimensions and tolerances are as per ANSI Y14.5M-1982.
2. Package surface to be matte finish VDI 11~13.
3. Die is facing up for mold. Die is facing down for trim/form, ie. reverse trim/form.
4. The footlength measuring is based on the guage plane method.

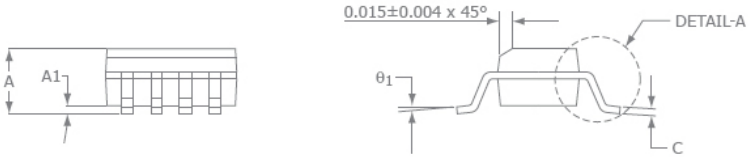
(3) Dimension are exclusive of mold flash and gate burr.

(4) Dimension are exclusive of solder plating.

SOIC-8 Package



SOIC-8		
SYMBOL	MIN	MAX
A	0.054	0.068
A1	0.004	0.0098
B	0.014	0.019
D	0.189	0.196
E	0.150	0.157
H	0.229	0.244
e	0.050 BSC	
C	0.0075	0.0098
L	0.016	0.034
X	0.0215 Ref	
θ_1	0°	8°
θ_2	7° BSC	



NOTE:

1. All dimensions are in inches.
2. Lead coplanarity should be 0" to 0.004" max.
3. Package surface finishing: VDI 24~27
4. All dimension excluding mold flashes.
5. The lead width, B to be determined at 0.0075" from the lead tip.

For additional information regarding our products, please visit CADEKA at: cadeka.com

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