National Semiconductor

July 2001

CLC410
Fast Settling, Video Op Amp with Disable

General Description

The current-feedback CLC410 is a fast settling, wideband, monolithic op amp with fast disable/enable feature. Designed for low gain applications (A_V = ±1 to ±8), the CLC410 consumes only 160mW of power (180mW max) yet provides a -3dB bandwidth of 200MHz (A_V = +2) and 0.05% settling in 12ns (15ns max). Plus, the disable feature provides fast turn on (100ns) and turn off (200ns). In addition, the CLC410 offers both high performance and stability without compensation - even at a gain of +1.

The CLC410 provides a simple, high performance solution for video switching and distribution applications, especially where analog buses benefit from use of the disable function to "multiplex" signals onto the bus. Differential gain/phase of 0.01%/0.01° provide high fidelity and the 60mA output current offers ample drive capability.

The CLC410's fast settling, low distortion, and high drive capabilities make it an ideal ADC driver. The low 160mW quiescent power consumption and very low 40mW disabled power consumption suggest use where power is critical and/or "system off" power consumption must be minimized.

The CLC410 is available in several versions to meet a variety of requirements. A three letter suffix determines the version.

Enhanced Solutions (Military/Aerospace)

SMD Number: 5962-90600

Space level versions also available.

For more information, visit http://www.national.com/mil

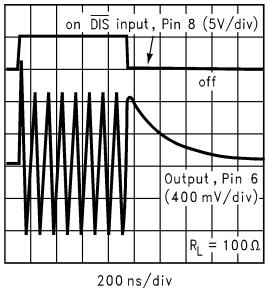
Features

- -3dB bandwidth of 200MHz
- 0.05% settling in 12ns
- Low Power, 160mW (40mW disabled)
- Low distortion, -60dBc at 20MHz
- Fast disable (200ns)
- Differential gain/phase: 0.01%/0.01°
- ±1 to ±8 closed-loop gain range

Applications

- Video switching and distribution
- Analog bus driving (with disable)
- Low power "standby" using Disable
- Fast, precision A/D conversion
- D/A current-to-voltage conversion
- IF processors
- High speed communications

Enable/Disable Response



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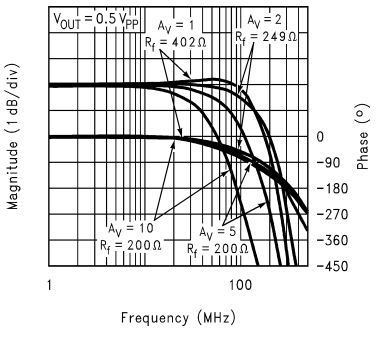
Non-Inverting Frequency Response



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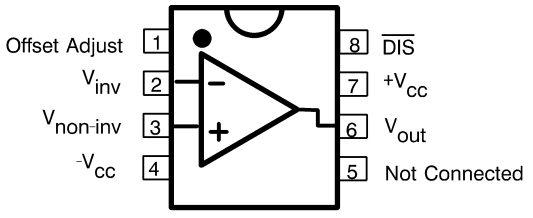
Connection Diagram



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Pinout
DIP & SOIC

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	±7V
I_{OUT} Output is short circuit protected to ground, but maximum reliability will be maintained if I_{OUT} does not exceed...	60mA
Common Mode Input Voltage	$\pm V_{CC}$
Differential Input Voltage	5V
Disable Input Voltage (pin 8)	$\pm V_{CC}$−1V
Applied output voltage when disabled	$\pm V_{CC}$
Junction Temperature	+150˚C
Operating Temperature Range	−40˚C to +85˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Solder Duration (+300˚C)	10 sec
ESD Rating (human body model)	500V

Operating Ratings

Thermal Resistance Package	(θ_{JC})	(θ_{JA})
MDIP	65˚C/W	120˚C/W
SOIC	60˚C/W	140˚C/W

Electrical Characteristics

A_V = +2, V_{CC} = ±5V, R_L = 100Ω, R_f = 250Ω; unless specified

Symbol	Parameter		Conditions	Typ	Max/Min (Note 2)			Units
Ambient Temperature			CLC410AJ	+25˚C	−40˚C	+25˚C	+85˚C	
Frequency Domain Response								
SSBW	-3dB Bandwidth		V_{OUT} <0.5V_{PP}	200	>150	>150	>120	MHz
LSBW			V_{OUT} <5V_{PP}, A_V = +5	50	>35	>35	>35	MHz
	Gain Flatness		V_{OUT}< 0.5V_{PP}					
GFPL	Peaking		DC to 40MHz	0	<0.4	<0.3	<0.4	dB
GFPH	Peaking		>40MHz	0	<0.7	<0.5	<0.7	dB
GFR	Rolloff		DC to 75MHz	0.6	<1	<1	<1.3	dB
LPD	Linear Phase Deviation		DC to 75MHz	0.2	<1	<1	<1.2	deg
Time Domain Response								
TRS	Rise and Fall Time		0.5V Step	1.6	<2.4	<2.4	<2.4	ns
TRL			5V Step	6.5	<10	<10	<10	ns
TSP	Settling Time to	±0.1%	2V Step	10	<13	<13	<13	ns
TS		±0.05%	2V Step	12	<15	<15	<15	ns
OS	Overshoot		0.5V Step	0	<15	<10	<10	%
SR	Slew Rate	A_V = +2		700	>430	>430	>430	V/µs
SR1		A_V = −2		1600	–	–	–	V/µs
Distortion And Noise Response								
HD2	2nd Harmonic Distortion		2V_{PP}, 20MHz	−60	<−40	<−45	<−45	dBc
HD3	3rd harmonic distortion		2V_{PP}, 20MHz	−60	<−50	<−50	<−50	dBc
	Equivalent Input Noise							
SNF	Noise Floor		>1MHz (Note 4)	−157	<−154	<−154	<−153	dBm (1Hz)
INV	Integrated Noise		1MHz to 200MHz (Note 4)	40	<54	<57	<63	µV
DG	Differential Gain (Note 5)		(See Plots)	0.01	0.05	0.04	0.04	%
DP	Differential Phase (Note 5)		(See Plots)	0.01	0.1	0.02	0.02	deg
Disable/Enable Performance								
TOFF	Disable Time to >50dB Attenuation at 10MHz			200	<1000	<1000	<1000	ns
TON	Enable Time			100	<200	<200	<200	ns
	$\overline{DIS}$ Voltage							

Electrical Characteristics (Continued)

A_V = +2, V_{CC} = ±5V, R_L = 100Ω, R_f = 250Ω; unless specified

Symbol	Parameter	Conditions	Typ	Max/Min (Note 2)			Units
VDIS	To Disable		1.0	0.5	0.5	0.5	V
VEN	To Enable		2.6	2.3	3.2	4.0	V
	$\overline{DIS}$ current (sourced from CLC410, see *Figure 5*)						
IDIS	To Disable		200	250	250	250	µA
IEN	To Enable		80	60	60	60	µA
OSD	Off Isolation	At 10MHz	59	>55	>55	>55	dB
Static, DC Performance							
VIO	Input Offset Voltage (Note 3)		2	<±8.2	<±5.0	<±9.0	mV
DVIO	average temperature coefficient		20	<±40	–	<±40	µV/˚C
IBN	Input Bias Current (Note 3)	Non Inverting	10	<±36	<±20	<±20	µA
DIBN	Average Temperature Coefficient		100	<±200	–	<±100	nA/˚C
IBI	Input Bias Current (Note 3)	Inverting	10	<±36	<±20	<±30	µA
DIBI	Average Temperature Coefficient		50	<±200	–	<±100	nA/˚C
PSRR	Power Supply Rejection Ratio		50	>45	>45	>45	dB
CMRR	Common Mode Rejection Ratio		50	>45	>45	>45	dB
ICC	Supply Current (Note 3)	No Load,Quiescent	16	<18	<18	<18	mA
ISD	Supply Current, Disabled	No Load,Quiescent	4	<6	<6	<6	mA
Miscellaneous Performance							
RIN	Non-Inverting Input	Resistance	200	>50	>100	>100	kΩ
CIN		Capacitance	0.5	<2	<2	<2	pF
RO	Output Impedance	At DC	0.1	<0.2	<0.2	<0.2	Ω
ROD	Output Impedance, Disabled	Resistance,at DC	200	<100	<100	<100	kΩ
COD		Capacitance,at DC	0.5	<2	<2	<2	pF
VO	Output Voltage Range	No Load	±3.5	>±3	>±3.2	>±3.2	V
CMIR	Common Mode Input Range	For Rated Performance	±2.1	>±1.2	>±2	>±2	V
IO	Output Current	−40˚C to +85˚C	±70	>±35	>±50	>±50	mA
IO		−55˚C to +125˚C	±60	>±30	>±50	>±50	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Note 3: AJ-level: spec. is 100% tested at +25˚C, sample at 85˚C.

Note 4: Noise tests are performed from 5MHz to 200MHz.

Note 5: Differential gain and phase measured at: A_V = +2, R_f = 250Ω, R_L = 150Ω 1V_{PP} equivalent video signal, 0-100 IRE, 40 IRE_{PP}, 3.58 MHz,) IRE =0 volts, at 75Ω load. See text.

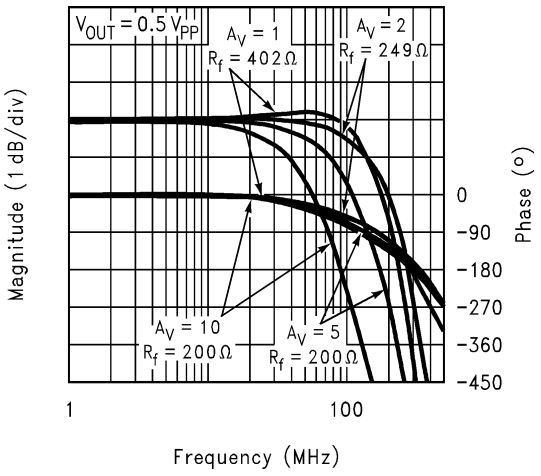
Ordering Information

Package	Temperature Range Industrial	Part Number	Package Marking	NSC Drawing
8-pin plastic DIP	−40˚C to +85˚C	CLC410AJP	CLC410AJP	N08A
8-pin plastic SOIC	−40˚C to +85˚C	CLC410AJE	CLC410AJE	M08A

Typical Performance Characteristics

(T_A = 25°, A_V = +2, V_{CC} = ±5V, R_L = 100Ω; Unless Specified).

Non-Inverting Frequency Response



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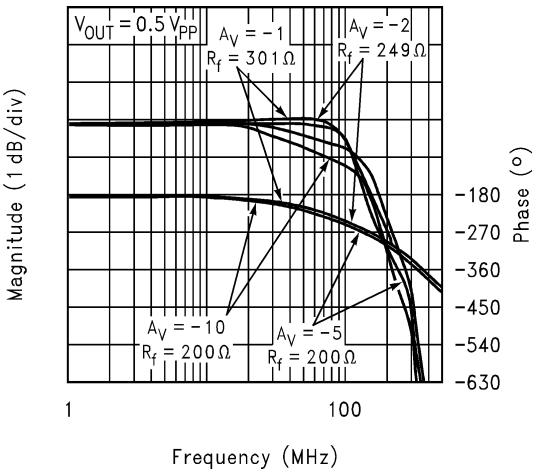
Inverting Frequency Response



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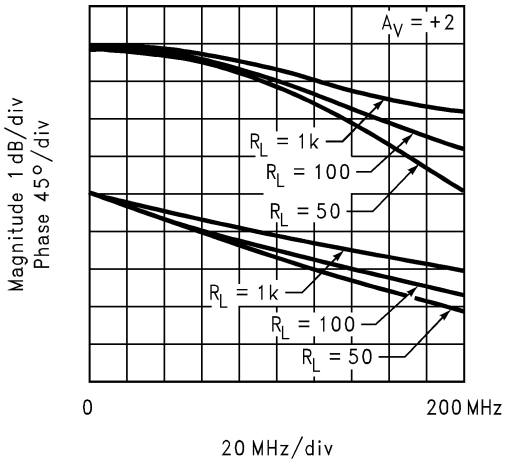
Frequency Response for Various R_LS



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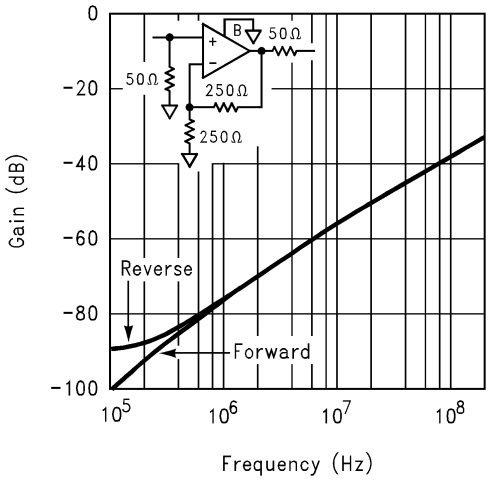
Forward and Reverse Gain During Disable



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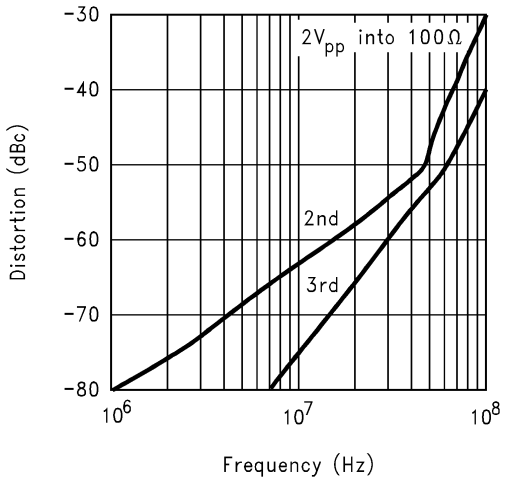
2nd and 3rd Harmonic Distortion



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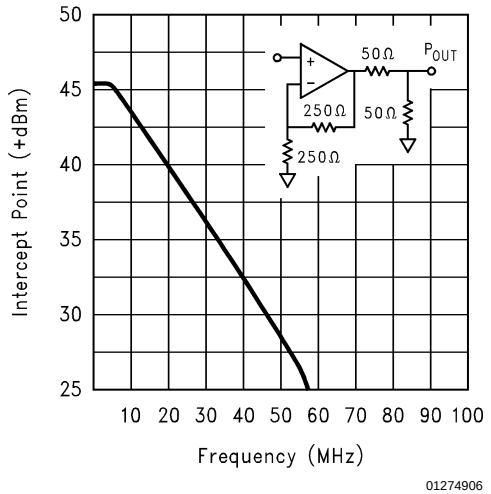
2-Tone, 3rd Order, Intermodulation Intercept



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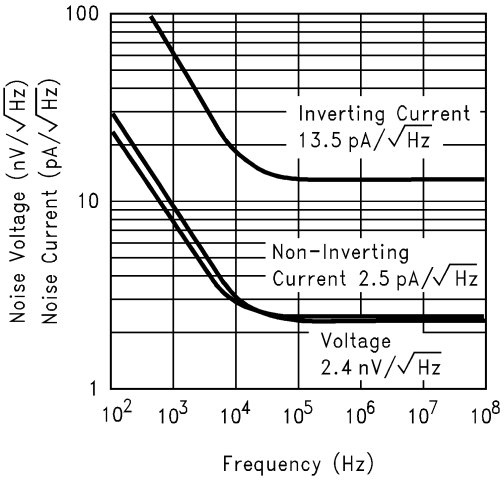
Typical Performance Characteristics (T_A = 25°, A_V = +2, V_{CC} = ±5V, R_L = 100Ω; Unless Specified). (Continued)

Equivalent Input Noise



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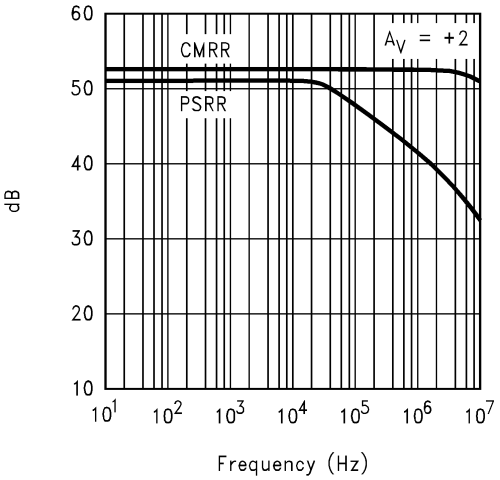
CMRR and PSRR



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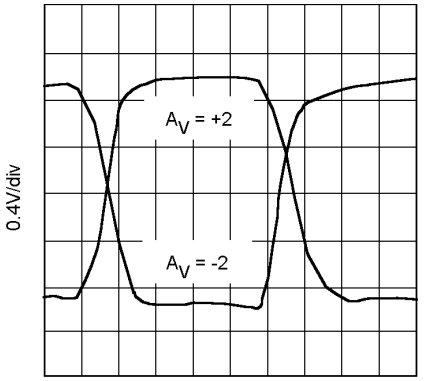
Pulse Response



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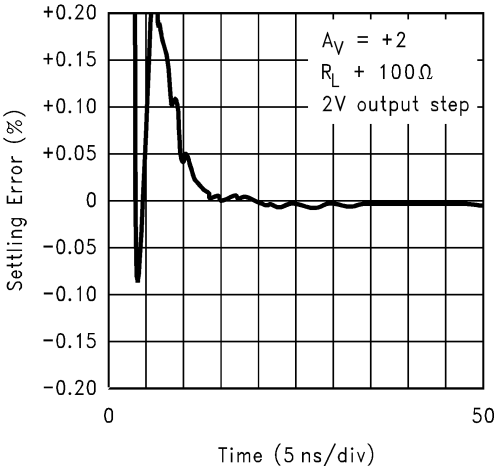
Settling Time



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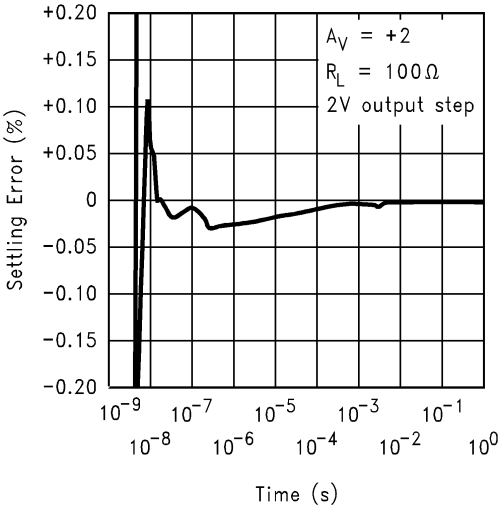
Long-Term Settling Time



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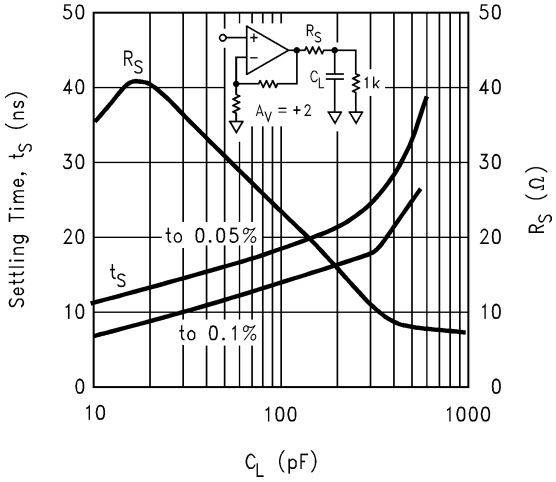
Settling Time vs. Capacitive Load



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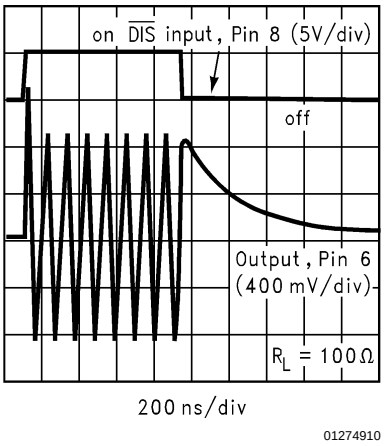
Typical Performance Characteristics (T_A = 25°, A_V = +2, V_{CC} = ±5V, R_L = 100Ω; Unless Specified). (Continued)

Enable/Disable Response



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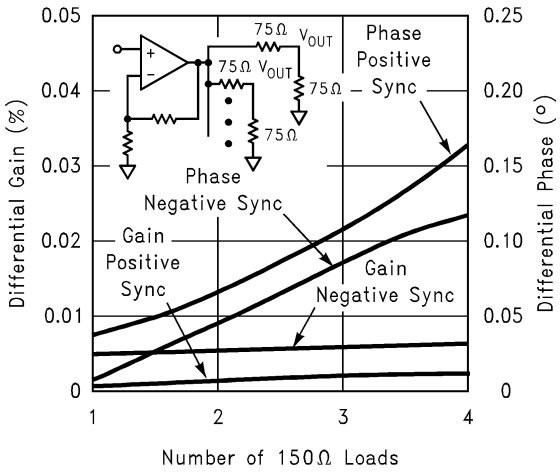
Differential Gain and Phase (3.58MHz)



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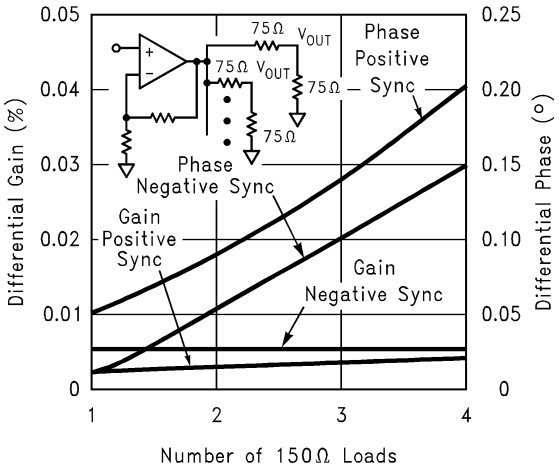
Differential Gain and Phase (4.43MHz)



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Application Division

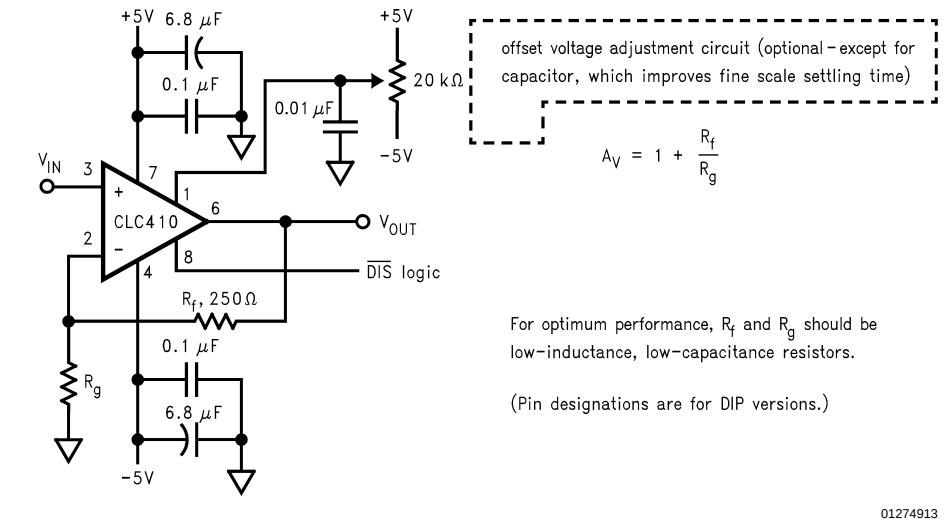


FIGURE 1. Recommended Non-Inverting Gain Circuit

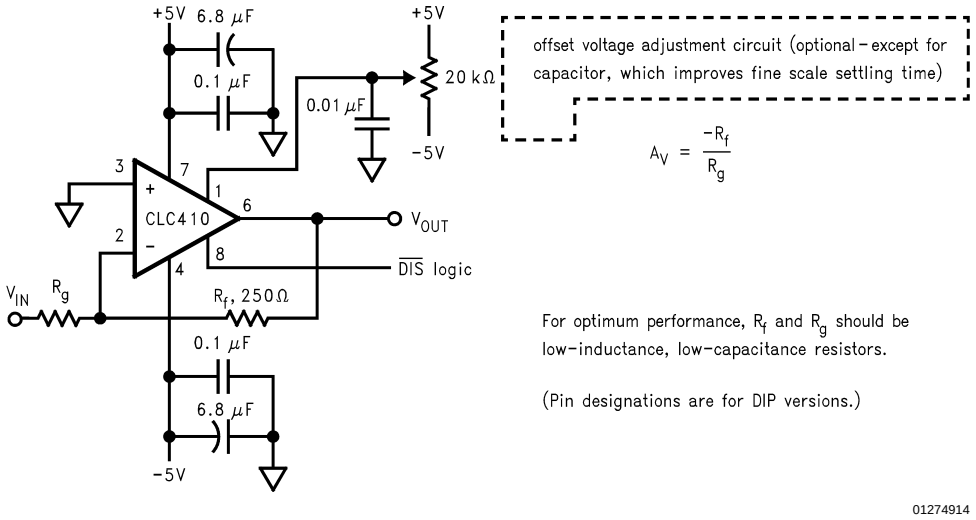


FIGURE 2. Recommended Inverting Gain Circuit

Application Division (Continued)

Enable/Disable Operation

The CLC410 has an enable/disable feature that is useful for conserving power and for multiplexing the outputs of several amplifiers onto an analog bus (*Figure 3*). Disabling an amplifier while not in use reduces power supply current and the output and inverting input pins become a high impedance.

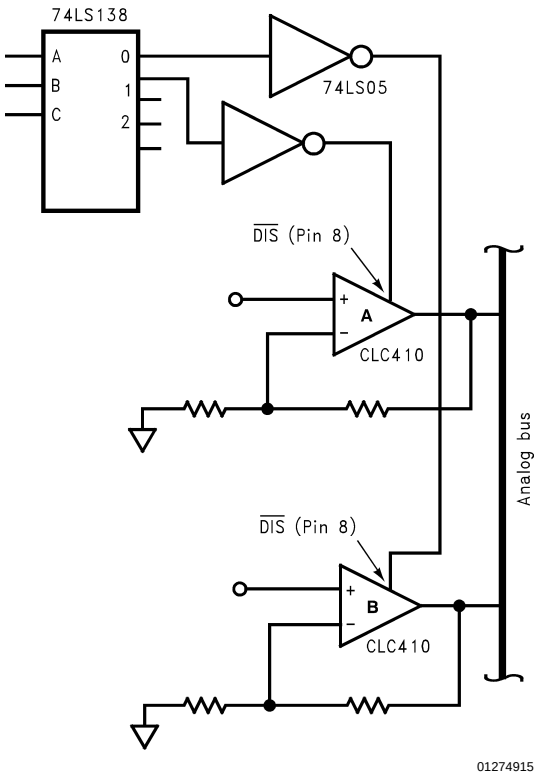


FIGURE 3.

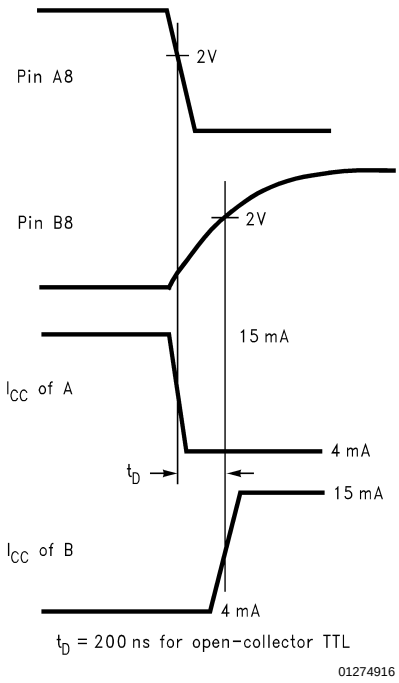


FIGURE 4.

Pin 8, the $\overline{DIS}$ pin, can be driven from either open-collector TTL or from 5V CMOS. A logic low disables the amplifier and an internal 15kΩ pull-up resistor ensures that the amplifier is enabled if pin 8 is not connected (*Figure 5*). Both TTL and 5V CMOS logic are guaranteed to drive a high enough high-level output voltage (V_{OH}) to ensure that the CLC410 is enabled. Whichever type used, “break-before-make” operation should be established when outputs of several amplifiers are connected together. This is important for avoiding large, transient currents flowing between amplifiers when two or more are simultaneously enabled. Typically, proper operation is ensured if all the amplifiers are driven from the same decoder integrated circuit because logic output rise times tend to be longer than fall times. As a result, the amplifier being disabled will reach the 2V threshold sooner than the amplifier being enabled (see t_D of *Figure 4* timing diagram).

Application Division (Continued)

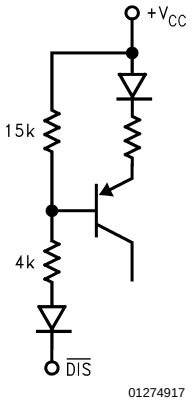


FIGURE 5. Equivalent of $\overline{DIS}$ input

During disable, supply current drops to approximately 4mA and the inverting input and output pin impedances become 200kΩ‖0.5pF each. The total impedance that a disabled amplifier and its associated feedback network presents to the analog bus is determined from *Figure 6*. For example, at a non-inverting gain of 1, the output impedance at video frequencies is 100kΩ‖1pF since the 250Ω feedback resistor is a negligible impedance. Similarly, output impedance is 500Ω‖0.5pF at a non-inverting gain of 2 (with $R_f = R_g$ = 250Ω).

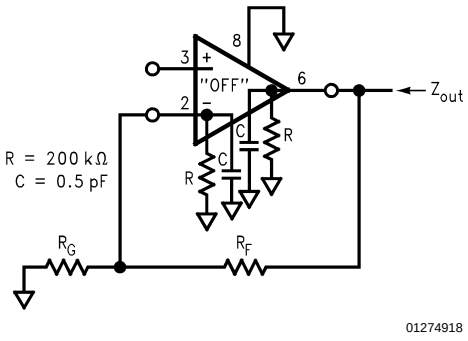


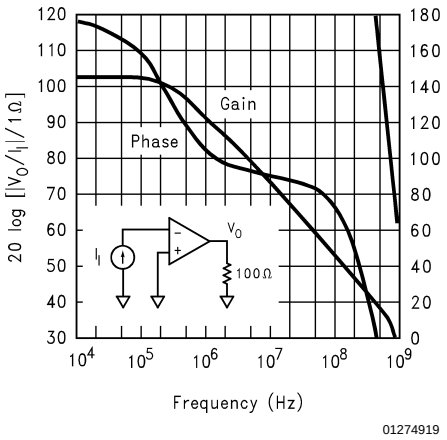
FIGURE 6.

Differential Gain and Phase

Plots on the preceding page illustrate the differential gain and phase performance of the CLC410 at both 3.58MHz and 4.43MHz. Application Note OA-08 presents a measurement technique for measuring the very low differential gain and phase of the CLC410. Observe that the gain and phase errors remain low even as the output loading increases, making the device attractive for driving multiple video outputs.

Understanding the Loop Gain

The CLC410 is a current-feedback op amp. Referring to the equivalent circuit of *Figure 7*, any current flowing in the inverting input is amplified to a voltage at the output through the transimpedance gain shown below. This Z(s) is analogous to the open-loop gain of a voltage feedback amplifier.



Open-Loop Transimpedance Gain, Z(s)

Developing the non-inverting frequency response for the topology of *Figure 3* yields:

$$\frac{V_O}{V_i} = \frac{1 + R_f / R_g}{1 - 1 / LG} \quad (1)$$

where LG is the loop gain defined by,

$$LG = \frac{Z(s)}{R_f} \times \frac{1}{1 + Z_i / (R_f \| R_g)} \quad (2)$$

Equation 1 has a form identical to that for a voltage feedback amplifier with the differences occurring in the LG expression, eq.2. For an idealized treatment, set Z_i = 0 which results in a very simple LG=Z(s)/R_f (Derivation of the transfer function for the case where Z_i = 0 is given in Application Note AN300-1). Using the Z(s) (open-loop transimpedance gain) plot shown on the previous page and dividing by the recommended R_f = 250Ω, yields a large loop gain at DC. As a result, Equation 1 shows that the closed-loop gain at DC is very close to (1+R_f/R_g).

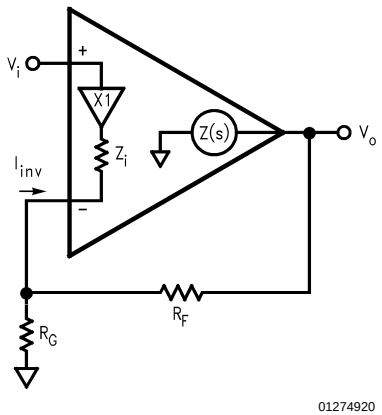


FIGURE 7. Current Feedback Topology

At higher frequencies, the roll-off of Z(s) determines the closed-loop frequency response which, ideally, is dependent only on R_f. **The specifications reported on the previous pages are therefore valid only for the specified R_f = 250Ω.** Increasing R_f from 250Ω will decrease the loop gain

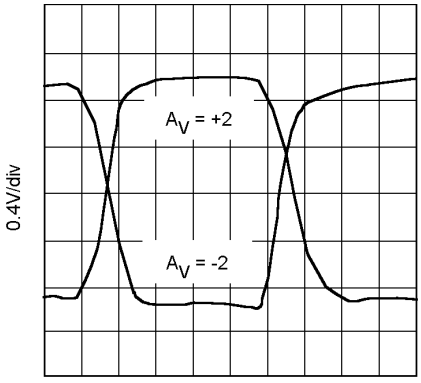
Application Division (Continued)

and band width, while decreasing it will increase the loop gain possibly leading to inadequate phase margin and closed-loop peaking. Conversely, fixing R_f will hold the frequency response constant while the closed-loop gain can be adjusted using R_g.

The CLC410 departs from this idealized analysis to the extent that the inverting input impedance is finite. With the low quiescent power of the CLC410, $Z_i \approx 50\Omega$ leading to drop in loop gain and bandwidth at high gain settlings, as given by equation 2. The second term in Equation 2 accounts for the division in feedback current that occurs between Z_i and $R_f \| R_g$ at the inverting node of the CLC410. This decrease in bandwidth can be circumvented as described in "Increasing Bandwidth at High Gains." Also see "Current Feedback Amplifiers" in the National Databook for a thorough discussion of current feedback op amps.

Increasing Bandwidth At High Gains

Bandwidth may be increased at high closed-loop gains by adjusting R_f and R_g to make up for the losses in loop gain that occur at these high gain settlings due to current division at the inverting input. An approximate relationship may be obtained by holding the LG expression constant as the gain is changed from the design point used in the specifications (that is, R_f = 250Ω and R_g = 250Ω). For the CLC400 this gives,



(3)

where A_V is the non-inverting gain. Note that with A_V = +2 we get the specified R_f = 250Ω, while at higher gains, a lower value gives stable performance with improved bandwidth.

DC Accuracy and Noise

Since the two inputs for the CLC410 are quite dissimilar, the noise and offset error performance differs somewhat from that of a standard differential input amplifier. Specifically, the inverting input current noise is much larger than the non-inverting current noise. Also the two input bias currents are physically unrelated rendering bias current cancellation through matching of the inverting and non-inverting pin resistors ineffective.

In Equation 4, the output offset is the algebraic sum of the equivalent input voltage and current sources that influence DC operation. Output noise is determined similarly except that a root-sum-of-squares replaces the algebraic sum. R_s is the non-inverting pin resistance.

Equation 4

Output Offset $V_O = \pm IBNx\ R_S(1+R_f/R_g) \pm$

$VIO\ (1+R_f/R_g) \pm IBIx\ R_f$

An important observation is that for fixed R_f, offsets as referred to the input improve as the gain is increased (divide all terms by $1+R_f/R_g$). A similar result is obtained for noise where noise figure improves as a gain increases.

The input noise plot shown in the CLC400 datasheet applies equally as well to the CLC410.

Capacitive Feedback

Capacitive feedback should not be used with the CLC410 because of the potential for loop instability. See Application Note OA-7 for active filter realizations with the CLC410.

Offset Adjustment Pin

Pin 1 can be connected to a potentiometer as shown in *Figure 1* and used to adjust the input offset of the CLC410. Full range adjustment of ±5V on pin 1 will yield a ±10mV input offset adjustment range. Pin 1 should always be bypassed to ground with a ceramic capacitor located close to the package for best settling performance.

Printed Circuit Layout

As with any high frequency device, a good PCB layout will enhance performance. Ground plane construction and good power supply bypassing close to the package are critical to achieving full performance. In the non-inverting configuration, the amplifier is sensitive to stray capacitance to ground at the inverting input. Hence, the inverting node connections should be small with minimal coupling to the ground plane. Shunt capacitance across the feedback resistor should not be used to compensate for this effect.

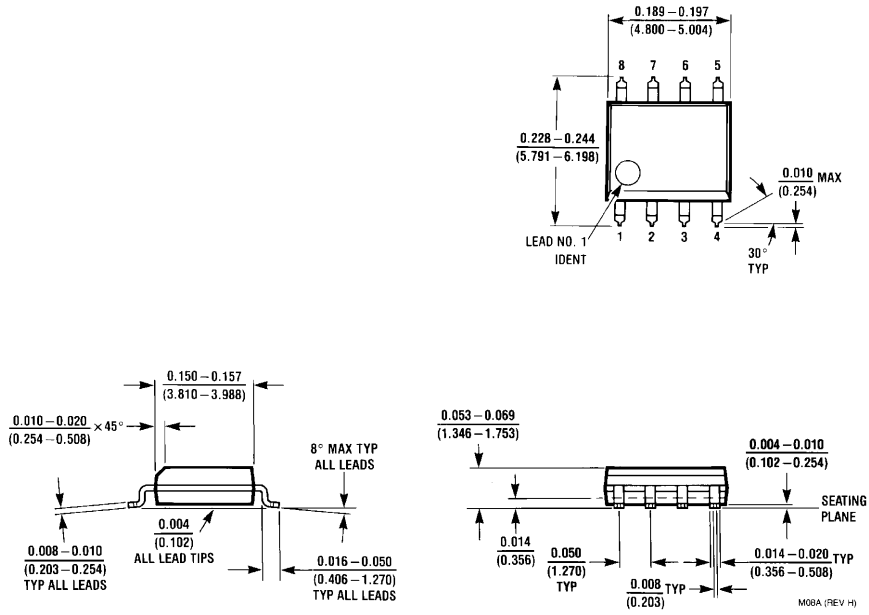
Parasitic or load capacitance directly on the output will introduce additional phase shift in the loop degrading the loop phase margin and leading to frequency response peaking. A small series resistor before the capacitance effectively decouples this effect. The graphs on the preceding page illustrates the required resistor value and resulting performance vs. capacitance.

Precision buffed resistors (PRP8351 series from Precision Resistive Products) with low parasitic reactances were used to develop the data sheet specifications. Precision carbon composition resistors will also yield excellent results. Standard spirally-trimmed RN55D metal film resistors will work with a slight decrease in bandwidth due to their reactive nature at high frequencies.

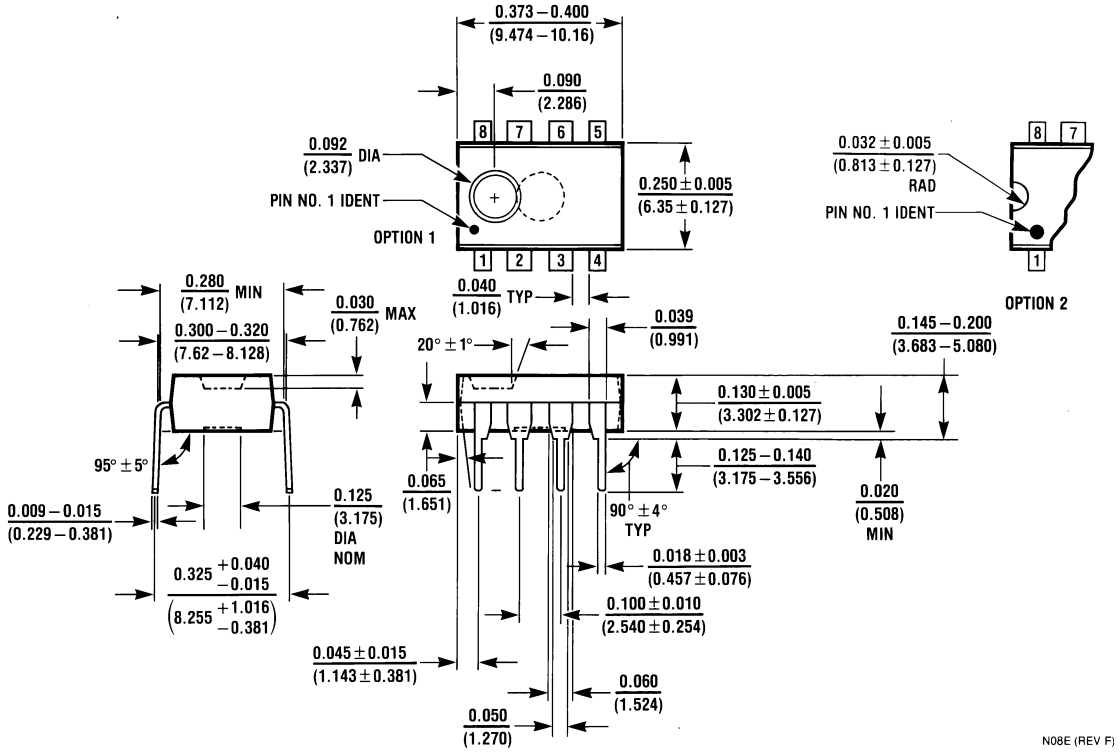
Evaluation PC boards (part no. 730013 for through-hole and 730027 for SOIC) for the CLC404 are available.

Physical Dimensions inches (millimeters)

unless otherwise noted



8-Pin SOIC
NS Package Number M08A



8-Pin MDIP
NS Package Number N08E

Notes

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