Dual P-Channel 1.8-V (G-S) MOSFET

CHARACTERISTICS

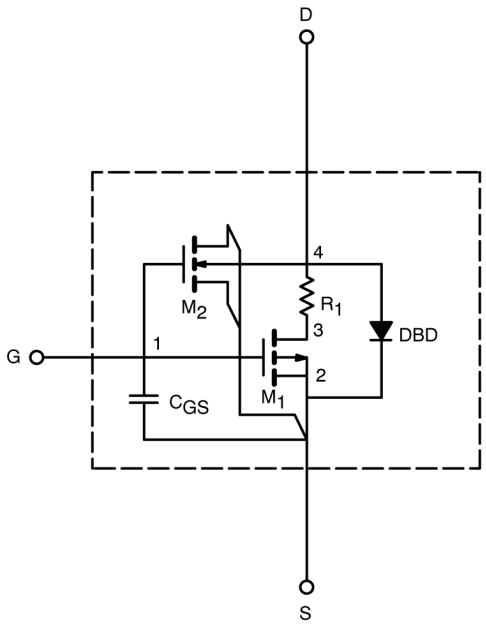
- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit mode is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0-to-5V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC

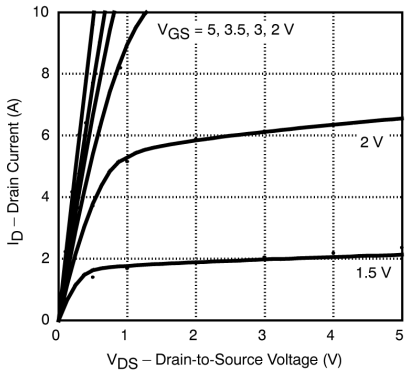


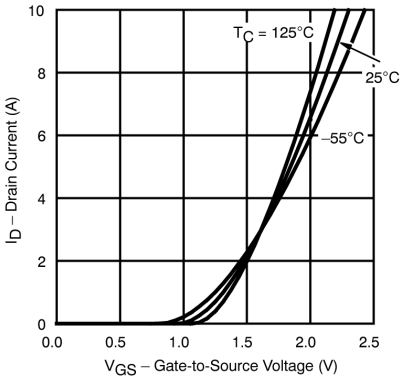
This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

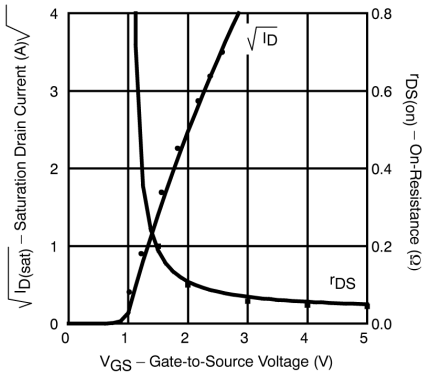
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	**Symbol**	**Test Condition**	**Simulated Data**	**Measured Data**	**Unit**
Static					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\mu A$	0.81		V
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} < -5V$, $V_{GS} = -4.5V$	43		A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	$V_{GS} = -4.5V$, $I_D = -3.4A$	0.053	0.058	Ω
		$V_{GS} = -2.5V$, $I_D = -2.7A$	0.085	0.090	
		$V_{GS} = -1.8V$, $I_D = -1A$	0.129	0.131	
Forward Transconductance[a]	g_{fs}	$V_{DS} = -5V$, $I_D = -3.4A$	8.3	8	S
Diode Forward Voltage[a]	V_{SD}	$I_S = -0.90A$, $V_{GS} = 0V$	- 0.80	- 0.80	V
Dynamic[b]					
Total Gate Charge	Q_g	$V_{DS} = -4V$, $V_{GS} = -4.5V$, $I_D = -3.4A$	5.9	5.9	nC
Gate-Source Charge	Q_{gs}		1.3	1.3	
Gate-Drain Charge	Q_{gd}		1.4	1.4	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -4V$, $R_L = 4\Omega$ $I_D \cong -1A$, $V_{GEN} = -4.5V$, $R_G = 6\Omega$	38	20	ns
Rise Time	t_r		68	70	
Turn-Off Delay Time	$t_{d(off)}$		26	35	
Fall Time	t_f		35	35	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -0.90A$, di/dt = 100A/µs	33	30	

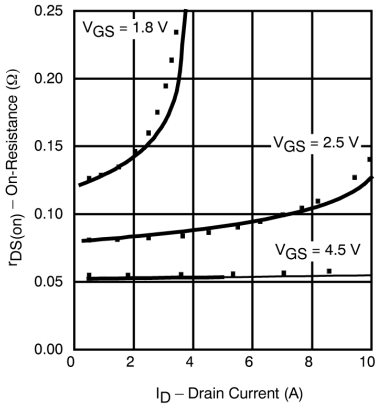
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

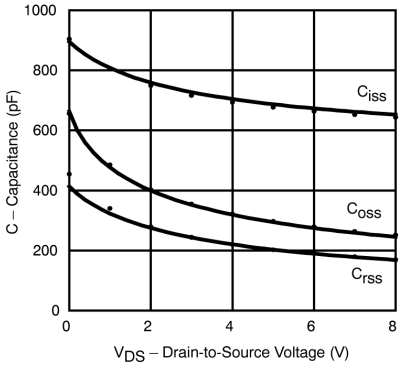
COMPARISON OF MODEL WITH MEASURED DATA (T_J=25°CUNLESS OTHERWISE NOTED)

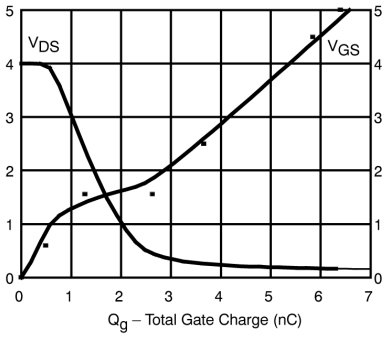












Note: Dots and squares represent measured data.