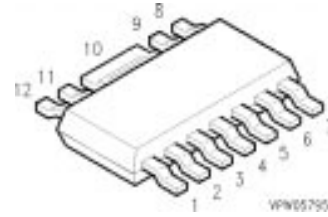


*Preliminary Datasheet*

- \* Power amplifier for PCN/PCS applications
- \* Fully integrated 2 stage amplifier
- \* Operating voltage range: 2.7 to 6 V
- \* Overall power added efficiency 35 %
- \* Input matched to 50  $\Omega$ , simple output match



ESD: Electrostatic discharge sensitive device,  
observe handling precautions!

Type	Marking	Ordering code (8-mm taped)	Package 1)
<b>CGY 181</b>	<b>CGY 181</b>	<b>Q68000-A8883</b>	<b>MW 12</b>

**Maximum ratings**

Characteristics	Symbol	max. Value	Unit
Positive supply voltage	$V_D$	9	V
Negative supply voltage <sup>2)</sup>	$V_G$	-8	V
Supply current	$I_D$	2	A
Channel temperature	$T_{Ch}$	150	$^{\circ}\text{C}$
Storage temperature	$T_{stg}$	-55...+150	$^{\circ}\text{C}$
RF input power	$P_{in}$	25	dBm
Total power dissipation ( $T_s \leq 81^{\circ}\text{C}$ ) <i>T<sub>s</sub>: Temperature at soldering point</i>	$P_{tot}$	5	W

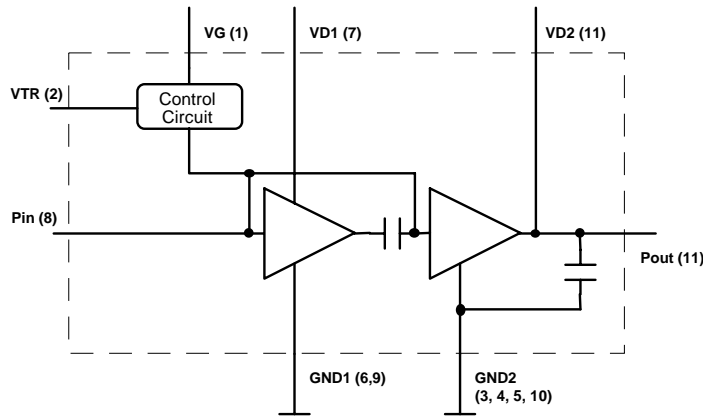
**Thermal Resistance**

Channel-soldering point	$R_{thChS}$	$\leq 14$	K/W
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1) Plastic body identical to SOT 223, dimensions see chapter Package Outlines

2)  $V_G = -8\text{V}$  only in combination with  $V_{TR} = 0\text{V}$ ;  $V_G = -6\text{V}$  while  $V_{TR} \neq 0\text{V}$

Functional block diagramm:



Short description of CGY181 operation:

A negative voltage between -4V to -6V (stabilization not necessary) has to be connected to the VG-pin, a positive supply voltage has to be applied to the VD-pins.

The VTR-pin has to be switched to 0V (GND) during transmit operation. The MMIC CGY181 is self-biased, the operating current is adjusted by the internal control circuit.

In receive mode the VTR-pin is not

connected (shut off mode).

Pin #		Configuration
1	<b>VG</b>	Negative voltage at control circuit (-4V...-8V)
2	<b>VTR</b>	Control voltage for transmit mode (0V) or receive mode (open)
3,4,5,10	<b>GND 2</b>	RF and DC ground of the 2nd stage
6,9	<b>GND 1</b>	RF and DC ground of the 1st stage
7	<b>VD1</b>	Positive drain voltage of the 1st stage
8	<b>RFin</b>	RF input power
11	<b>VD2,RFout</b>	Positive drain voltage of the 2nd stage, RF output power
12	-	not connected

DC characteristics

Characteristics	Symbol	Conditions	min	typ	max	Unit
Drain current stage 1	$IDSS1$	$VD=3V, VG=0V, VTR$ n.c.	0.6	0.9	1.2	A
	stage 2		$IDSS2$	2.4	3.5	4.8
Drain current with active current control	$ID$	$VD=3V, VG=-4V, VTR=0V$		1.0		A
Transconductance (stage 1 and 2)	$gfs1$	$VD=3V, ID=350mA$	0.28	0.32	-	S
	$gfs2$	$VD=3V, ID=700mA$	1.1	1.3	-	S
Pinch off voltage	$Vp$	$VD=3V, ID<500\mu A$ (all stages)	-3.8	-2.8	-1.8	V

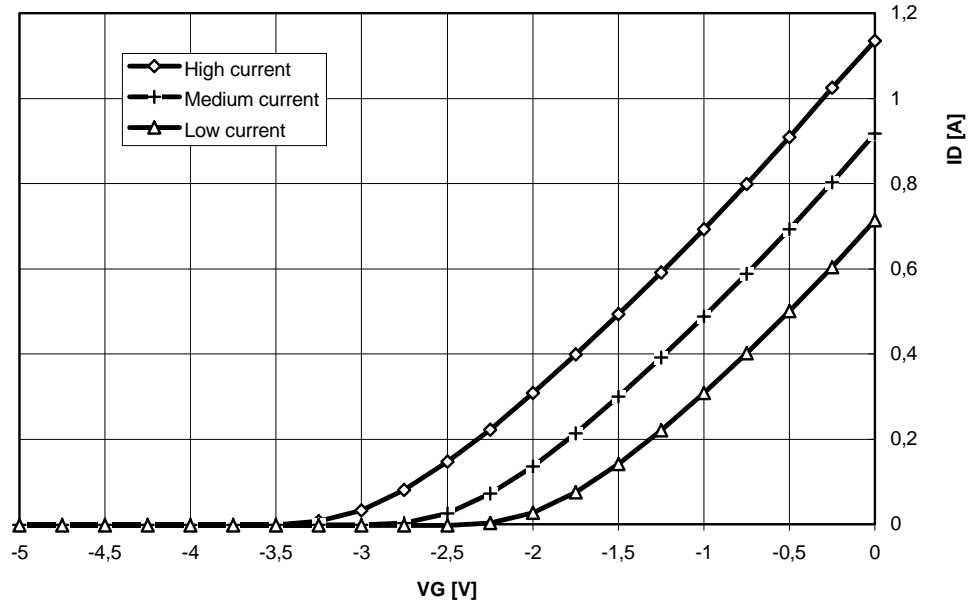
## Electrical characteristics

( $T_A = 25^\circ\text{C}$ ,  $f = 1.75\text{ GHz}$ ,  $Z_S = Z_L = 50\text{ Ohm}$ ,  $V_D = 3.6\text{V}$ ,  $V_G = -4\text{V}$ , VTR pin connected to ground, unless otherwise specified)

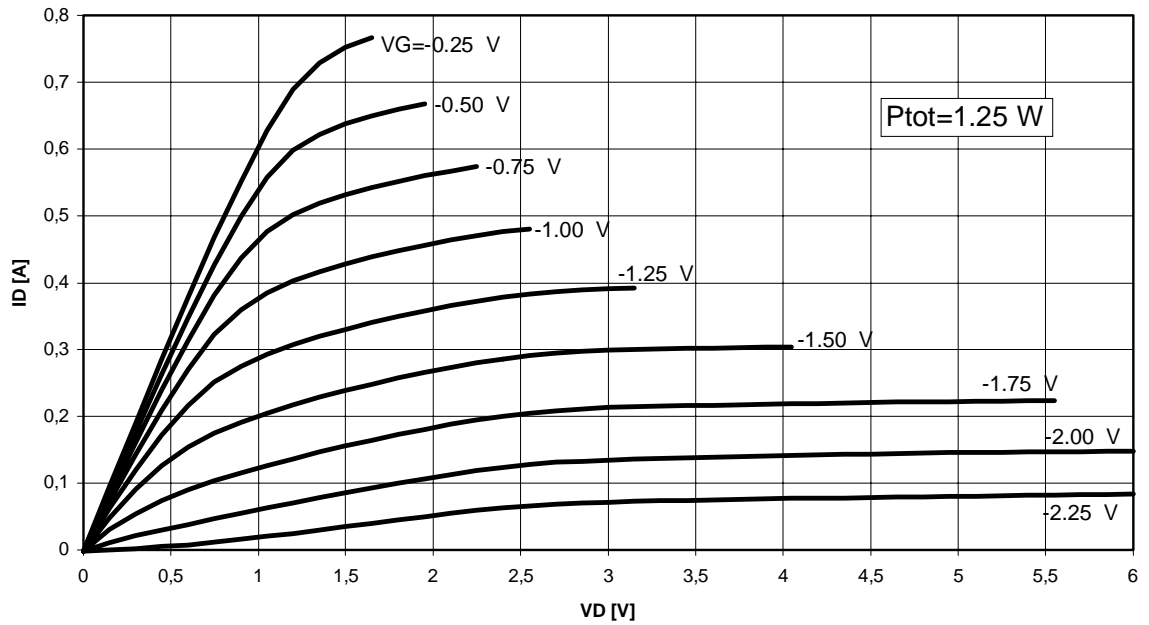
Characteristics	Symbol	min	typ	max	Unit
Supply current Pin= 0 dBm	$I_{DD}$	-	1.2	-	A
Negative supply current (normal operation)	$I_G$	-	2	3	mA
Shut-off current VTR n.c.	$I_D$	-	400	-	$\mu\text{A}$
Negative supply current (shut off mode, VTR pin n.c.)	$I_G$	-	10	-	$\mu\text{A}$
Small signal gain $P_{in} = -5\text{dBm}$	$G$	-	20.5	-	dB
Power Gain $V_D = 3.6\text{V}$ , Pin = 16 dBm	$G$	14.5	15.5	-	dB
Power Gain $V_D = 5\text{V}$ , Pin = 16 dBm	$G$	17.5	18.5	-	dB
Output Power $V_D = 3.6\text{V}$ , Pin = 16 dBm	$P_O$	30.5	31.5	-	dBm
Output Power $V_D = 5\text{V}$ , Pin = 16 dBm	$P_O$	33.5	34.5	-	dBm
Overall Power Added Efficiency $V_D = 3.6\text{V}$ , $P_{in} = 16\text{ dBm}$	$\eta$	-	37	-	%
Overall Power Added Efficiency $V_D = 5\text{V}$ , $P_{in} = 16\text{ dBm}$	$\eta$	-	35	-	%
Harmonics ( $P_{in} = 16\text{dBm}$ ) $V_D = 3.6\text{V}$ ( $P_{out} = 31.85\text{dBm}$ )	$2f_0$ $3f_0$	-	-44.8 -70	-	dBc
Harmonics ( $P_{in} = 16\text{dBm}$ ) $V_D = 5\text{V}$ ( $P_{out} = 31.85\text{dBm}$ )	$2f_0$ $3f_0$	-	-45.1 -75	-	dBc
Input VSWR $V_D = 3.6\text{V}$			1.9:1		
Third order intercept point $f_1 = 1.7500\text{GHz}$ ; $f_2 = 1.7502\text{GHz}$ ; $V_D = 3.6\text{V}$	$IP_3$		41		dBm
Third order intercept point $f_1 = 1.7500\text{GHz}$ ; $f_2 = 1.7502\text{GHz}$ ; $V_D = 5\text{V}$	$IP_3$		44		dBm

All RF-measurements were done in a pulsed mode with a duty cycle of 10% ( $t_{on} = 0.33\text{ms}$ )!

DC-ID(VG) characteristics - typical values of stage 1, VD=3V

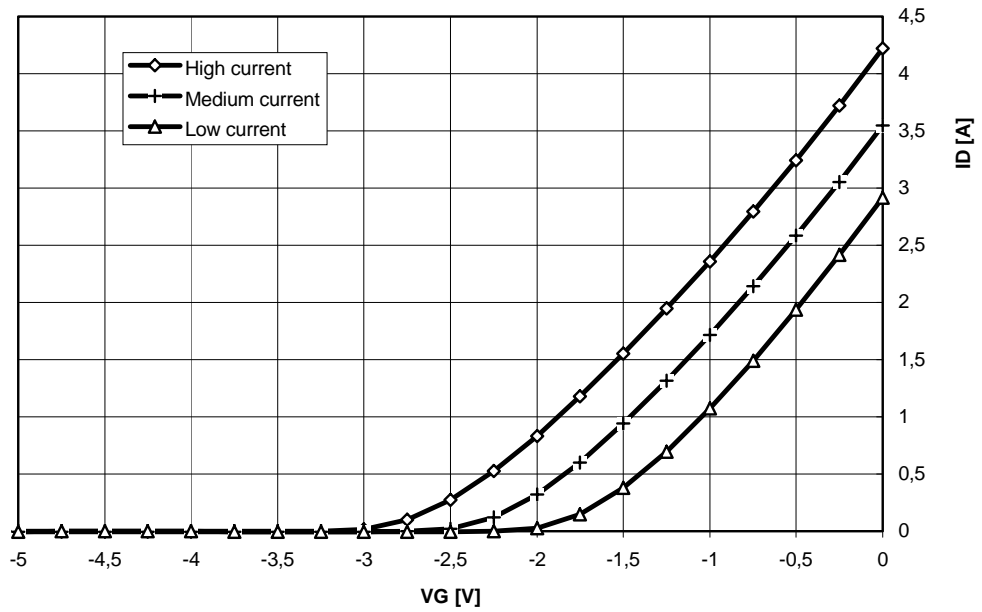


DC-Output characteristics - typical values of stage 1

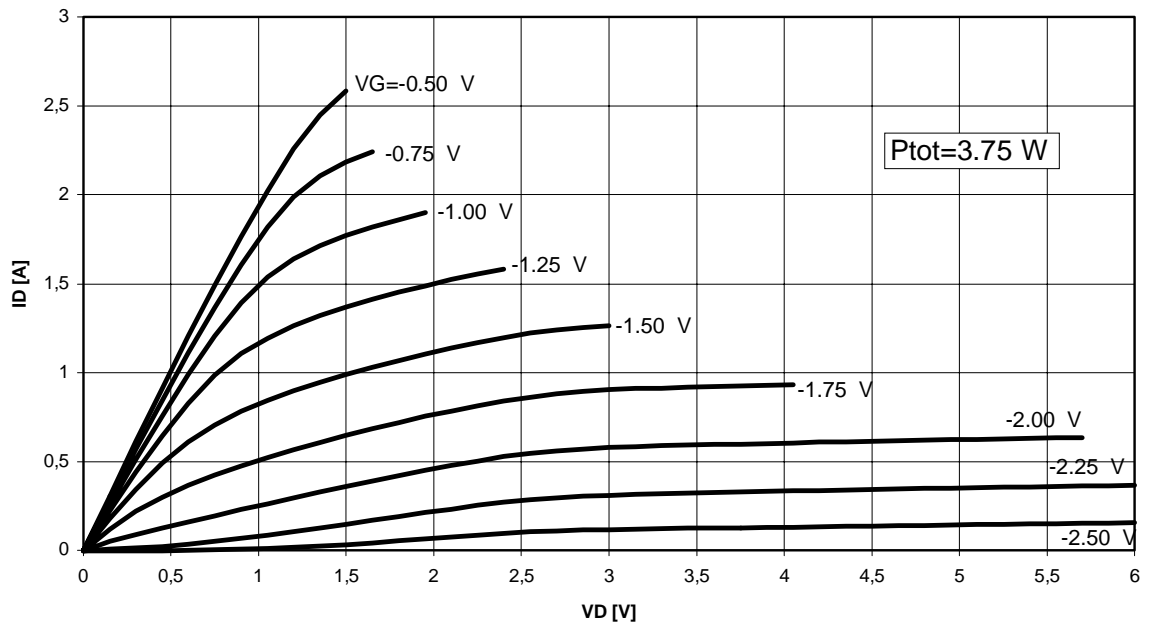


Pin 2 ( $V_{TR}$ ) has to be open during measuring DC-characteristics!

DC-ID(VG) characteristics - typical values of stage 2, VD=3V



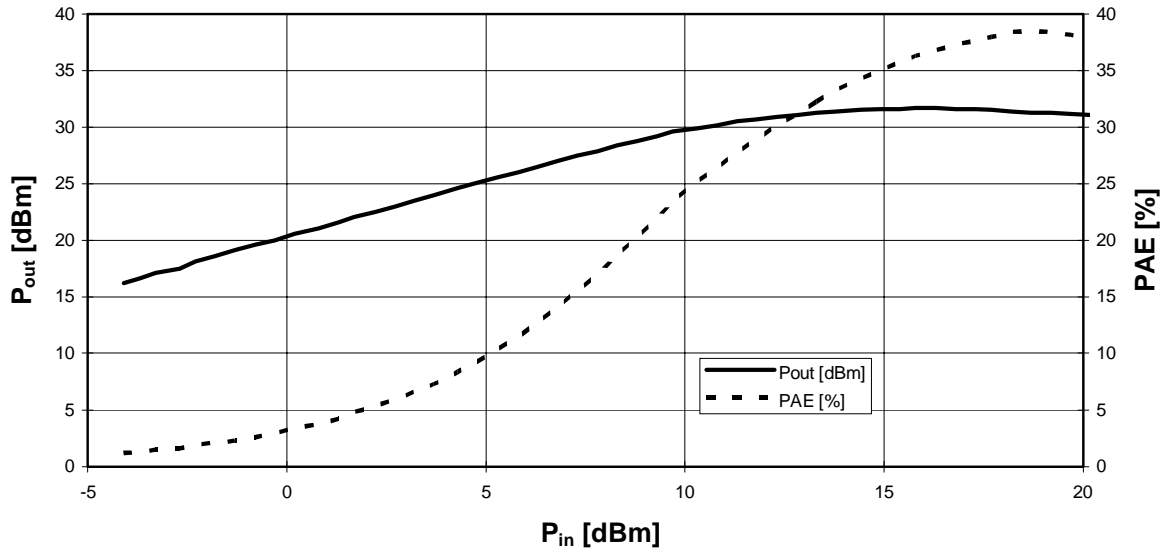
DC-Output characteristics - typical values of stage 2



Pin 2 ( $V_{TR}$ ) has to be open during measuring DC-characteristics!

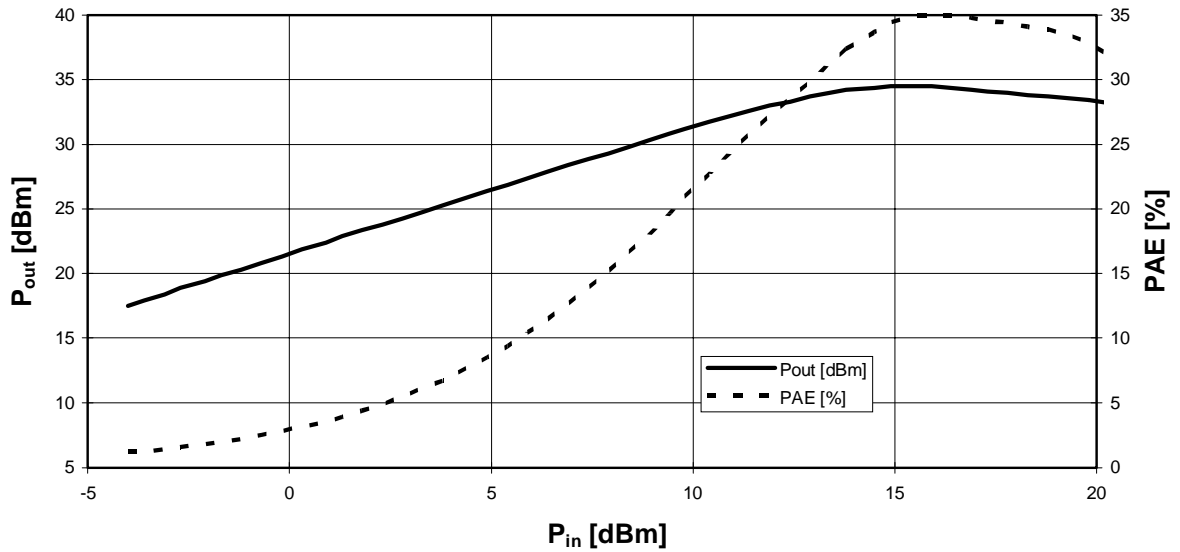
**P<sub>out</sub> and PAE vs. P<sub>in</sub>**

( V<sub>D</sub>=3.6V, V<sub>G</sub>=-4V, f=1.75GHz, pulsed with a duty cycle of 10%, t<sub>on</sub>=0.33ms )



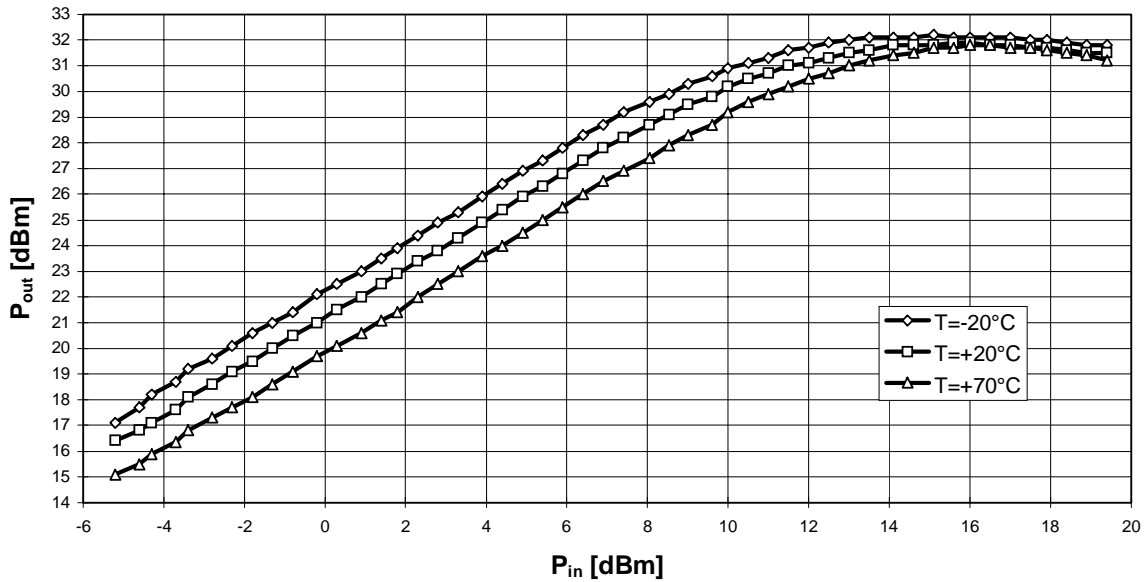
**P<sub>out</sub> and PAE vs. P<sub>in</sub>**

( V<sub>D</sub>=5V, V<sub>G</sub>=-4V, f=1.75GHz, pulsed with a duty cycle of 10%, t<sub>on</sub>=0.33ms )



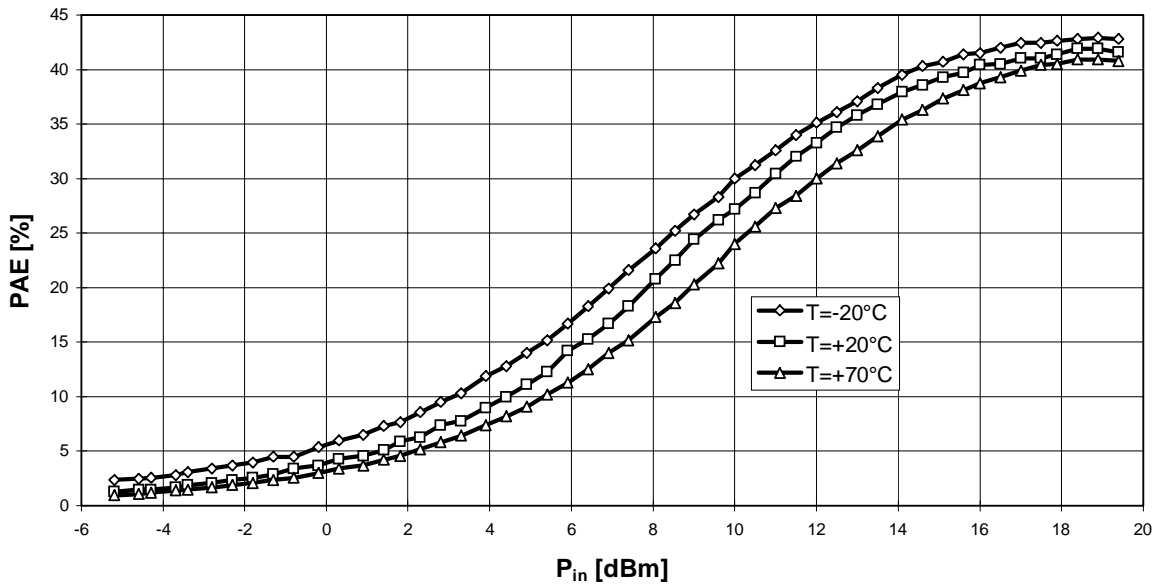
**Output power at different temperatures**

( $V_D=3.6V, V_G=-4V, f=1.75GHz$ , pulsed with a duty cycle of 10%,  $t_{on}=0.33ms$ )



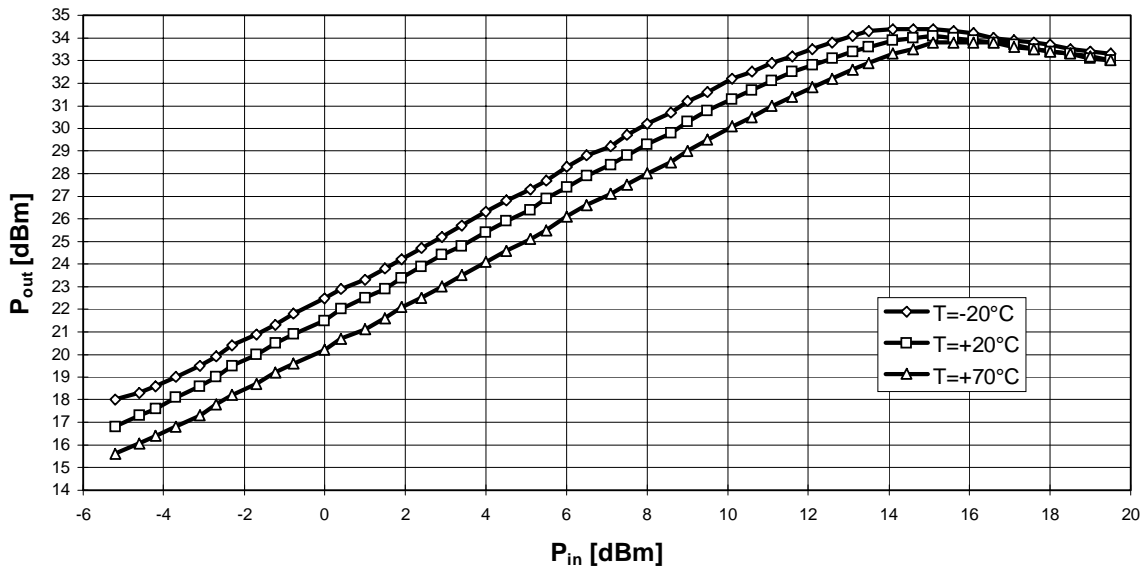
**Power added efficiency at different temperatures**

( $V_D=3.6V, V_G=-4V, f=1.75GHz$ , pulsed with a duty cycle of 10%,  $t_{on}=0.33ms$ )



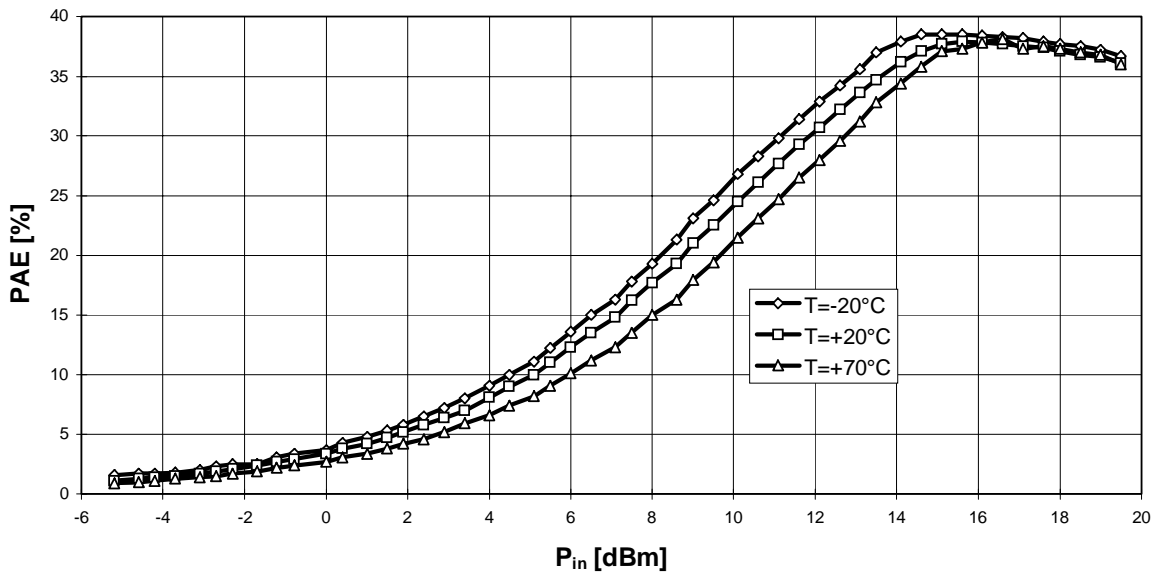
**Output power at different temperatures**

( $V_D=5V, V_G=-4V, f=1.75GHz$ , pulsed with a duty cycle of 10%,  $t_{on}=0.33ms$ )



**Power added efficiency at different temperatures**

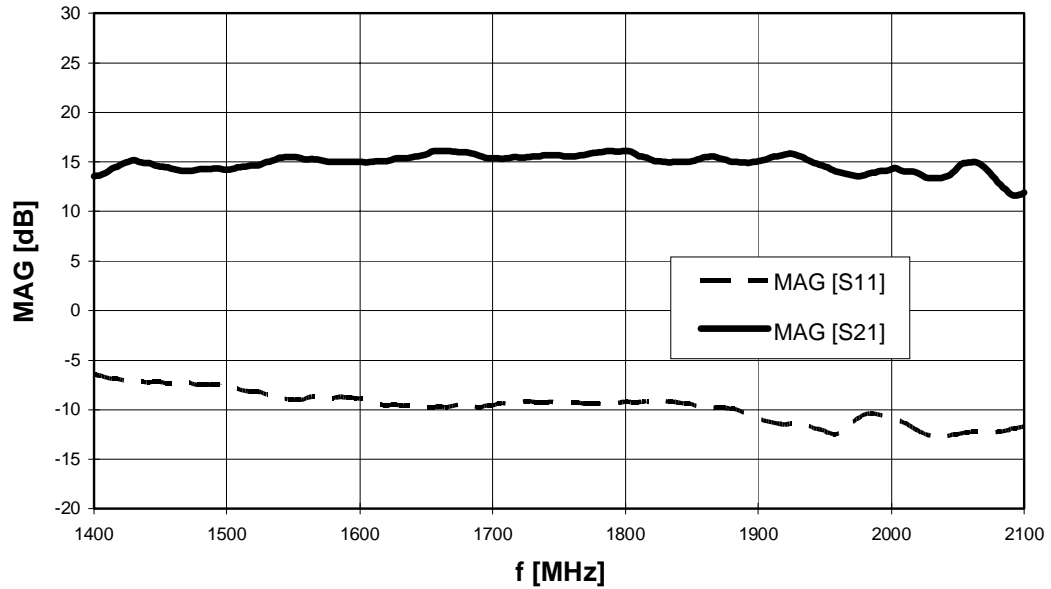
( $V_D=5V, V_G=-4V, f=1.75GHz$ , pulsed with a duty cycle of 10%,  $t_{on}=0.33ms$ )





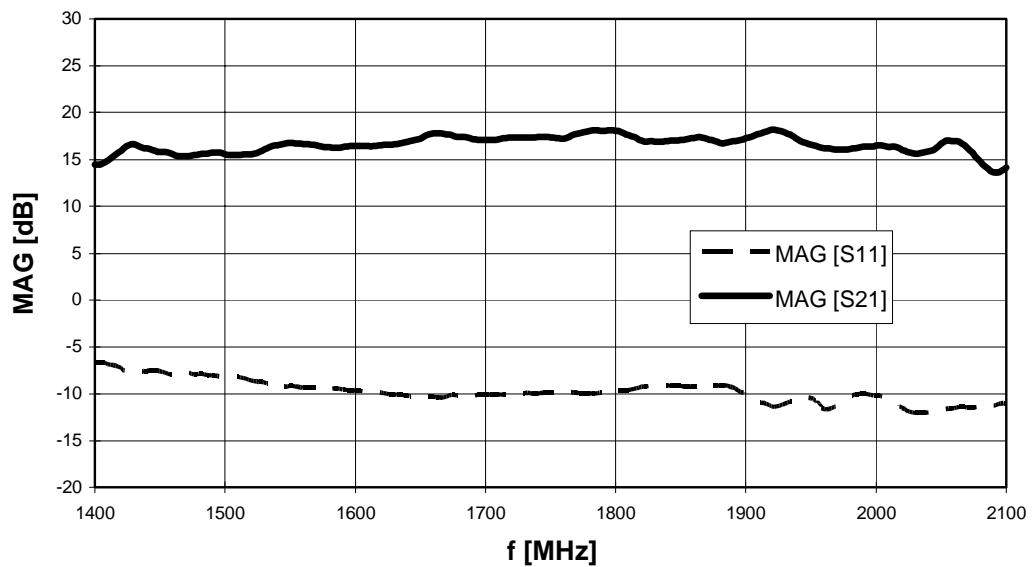
**Measured S-parameter at  $V_D=3.6V$  and  $P_{in}=16dBm$**

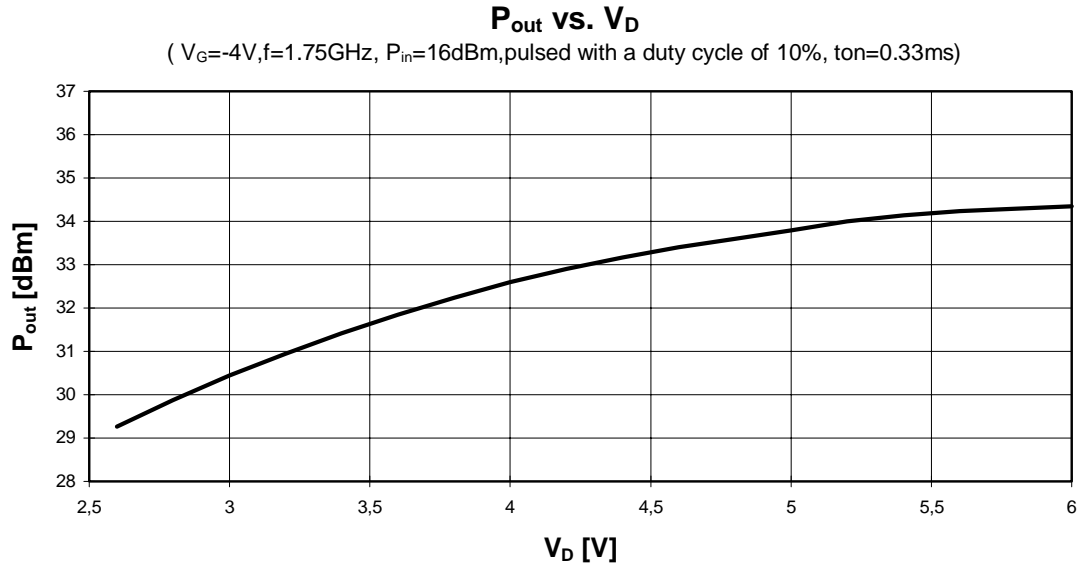
( $V_G=-4V$ , VTR connected to ground, pulsed with a duty cycle of 10%,  $t_{on}=0.33ms$ )



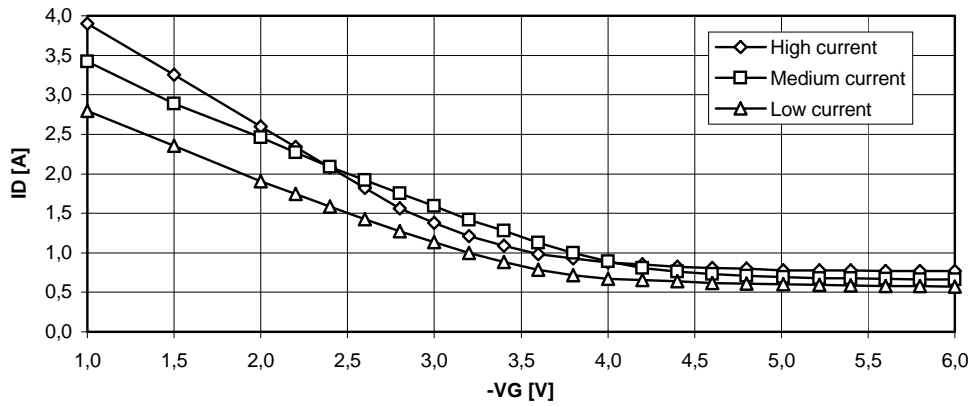
**Measured S-parameter at  $V_D=5V$  and  $P_{in}=16dBm$**

( $V_G=-4V$ , VTR connected to ground, pulsed with a duty cycle of 10%,  $t_{on}=0.33ms$ )

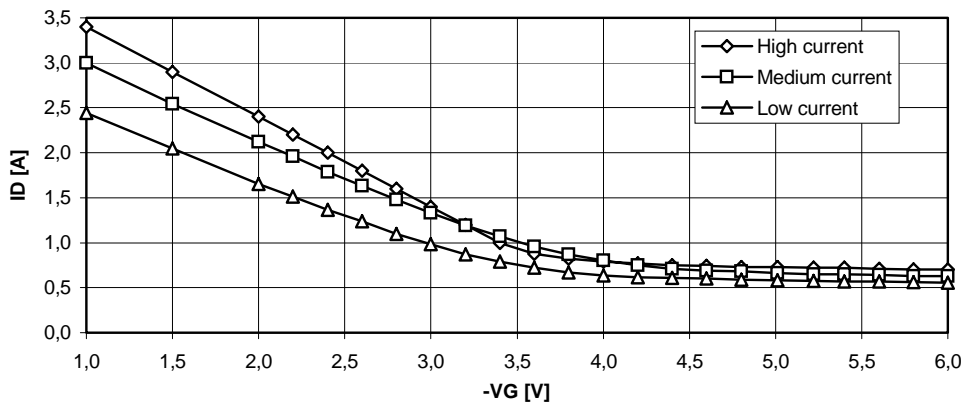




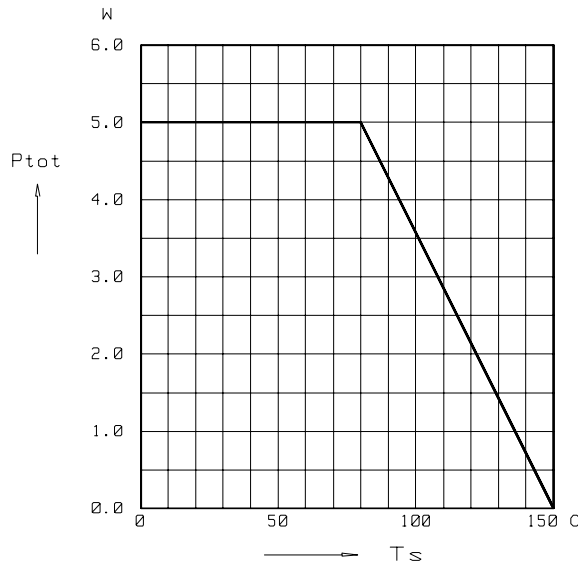
**Performance of internal bias control circuit @VD=3V**  
 (VTR=0V, pulsed with a duty cycle of 10%, ton=0.33ms)



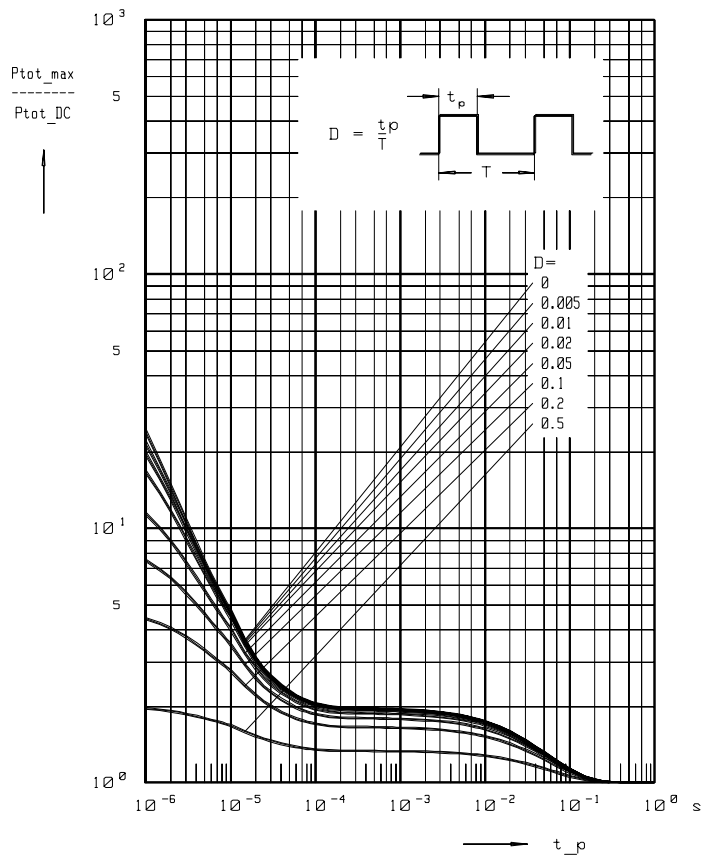
**Performance of internal bias control circuit @VD=5V**  
 (VTR=0V, pulsed with a duty cycle of 10%, ton=0.33ms)



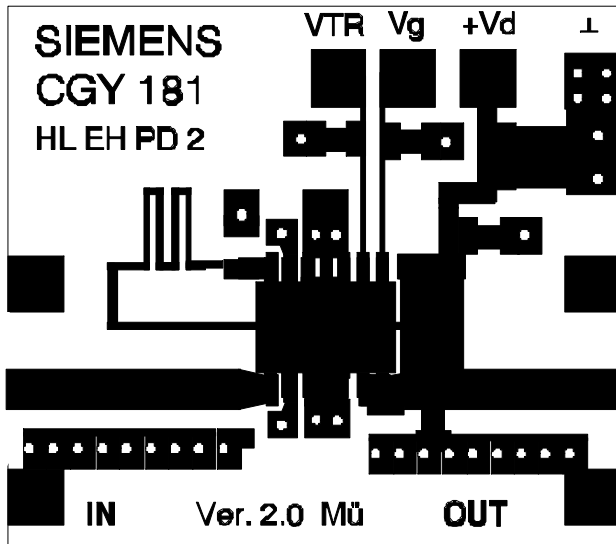
**Total Power Dissipation  $P_{tot}=f(T_s)$**



**Permissible pulse load  $P_{tot\_max}/P_{tot\_DC} = f(t_p)$**



**CGY181 application board:**



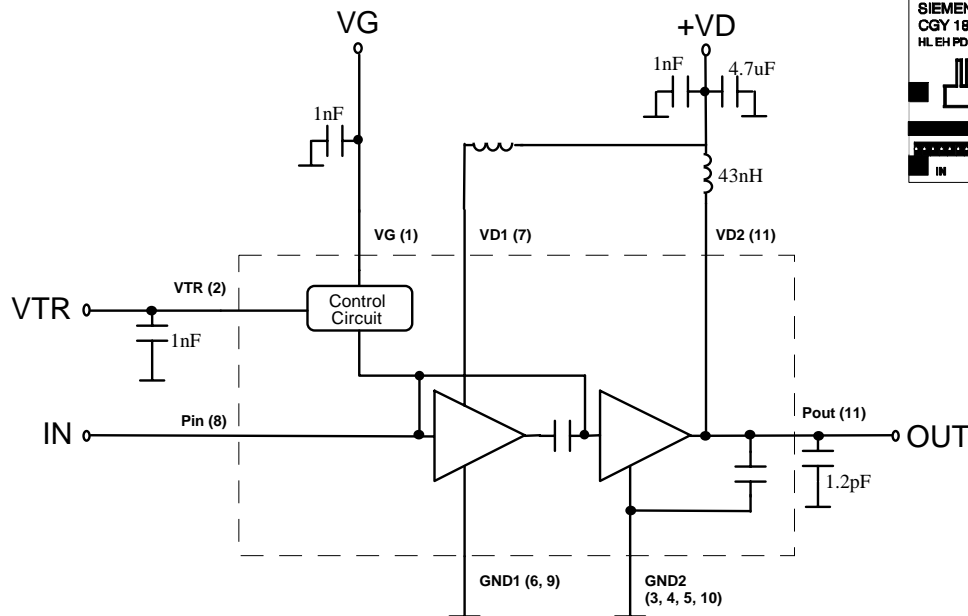
**Part Type**

**Description:**

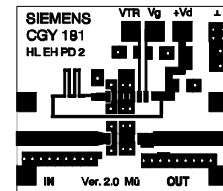
Part Type	Description:
CGY181	Siemens GaAs-MMIC
1nF	Capacitor SMD 0805
1nF	Capacitor SMD 0805
1nF	Capacitor SMD 0805
1p2	Capacitor SMD 0805
4μ7	Capacitor SMD Tantal
43nH	Coilcraft SMD Spring Inductor B10T (distributed by Ginsbury Electronic GmbH Am Moosfeld 85, D-81829 München Tel.: 089/45170-223)

Layout size is 30mm x 26mm.

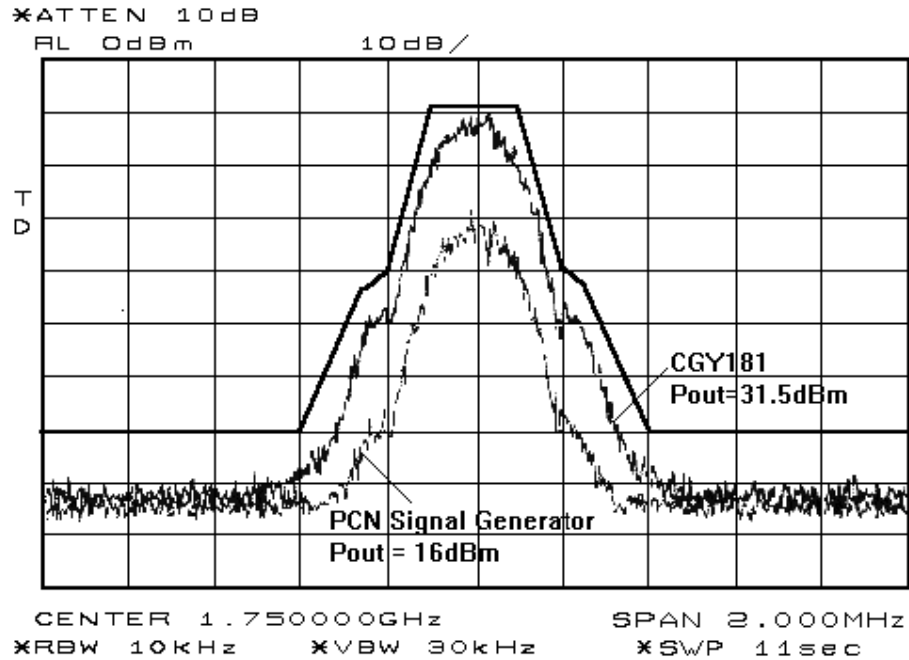
**Principal circuit:**



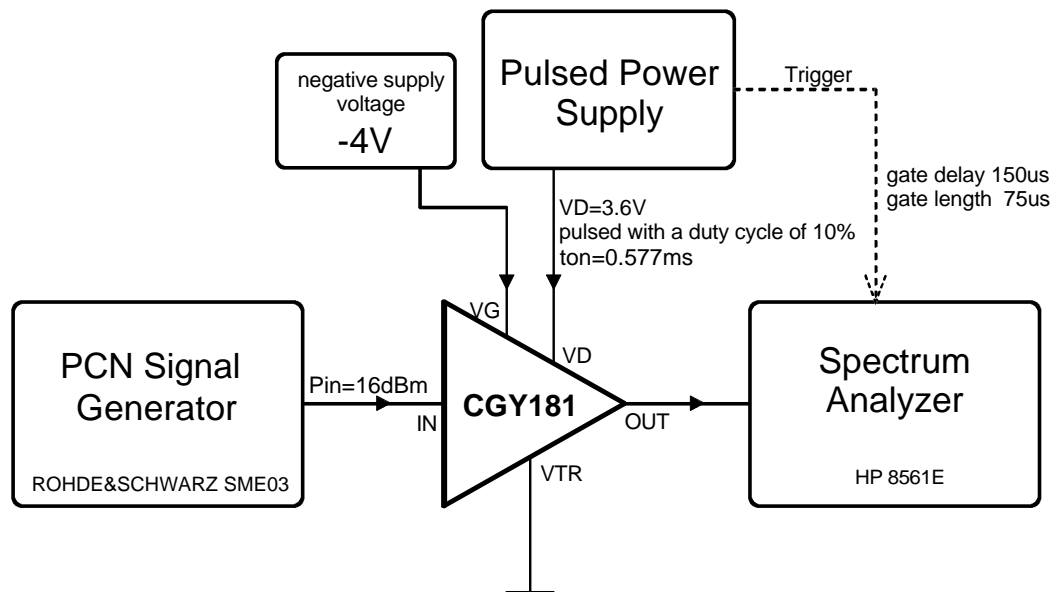
**Original Size:**



Emissions due to GMSK modulation:



Measurement was done with the following equipment:



## APPLICATION - HINTS

### 1. CW - capability of the CGY181

Proving the possibility of CW - operations there must be known the total power dissipation of the device. This value can be found as a function of temperature in the datasheet (page 12). The CGY181 has a maximum total power dissipation of  $P_{\text{tot}} = 5 \text{ W}$ .

As an example we take the operating point with a drain voltage  $V_{\text{D}} = 3.6 \text{ V}$  and a typical drain current of  $I_{\text{D}} = 1.2 \text{ A}$ . So the maximum DC - power can be calculated to:

$$P_{\text{DC}} = V_{\text{D}} \cdot I_{\text{D}} = 4.32 \text{ W}.$$

This value is smaller than 5W and CW - operation is possible.

By decoupling RF power out of the CGY181 the power dissipation of the device can be further reduced. Assuming a power added efficiency PAE of 35 % the total power dissipation  $P_{\text{tot}}$  can be calculated using the following formula:

$$P_{\text{tot}} = P_{\text{DC}} (1 - \text{PAE}) = 4.32 \text{ W} (1 - 0.35) = 2.808 \text{ W}$$

### 2. Operation without using the internal current control

If you don't want to use the internal current control, it is recommended to connect the negative gate voltage at pin 2 ( $V_{\text{TR}}$ ) instead of pin 1 ( $V_{\text{G}}$ ). In that case  $V_{\text{G}}$  is not connected.

### 3. Biasing and use considerations

Biasing should be timed in such a way that the gate voltage ( $V_{\text{G}}$ ) is always applied before the drain voltages ( $V_{\text{D}}$ ), and when returning to the standby mode, the drain voltages have to be removed before the gate voltage.