TELEVISION SIGNAL PROCESSING CIRCUIT

The TBA890 is a silicon monolithic integrated signal processing circuit for monochrome and colour television receivers.

It combines the following functions:

- video pre-amplifier with emitter-follower output and short circuit protection.
- blanking facility for the video amplifier.
- gated a.g.c. detector supplying the a.g.c. voltages for the vision i.f. amplifier and tuner.
- noise cancelling circuit in the a.g.c. and sync separator circuits.
- sync separator.
- automatic horizontal phase detector
- vertical sync pulse separator.

The circuit is designed for receivers equipped with tubes or transistors in the deflection and video output stages.

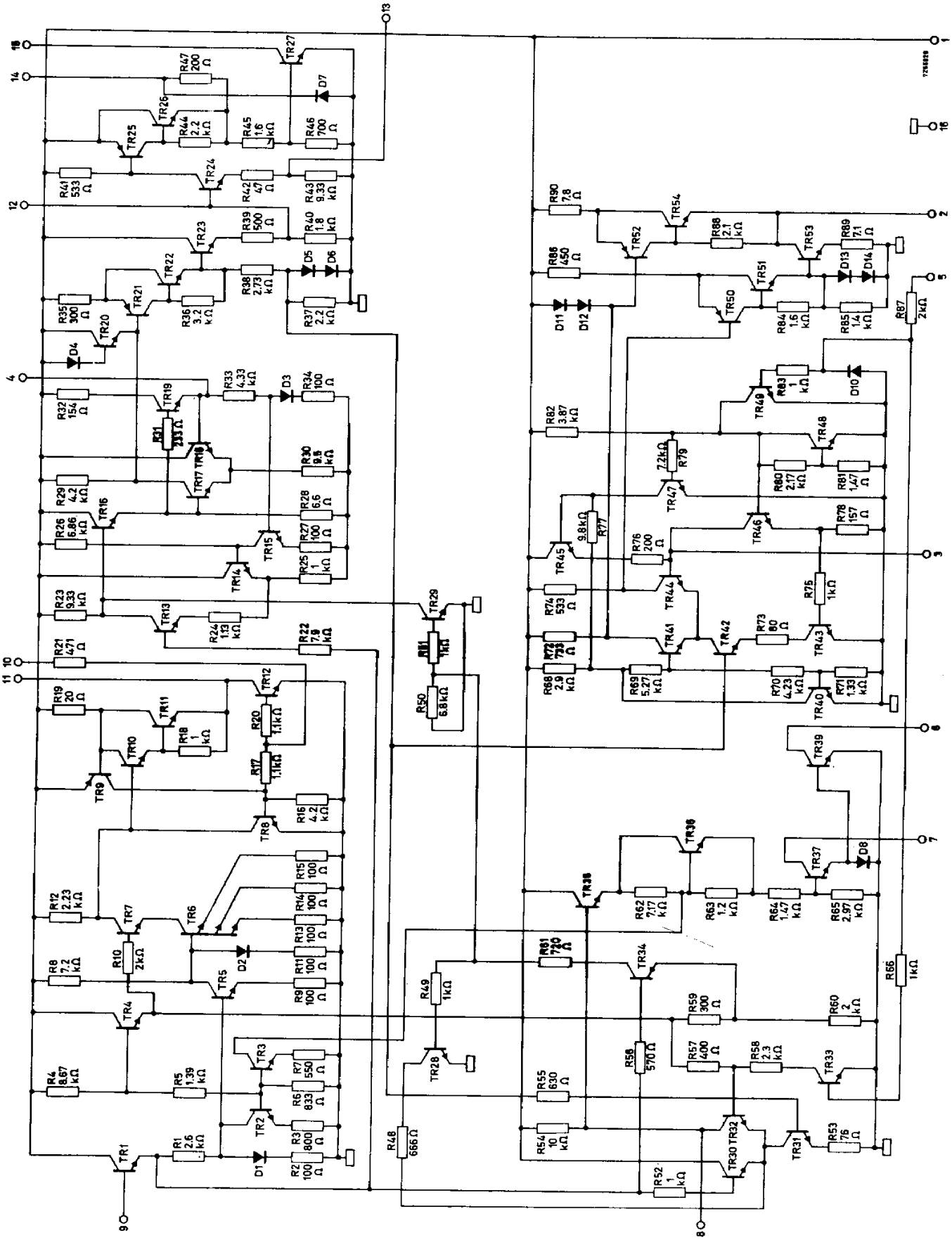
The control stages in the i.f. amplifier and the tuner have to be equipped with n-p-n transistors. The circuit is developed for signals with negative modulation.

QUICK REFERENCE DATA

Supply voltage	V_P	typ.	12	V
Ambient temperature	T_{amb}	typ.	25	°C
Video input voltage (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	2,7	V
Voltage gain of the video amplifier	G_v	typ.	7	dB
A.G.C. voltage for i.f. part	V_{7-16}	1,0 to	12	V
A.G.C. voltage for tuner	V_{6-16}	0,3 to	12	V
Output voltage range horizontal phase detector	V_{2-16}	2 to	10	V
Vertical sync output voltage (positive going pulse; peak-to-peak value)	$V_{14-16(p-p)}$	typ.	11	V

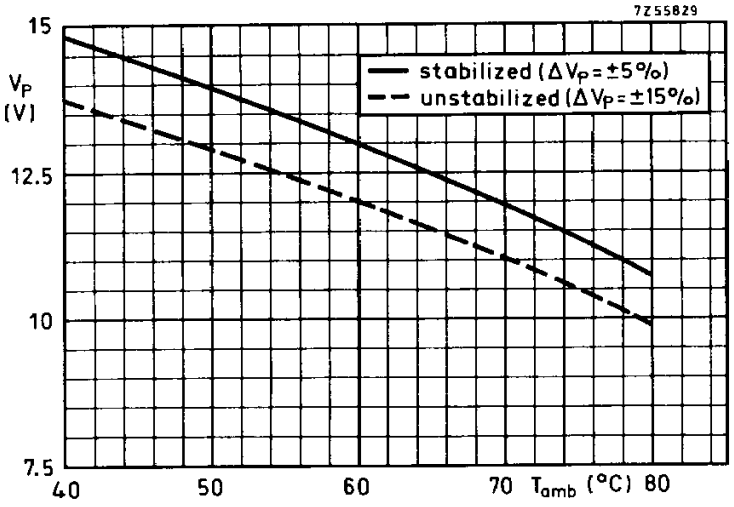
PACKAGE OUTLINES

TBA890 : 16-lead DIL; plastic (SOT-38).
TBA890Q: 16-lead QIL; plastic (SOT-58).



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.		20	V[1]
Power dissipation	P_{tot}	max.		700	mW
Temperatures					
Storage temperature	T_{stg}	−55	to	+125	°C
Operating ambient temperature	T_{amb}	-25	to	+80	°C



Maximum allowable nominal supply voltage as a function of the maximum ambient temperature.

[1] Allowed only while receiver is warming up.

CHARACTERISTICS

Supply voltage range	V_P	See curves on page 3		

The following characteristics are measured in the circuit on p. 7 at T_{amb} = 25 °C; V_P = 12 V.

Video amplifier				
Input resistance	R_{9-16}	>	30	kΩ
Input capacitance	C_{9-16}	<	3	pF
Bandwidth (3 dB)	B	>	5	MHz
Linearity (m)		>	0.9	
Rise time and fall time at the output	t_r; t_f	<	50	ns
Voltage gain	G_v	typ.	7	dB
Video input voltage (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	2.7	V [1]
D.C. bias video detector voltage	V_{bias}	typ.	6	V [2]
Video output voltage (peak-to-peak value)	$V_{11-16(p-p)}$	typ.	6	V [1]
Black level at the output	V_{11-16}	typ.	5	V [3]
Available video output current (peak value)	I_{11M}	≤	30	mA [4]
Tolerances on the video output voltages				
I.C. processing spreads	$\pm\Delta V_{11-16}$	<	420	mV [5]
Temperature drift	$-\Delta V_{11-16}$	typ.	1.8	mV/°C
Spreads over a.g.c. expansion (entire range)	$\pm\Delta V_{11-16}$	<	100	mV [6]
Supply voltage	$\frac{\Delta V_{11-16}}{\Delta V_P}$	typ.	0.5	

1) Signal with negative going sync.; this value is obtained only when the input signal meets the C.C.I.R. standard.

2) A voltage divider with 5% tolerance resistors is required between pin 9 and supply terminal.

3) Only valid if the video signal is in accordance with the C.C.I.R. standard.

4) The total load on pin 11 must be such that the d.c. output current $I_{11} \leq 15$ mA.

5) The spreads of the voltage divider for the bias of the video detector of ± 5% is included in this figure.

6) Variation about a nominal condition, the i.f. being fully controlled and the tuner uncontrolled.

CHARACTERISTICS (continued)

Tolerances on the black level at the output

I.C. processing spreads	$\pm\Delta V_{11-16}$	<	420	mV[1]
Temperature drift	$-\Delta V_{11-16}$	typ.	1.7	mV/°C
Spreads over a.g.c. expansion (entire range)	$\pm\Delta V_{11-16}$	<	130	mV[2]
Supply voltage	$\frac{\Delta V_{11-16}}{\Delta V_P}$	typ.	0.4	

Video blanking

Input voltage (peak-to-peak value)	$V_{10-16(p-p)}$		1 to 5	V
Input resistance	R_{10-16}	typ.	1	kΩ
Output voltage during blanking	V_{11-16}	<	500	mV

A.G.C. circuit

Range of control voltage i.f. amplifier	V_{7-16}		1 to 12	V[3]
Range of control voltage tuner	V_{6-16}		0.3 to 12	V[3]
Signal expansion for full control of i.f. amplifier and tuner		typ.	0.5	dB
Current i.f. control point	I_7	<	20	mA
Current tuner control point	I_6	<	20	mA
Current i.f. control point for tuner take-over	I_7	see note 4		
Keying input pulse (peak-to-peak value)	$V_{5-16(p-p)}$	see note 5		
Input resistance	R_{5-16}	typ.	2	kΩ

1) The spreads of the voltage divider for the bias of the video detector of ± 5% is included in this figure (pin 9).

2) Variation about a nominal condition, the i.f. being fully controlled and the tuner uncontrolled.

3) Positive going at increasing input signal.

4) This value depends on the ratio between the external impedances on pins 6 and 7. With equal impedances the current of the i.f. control point at tuner take-over will be about 16% from its maximum value (minimum control voltage).

5) Negative going pulse is required. The voltage during scan should be between 1 V and 2 V.

CHARACTERISTICS (continued)

Horizontal synchronization circuit				
Sync. separator			see note 1	
Output voltage range of phase detector	V_{2-16}		2 to 10	V [2]
Control steepness	S_φ	typ.	2.5	V/µs [3]
Phase deviation between front edge sync. pulse and front edge flyback pulse	φ_0	typ.	1.5	µs
Variation φ_0 caused by internal spreads	$\pm\Delta_{\varphi 0}$	typ.	0.3	µs [4]
Output voltage range as a frequency detector	V_{2-16}		4 to 8	V [5]
Vertical synchronization circuit				
Output voltage vertical sync. pulse generator	V_{14-16}	typ.	11	V
Output impedance	R_{14-16}	typ.	2	kΩ

1) The sync. pulse is sliced about 25% below top sync. level. A sliding bias circuit makes the slicing level independent of the signal strength.

2) Nominal voltage 6 V.

3) Higher values of this control steepness can be obtained by changing R_S (see circuit on page 7). For example R_S = 56 Ω, S_φ = 5 V/µs and R_S = 0, S_φ = ≥25 V/µs.

4) In addition to this figure ± 7% of the retrace time of the sawtooth generated on pin 3 has to be added to find the total spreads of φ_0.
This value of ± 7% is obtained only when the tolerance of the capacitor connected to pin 3 does not exceed ± 10%.

5) Nominal voltage 6 V.
The load impedance on pin 2 of the circuit on page 7 is about 50 kΩ.
When a higher impedance is used (tube equipped reactance stage) values from 2 V to 10 V can be reached.

APPLICATION INFORMATION