SECAM ENCODER

GENERAL DESCRIPTION

The TDA2506/T converts colour-difference signals (D'_R and D'_B) into sequential, frequency modulated signals according to the SECAM system. The signals (D'_R) and (D'_B) are the colour difference signals before low-frequency pre-emphasis; D'_R = -1,9 (R-Y) and D'_B = ∓1,5(B-Y). The circuit is intended for use in video cameras, games, recorders and players, PAL-SECAM transcoding circuits and SECAM test signal generators.

Synchronizing pulses required for operation of the TDA2506/T may be obtained from a universal sync generator SAA1043 or other pulse generator. All pulses are to be active HIGH and are as follows:

Horizontal sync pulses to pin 11
Half-rate horizontal sync (H/2) pulses to pin 9
Vertical sync pulses to pin 12
Chrominance blanking pulses to pin 13 (may include colour-killer pulses)

Frequency modulation is performed in conjunction with modulator-controller TDA2507.

Features

- Chrominance processor
- Vertical identification signal generator
- Timing pulse output to TDA2507
- Sample and hold circuit for control signal from TDA2507
- No adjustments of external components required (except high-frequency pre-emphasis (bell filter) stage)

QUICK REFERENCE DATA

Supply voltage	V_{4-2}	typ.	5 V
Supply current	I_4	typ.	45 mA
Reference voltage	V_{7-2}, V_{22-24}	typ.	3,5 V
Operating ambient temperature range	T_{amb}	−25 to	+70 °C
Storage temperature range	T_{stg}	−55 to	+150 °C

PACKAGE OUTLINES

TDA2506: 24-lead DIL; plastic (with internal heat spreader) (SOT101B).
TDA2506T: 24-lead mini-pack; plastic (SO24; SOT137A).

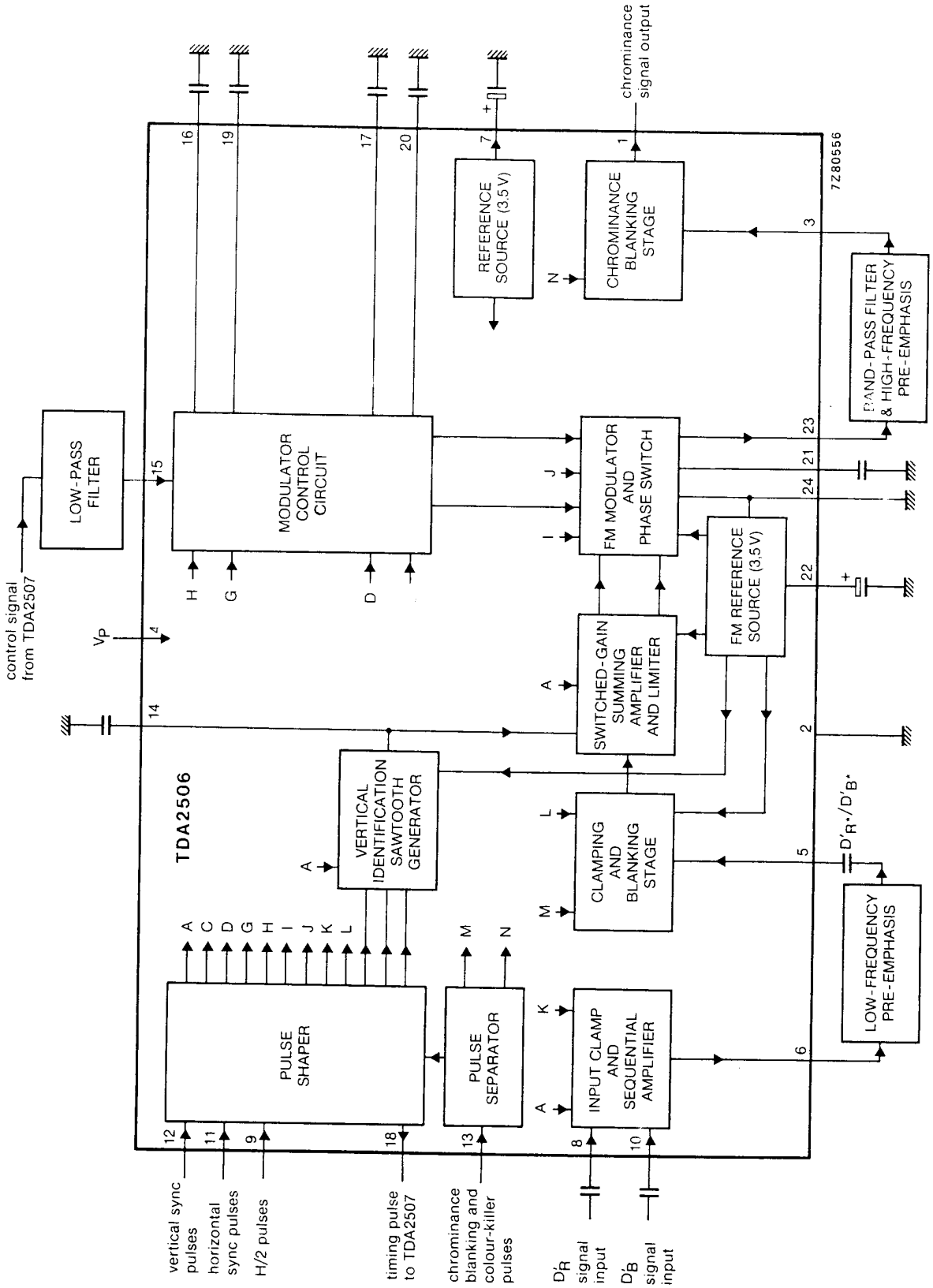


Fig. 1 Block diagram.

Pin functions

1. Chrominance signal output.
2. Ground.
3. Input to chrominance blanking stage from high-frequency pre-emphasis and band-pass filter.
4. Positive supply voltage.
5. Input to clamping and blanking stage from low-frequency pre-emphasis filter.
6. Output from sequential amplifier to low-frequency pre-emphasis filter.
7. Reference voltage output.
8. D'_R signal input.
9. H/2 pulse input (required only if specific phase sequencing is desired; should be connected to ground if not used).
10. D'_B signal input.
11. Horizontal sync pulse input.
12. Vertical sync pulse input.
13. Chrominance blanking and colour-killer pulse input.
14. Capacitor for vertical identification sawtooth.
15. Control signal input from TDA2507 via low-pass filter.
16. 4 406,250 kHz hold capacitor.
17. (R-Y) control.
18. Timing pulse output to TDA2507.
19. 4 250,000 kHz hold capacitor.
20. (B-Y) control.
21. FM modulator tuning capacitor (fixed).
22. FM reference voltage output.
23. FM modulator output to high frequency pre-emphasis and band-pass filter.
24. Ground connection for FM modulator.

FUNCTIONAL DESCRIPTION

Input clamp and sequential amplifier

This circuit clamps the zero levels of the D'_R and D'_B input signals (pins 8 and 10) to the reference voltage from pin 7. The input signals are switched into the amplifier sequentially by an internally delayed H/2 waveform. The amplifier output at pin 6 is D'_R when the delayed H/2 waveform is HIGH and D'_B when it is LOW. The stage gain is 1,5.

Clamping and blanking stage

After external low-frequency pre-emphasis, the sequential $D'_R{}^*$ and $D'_B{}^*$ signals are returned to the IC at pin 5. The signal amplitude at pin 5 is typically 0,5 V (peak-to-peak value) for 75% colour bar (EBU). Black levels are clamped to the FM reference voltage (pin 22). Blanking takes place during the chrominance blanking pulse and, if required, during the video blanking and/or colour killing pulses.

FUNCTIONAL DESCRIPTION (continued)

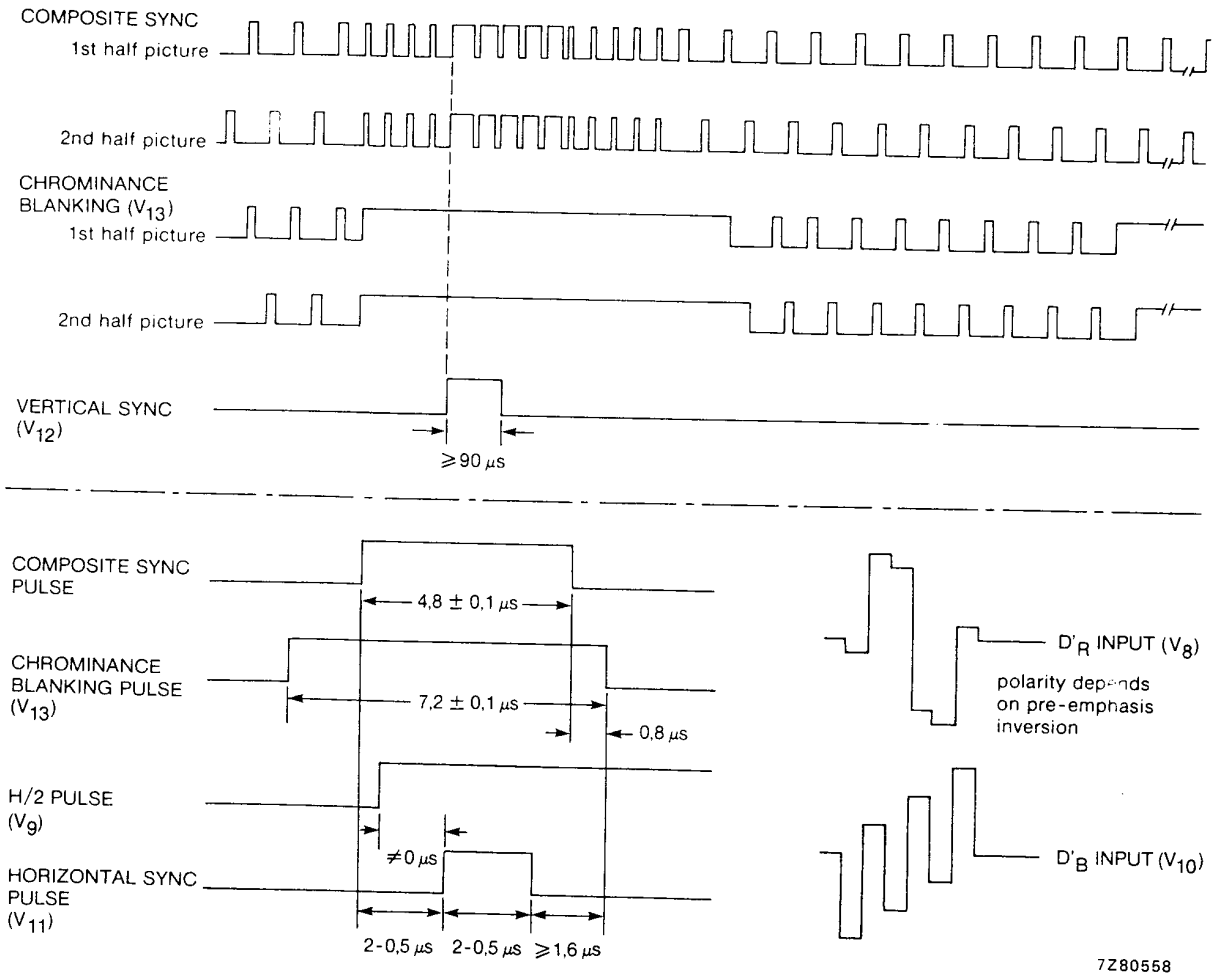


Fig. 2 Survey of input signals in relation to composite sync.

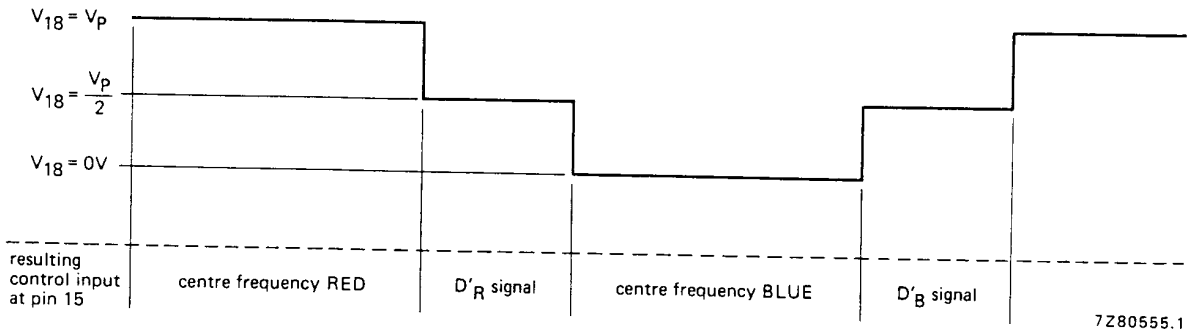


Fig. 3 Timing pulse output (pin 18) and resulting control input (pin 15).

Switched-gain summing amplifier and limiter

Inputs into the summing amplifier are the sequential D'_R* and D'_B* signals, the vertical identification sawtooth waveform and reference d.c. levels. The gain of the amplifier is switched by the internally delayed H/2 waveform to give the correct input amplitudes for the FM modulator (D'_R* gain = 280/230 x D'_B* gain). An offset is also introduced between the black levels of the D'_R* and D'_B* signals which corresponds to the upper and lower thresholds of the limiter.

FM modulator and phase switch

The FM modulator provides accurate FM modulation which follows the amplitude envelopes of the sequential D'_R* and D'_B* waveforms. The centre frequencies of 4 406,250 kHz for the D'_R* signal and 4 250,000 kHz for the D'_B* signal are controlled by d.c. levels from the sample and hold circuit (which in turn are controlled by the TDA2507). The upper and lower frequency limits are 4 756,000 ± 35 kHz and 3 900,000 ± 35 kHz.

Reference d.c. levels are switched within the FM modulator to define the starting phase of the modulator output (pin 23) at the initiation of each horizontal and vertical scan. The starting phase sequence is as follows:

vertical scan (frame to frame) 0°, 180°, 0°, 180°, repeating;

horizontal scan (line to line) 0°, 0°, 180°, 0°, 0°, 180°, repeating.

Chrominance blanking stage

The frequency modulated colour difference signals are passed via high-frequency pre-emphasis and band-pass filters to the chrominance blanking input at pin 3. The d.c. level of this input should be equal to the reference voltage at pin 7. Blanking occurs during the chrominance blanking pulse. The stage gain is 1,75.

Vertical identification sawtooth generator

Vertical sync, horizontal sync and chrominance blanking pulses are used to determine vertical identification (see Fig. 4). The vertical identification sawtooth generator is driven in opposite directions for identification signals IdR and IdB; the capacitor for the generator is connected at pin 14. If no vertical identification is required, pin 14 should be connected to the FM reference voltage at pin 22.

Pulse shaper

This stage developes all pulses that are required within the TDA2506 and also the timing pulses required for the modulator controller TDA2507 (see Fig. 3). Internal H/2 pulses are generated by a flip-flop working from the horizontal sync input (pin 11), this makes the H/2 input at pin 9 necessary only if it is required to lock the modulator into a specific phase sequence. If the H/2 input is not required, pin 9 should be connected to ground. A pulse separator at the chrominance blanking/colour-killer input (pin 13) allows this input to be used for blanking the sequential D'_R*/D'_B* signal.

Sample and hold circuit

This circuit provides reference voltages to the FM modulator which set the centre modulation frequencies for the sequential D'_R* and D'_B* signals. The reference voltage levels are supplied to pin 15 from the TDA2507 in a sequence that is time-related to D'_R*/D'_B* switching. The levels are sampled and then held for D'_R* using capacitors at pins 16 and 17, and for D'_B* using capacitors at pins 19 and 20.

FUNCTIONAL DESCRIPTION (continued)

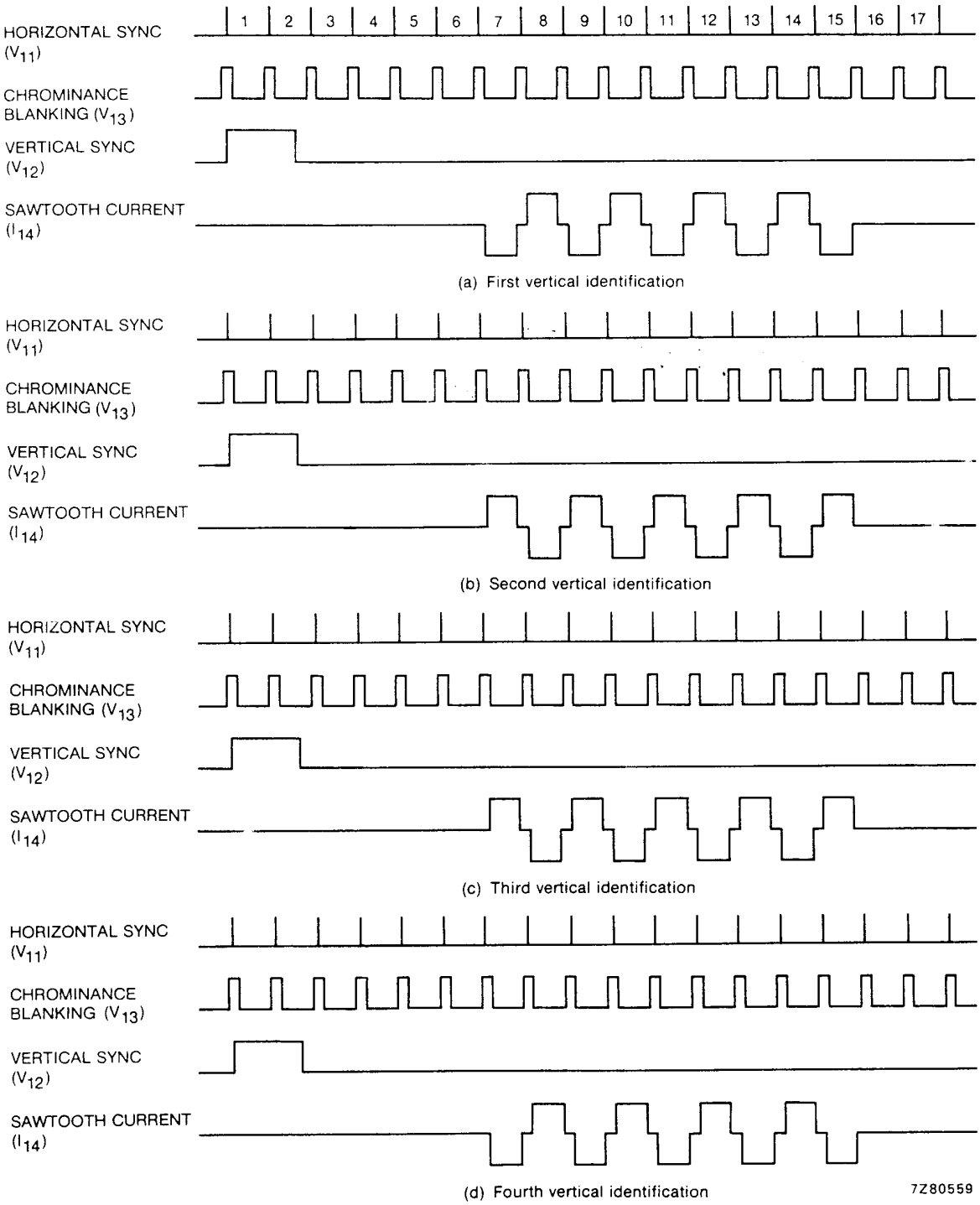


Fig. 4 Vertical identification generation.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating system IEC 134

Supply voltage	V_{4-1}	max. 13,2 V
Total power dissipation	P_{tot}	see Figs 5 and 6
Operating ambient temperature range	T_{amb}	−25 to +70 °C
Storage temperature range	T_{stg}	−55 to +150 °C

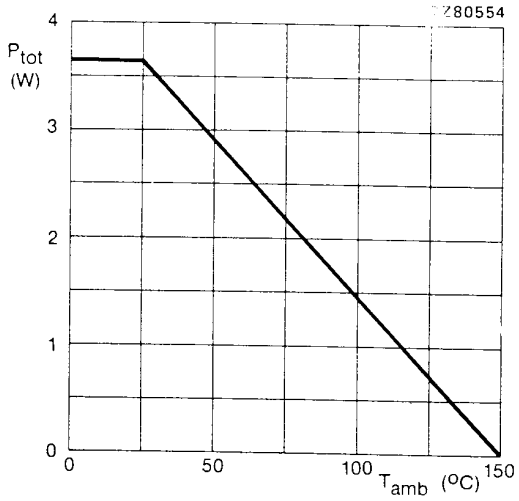


Fig. 5 Power derating curve for DIL package (SOT-101B).

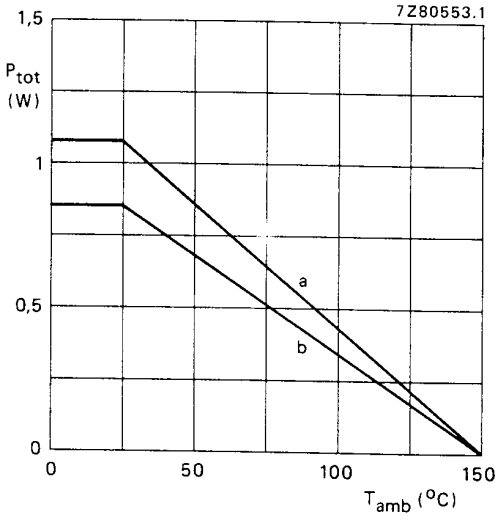


Fig. 6 Power derating curve.

a = device mounted on a ceramic substrate.
b = device mounted on a printed circuit board.

CHARACTERISTICS

$V_p = V_{4-2} = 5$ V; $T_{amb} = 25$ °C; all voltages are with reference to ground (pins 2 and 24); all currents stated are positive into the IC; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage (pin 4)	$V_p = V_{4-2}$	4.75	5	7	V
Supply current	$I_p = I_4$	30	45	60	mA
Reference voltage (pin 7)	V_{7-2}	3.4	3.55	3.7	V
Reference voltage (pin 22)	V_{22-24}	3.35	3.5	3.65	V
Pulse shaper (pins 9,11 and 12, emitter follower inputs; pin 18, collector output)					
Bias current (pins 9 and 12)	I_9, I_{12}	–	–	10	μA
Bias current (pin 11)	I_{11}	–	–	15	μA
Input resistance (pin 9,11,12)	R_9, R_{11}, R_{12}	200	–	–	kΩ
Input pulse amplitude (pin 9,11,12)	V_9, V_{11}, V_{12}	2.5	–	–	V
Timing pulse output (pin 18) high level	V_{18}	4.7	–	–	V
intermediate (V_p/2) level	V_{18}	2.2	2.5	2.8	V
low level	V_{18}	–	–	0.4	V
Pulse separator (pin 13, emitter follower)					
Input resistance	R_{13}	100	–	–	kΩ
Chrominance blanking pulse amplitude	V_{13}	3.6	–	–	V
D'_R*/D'_B* blanking pulse amplitude (colour killing)	V_{13}	1.7	1.8	1.9	V
Vertical identification sawtooth generator (pin 14)					
Voltage clamping level ($I_{14} = \pm 50$ μA	V_{14}	V_{22}−15 mV	V_{22}	V_{22}+15 mV	V
Ramp current (occurs in lines 7 to 15 after vertical sync)	$\pm I_{14}$	45	65	85	μA
Maximum voltage level	V_{14}	V_{22}+0.5	V_{22}+0.7	V_{22}+0.8	V
Minimum voltage level	V_{14}	V_{22}−0.8	V_{22}−0.7	V_{22}−0.5	V
Voltage level during line blanking	V_{14}	V_{22}−7 mV	V22	V_{22}+7 mV	V
Inputs D'_R*, D'_B* (pins 8 and 10)					
Signal level during clamping ($I_8, I_{10} = \pm 50$ μA)	V_8, V_{10}	V_7−25 mV	V7	V_7+25 mV	V
Input bias current	I_8, I_{10}	–	–	1.5	μA

parameter	symbol	min.	typ.	max.	unit
Sequential amplifier output (pin 6)					
(Pins 8 and 10 AC coupled to fixed DC voltage)					
DC output	V_6	1.6	$\frac{V_7}{2} - 10$ mV	1.85	V
Output resistance	R_6	–	8	16	Ω
Amplifier voltage gain (pin 8 or 10 to pin 6)	$G_{8,10\text{-}6}$	1.4	1.5	1.6	
Clamping and blanking stage (pin 5)					
Input voltage (clamped; $I_5 = \pm 50\ \mu A$)	V_5	$V_{22} - 12$ mV	V_{22}	$V_{22} + 12$ mV	V
Input bias current ($V_5 = V_{22}$)	I_5	–	–	2.5	μA
Modulator control circuit (pin 15, buffer amplifier non-inverting input)					
Bias current ($V_{15} = V_7$)	I_{15}	–	–	1.25	μA
Permitted input signal d.c. levels	V_{15}	2	–	4.3	V
FM modulator output (pin 23, emitter follower)					
Output resistance	R_{23}	–	50	80	Ω
High DC output level at $V_{21} = 3.8$ V	V_{23}	$V_{22} - 0.85$	–	$V_{22} - 0.7$	V
Output signal amplitude	V_{23}	0.9	1.0	1.15	V

CHARACTERISTICS (Continued)

parameter	symbol	min.	typ.	max.	unit
Chrominance blanking stage (pin 3, emitter follower input; pin 1, amplifier output)					
Input current ($V_3 = V_7$)	I_3	–	–	15	μA
Input resistance	R_3	300	–	–	kΩ
Required DC level of input signal	V_3	–	V_7	–	V
Output resistance	R_1	–	–	10	Ω
Temperature coefficient of output DC level	V_I/T	–	1.8	—	mV/K
Amplifier gain	$\Delta V_I/\Delta V_3$	1.69	1.75	1.79	
Output DC level during blanking(V_{13} = HIGH)	V_1	$V_7-0.88$	$V_7-0.79$	$V_7-0.70$	V
Output DC level unblanked ($V_3 = V_7$; V_{13} = LOW)	V_1	$V_7-0.88$	$V_7-0.79$	$V_7-0.70$	V

A.C. CHARACTERISTICS

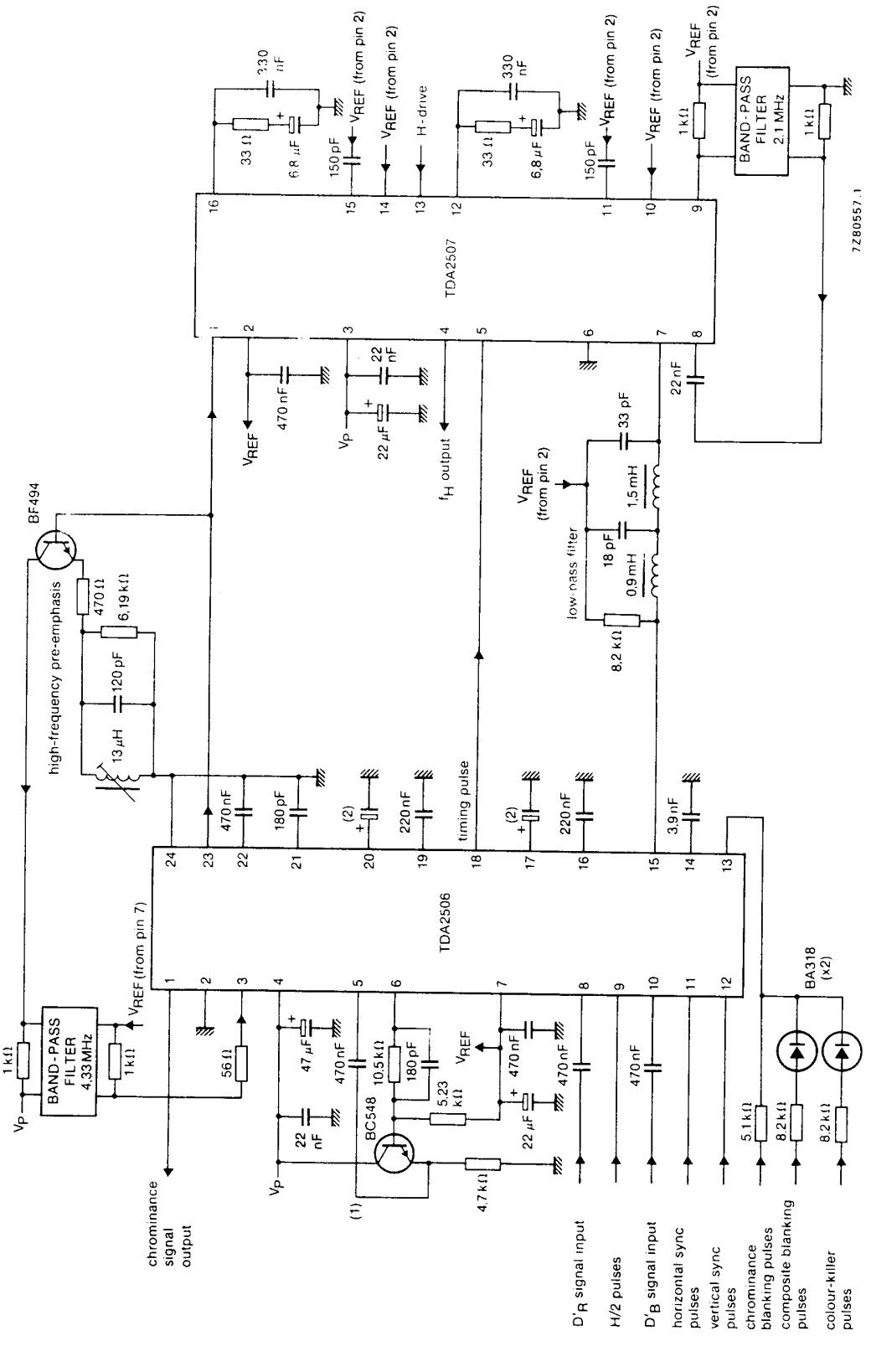
Values are valid for TDA2506 operating with TDA2507. Horizontal frequency (f_H) = 15 625 Hz.

parameter	symbol	min.	typ.	max.	unit
Centre frequency RED	f_{0R}	–	4 406,250 ± 2	–	kHz
Centre frequency BLUE	f_{0B}	–	4 250,000 ± 2	–	kHz
Ident. frequency RED *	f_{IdR}	–	4 756,250 ± 35	–	kHz
Ident. frequency BLUE *	f_{IdB}	–	3 900,000 ± 35	–	kHz
Minimum frequency RED **	$-f_R$	–	4 126,250 ± 12	–	kHz
Maximum frequency RED **	$+f_R$	–	4 686,250 ± 12	–	kHz
Minimum frequency BLUE **	$-f_B$	–	4 020,000 ± 12	–	kHz
Maximum frequency BLUE **	$+f_B$	–	4 480,000 ± 12	–	kHz

* The ident. frequencies are also the maximum and minimum output frequencies of the encoder.

** Values are valid for 75% colour bar saturation (EBU) (V_5 = ± 250 mV deviation from clamping level).

APPLICATION INFORMATION



(1) Signal amplitude for 75% colour bar (EBU) = 0,5 V (peak-to-peak value).
(2) For $V_P = 4{,}75$ to 5,3 V, $C_{17} = C_{20} = 0{,}68\ \mu F$; for $V_P > 5{,}3$ V, $C_{17} = C_{20} = 2{,}2\ \mu F$.

Fig. 7 Application using TDA2507 with PLL tuning: $V_P = 5$ V.